INDUSTRY STANDARD ANALOG ICs

DATABOOK

2nd EDITION

MAY 1993

USE IN LIFE SUPPORT DEVICES OR SYSTEMS MUST BE EXPRESSLY AUTHORIZED.

SGS-THOMSON PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF SGS-THOMSON Microelectronics. As used herein:

1. Life support devices or systems are those which (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided with the product, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can reasonably be expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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SELECTION GUIDE

SGS-THOMSON DATABOOKS

DESCRIPTION	ORDER CODE
4 BIT MCU FAMILY ET9400	DBET9400ST/1
8 BIT MCU FAMILIES EF6801/04/05	DB68XXST/1
16 BIT MPUs & ASSOCIATED PERIPHERALS	DB6800ST/1
AUDIO POWER and PROCESSING ICs	DBAUDIOPROST/1
AUTOMOTIVE PRODUCTS	DBAUTOMOTIVEST/2
CB12000 SERIES STANDARD CELLS	DBCB12ST/1
CB12000 SERIES STANDARD CELL MODULE GENERATORS	DBCB12GEN/1
ANALOG CELLS AND ARRAYS	DBANACA/1090
HIGH SPEED CMOS	DBHSCMOSST/1
IMAGE PROCESSING	DBIMAGEPROST/2
INDUSTRIAL and COMPUTER PERIPHERAL ICs	DBINCOMPEST/2
CB22000 SERIES STANDARD CELLS	DBCB22KST/1
ISB12000 SERIES CONTINUOUS ARRAYS	DBISB12KST/1
ISB24000 SERIES CONTINUOUS ARRAYS	DBISB24KST/1
LINE CARD ICs (Q1'93)	DBLINCARDST/2
LOW POWER SCHOTTKY TTL ICs	DBLPSST/1
VOLTAGE REGULATORS	BKVOLTAREST/1
POWER BIPOLAR TRANSISTORS	DBBIPTRANST/1
POWER MODULES	DBPOMODULEST/1
POWER MOS DEVICES	DBPOWERMOSST/2
GAL PROGRAMMABLE LOGIC DEVICES	DBPROLOGICST/1
PROTECTION DEVICES	DBPROTECST/2
RF & MICROWAVE POWER TRANSISTORS	DBRFST/2
SMALL SIGNAL TRANSISTORS	DBSMSIGST/1
CMOS B SERIES	DBCMOSBST/1
CMOS LINEAR	BKCMOSLINST/3
POWER SCHOTTKY DIODES	DBPOSCHODIOST/1
STATIC RAMs	DBSRAM/1
ISDN & DATACOM PRODUCTS	DBISDNICST/1
TELEPHONE SET ICs (Q1 '93)	DBTELSETST/2
COMPUTER GRAPHICS	DBGRAPHICST/2
THE L4970 SWITCHING REGULATOR IC FAMILY	BKL4970FA/0489
THE TRANSPUTER DATABOOK	DBTRANST/3
THE TRANSPUTER DEVELOPMENT AND iq SYSTEMS DATABOOK	72TRN21901
THE T9000 TRANSPUTER INSTRUCTION SET	DBT9000UMST/1
THE T9000 TRANSPUTER HARDWARE REFERENCE	DBT9000RMST/1
SCRs & TRIACS	DBSCRTRIST/2
VIDEO PRODUCTS SIGNAL PROCESSING	DBTVCRSPST/1
VIDEO PRODUCTS POWER & GRAPHICS	DBPOMGRAST/1
Z80 MICROPROCESSOR FAMILY	DBZ80ST/1
ZENER, SCHOTTKY & RECTIFIER DIODES	DBDIODEST/1
MEMORY DATABOOK	DBMEMORYST/2
ST6210/ST6215/ST6220/ST6225	DBST6ST/2
ST624X Family LCD DISPLAY CONTROL (Q2'93)	DBST624XFST/1
ST9 FAMILY 8/16 BIT MCU	DBST9ST/1
ST9040 FAMILY 8/16 BIT MCU	DBST9040FAST/1
SUBSYSTEMS PRODUCT PROFILE	BKSUBST/1
ST10 USER MANUAL	UMST10ST/1

OPERATIONAL AMPLIFIERS SELECTION GUIDE

COMMERCIAL TEMPERATURE RANGE (0 to +70°C)

DEVICE NUMBER	DESCRIPTION	TECHNOLOGY	ELECTRICAL CHARACTERISTICS (25°C)							
			V_{CC} (V) Min.	V_{CC} (V) Max.	Vio (mV) Max.	Iib (nA) Typ.	Icc (mA) Typ/amp	GBP (MHz) Typ.	SR (V/µS) Typ.	en (nV/√Hz) Typ.
SINGLE OP-AMPs (0 to +70°C)										
TSH150C*	**VERY HIGH SPEED BIP INPUTs**	**BICMOS**	6	12	5	100	23	**150**	**190**	**7**
TSH151C*	**VERY HIGH SPEED CMOS INPUTs SINGLE SUPPLY**	**BICMOS**	6	12	10	**0.025**	23	**150**	**200**	20
TS271C	PROGRAMMABLE **SINGLE SUPPLY**	CMOS	3	18	10	**0.001**	Prog	Prog	Prog	Prog
TS271AC	PROGRAMMABLE **SINGLE SUPPLY**	CMOS	3	18	5	**0.001**	Prog	Prog	Prog	Prog
TS271BC	PROGRAMMABLE **SINGLE SUPPLY**	CMOS	3	18	2	**0.001**	Prog	Prog	Prog	Prog
LF351	GENERAL PURPOSE	JFET	8	36	10	0.02	1.4	4	16	15
LF355	GENERAL PURPOSE	JFET	4	44	10	0.02	2	2.5	5	20
LF356	MEDIUM SPEED	JFET	4	44	10	0.02	5	5	12	12
LF357	HIGH SPEED	JFET	4	44	10	0.02	5	**20**	**50**	12
MC34001	GENERAL PURPOSE	JFET	8	36	10	0.02	1.4	4	16	15
MC34001A	GENERAL PURPOSE	JFET	8	36	2	0.02	1.4	4	16	15
MC34001B	GENERAL PURPOSE	JFET	8	36	5	0.02	1.4	4	16	15
TL061C	LOW CONSUMPTION	JFET	4	36	15	0.03	**0.2**	1	3.5	42
TL061AC	LOW CONSUMPTION	JFET	4	36	6	0.03	**0.2**	1	3.5	42
TL061BC	LOW CONSUMPTION	JFET	4	36	3	0.03	**0.2**	1	3.5	42
TL071C	GENERAL PURPOSE	JFET	8	36	10	0.02	1.4	4	16	15
TL071AC	GENERAL PURPOSE	JFET	8	36	6	0.02	1.4	4	16	15
TL071BC	GENERAL PURPOSE	JFET	8	36	3	0.02	1.4	4	16	15
TL081C	GENERAL PURPOSE	JFET	8	36	10	0.02	1.4	4	16	15
TL081AC	GENERAL PURPOSE	JFET	8	36	6	0.02	1.4	4	16	15
TL081BC	GENERAL PURPOSE	JFET	8	36	3	0.02	1.4	4	16	15

Note : All devices are available in DIP and SO packages.

* = New Product

DEVICE NUMBER	DESCRIPTION	TECHNOLOGY	ELECTRICAL CHARACTERISTICS (25°C)							
			V_{CC} (V) Min.	V_{CC} (V) Max.	Vio (mV) Max.	Iib (nA) Typ.	Icc (mA) Typ/amp	GBP (MHz) Typ.	SR (V/µS) Typ.	en ($nV/\sqrt{Hz}$) Typ.
SINGLE OP-AMPs (0 to +70°C) (continued)										
LM301A	GENERAL PURPOSE	BIPOLAR	4	44	7.5	70	1.8	1	0.5	25
LM308	GENERAL PURPOSE	BIPOLAR	7	44	7.5	0.6	0.3	0.8	0.15	20
LM308A	PRECISION	BIPOLAR	7	44	**0.5**	0.6	0.3	0.8	0.15	20
LM318	HIGH SPEED	BIPOLAR	7	40	10	160	5	**15**	**70**	17
TDB7910	**MEDIUM POWER 0.5A**	BIPOLAR	8	36	6	80	10	1	0.5	NS
UA741C	GENERAL PURPOSE	BIPOLAR	4	44	5	10	1.7	1	0.5	23
UA741E	GENERAL PURPOSE	BIPOLAR	4	44	2	10	1.7	1	0.5	23
UA748C	GENERAL PURPOSE	BIPOLAR	4	44	7.5	70	1.8	1	0.5	25
UA776C	PROGRAMMABLE	BIPOLAR	3	36	5	15	Prog	Prog	Prog	Prog
DUAL OP-AMPs (0 to +70°C)										
TS272C	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	10	**0.001**	1	3.5	5.5	25
TS272AC	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	5	**0.001**	1	3.5	5.5	25
TS272BC	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	2	**0.001**	1	3.5	5.5	25
TS27L2C	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	10	**0.001**	**0.01**	0.1	0.04	68
TS27L2AC	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	5	**0.001**	**0.01**	0.1	0.04	68
TS27L2BC	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	2	**0.001**	**0.01**	0.1	0.04	68
TS27M2C	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	10	**0.001**	0.15	1	0.6	32
TS27M2AC	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	5	**0.001**	0.15	1	0.6	32
TS27M2BC	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	2	**0.001**	0.15	1	0.6	32
TS902C*	**RAIL to RAIL LOW POWER STANDBY**	CMOS	**2.7**	18	12	**0.001**	0.35	1	1	40
TS902AC*	**RAIL to RAIL LOW POWER STANDBY**	CMOS	**2.7**	18	5	**0.001**	0.35	1	1	40

Note : All devices are available in DIP and SO packages.

* = New Product

NS : Non specified

DEVICE NUMBER	DESCRIPTION	TECHNOLOGY	ELECTRICAL CHARACTERISTICS (25°C)							
			V_{CC} (V) Min.	V_{CC} (V) Max.	Vio (mV) Max.	Iib (nA) Typ.	Icc (mA) Typ/amp	GBP (MHz) Typ.	SR (V/µS) Typ.	en (nV/√Hz) Typ.
DUAL OP-AMPs (0 to +70°C) (continued)										
TS902BC*	**RAIL to RAIL LOW POWER STANDBY**	CMOS	**2.7**	18	**1.5**	**0.001**	0.35	1	1	40
TS912C*	**RAIL to RAIL LOW POWER**	CMOS	**2.7**	18	12	**0.001**	0.35	1	1	40
TS912AC*	**RAIL to RAIL LOW POWER**	CMOS	**2.7**	18	5	**0.001**	0.35	1	1	40
TS912BC*	**RAIL to RAIL LOW POWER**	CMOS	**2.7**	18	**1.5**	**0.001**	0.35	1	1	40
LF353	GENERAL PURPOSE	JFET	8	36	10	0.02	1.4	4	16	15
MC34002	GENERAL PURPOSE	JFET	8	36	10	0.02	1.4	4	16	15
MC34002A	GENERAL PURPOSE	JFET	8	36	2	0.02	1.4	4	16	15
MC34002B	GENERAL PURPOSE	JFET	8	36	5	0.02	1.4	4	16	15
TL062C	LOW CONSUMPTION	JFET	4	36	15	0.03	**0.2**	1	3.5	42
TL062AC	LOW CONSUMPTION	JFET	4	36	6	0.03	**0.2**	1	3.5	42
TL062BC	LOW CONSUMPTION	JFET	4	36	3	0.03	**0.2**	1	3.5	42
TL072C	GENERAL PURPOSE	JFET	8	36	10	0.02	1.4	4	16	15
TL072AC	GENERAL PURPOSE	JFET	8	36	6	0.02	1.4	4	16	15
TL072BC	GENERAL PURPOSE	JFET	8	36	3	0.02	1.4	4	16	15
TL082C	GENERAL PURPOSE	JFET	8	36	10	0.02	1.4	4	16	15
TL082AC	GENERAL PURPOSE	JFET	8	36	6	0.02	1.4	4	16	15
TL082BC	GENERAL PURPOSE	JFET	8	36	3	0.02	1.4	4	16	15
LM358	SINGLE SUPPLY	BIPOLAR	3	32	7	20	0.35	1.1	0.6	55
LM358A	SINGLE SUPPLY	BIPOLAR	3	32	3	20	0.35	1.1	0.6	55
LS204C	LOW NOISE	BIPOLAR	3	36	3.5	100	0.4	2.5	1	**8**
MC1458	GENERAL PURPOSE	BIPOLAR	4	44	5	30	1.15	1	0.8	45
MC4558C	GENERAL PURPOSE	BIPOLAR	4	44	5	50	1.1	5.5	2.2	12
TEB1033	LOW NOISE	BIPOLAR	4	36	**1**	50	0.5	2	1	**8**

Note : All devices are available in DIP and SO packages.

* = New Product

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			V_{CC} (V) Min.	V_{CC} (V) Max.	Vio (mV) Max.	Iib (nA) Typ.	Icc (mA) Typ/amp	GBP (MHz) Typ.	SR (V/µS) Typ.	en (nV/√Hz) Typ.
QUAD OP-AMPs (0 to +70°C)										
TS274C	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	10	**0.001**	1	3.5	5.5	25
TS274AC	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	5	**0.001**	1	3.5	5.5	25
TS274BC	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	2	**0.001**	1	3.5	5.5	25
TS27L4C	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	10	**0.001**	**0.01**	0.1	0.04	68
TS27L4AC	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	5	**0.001**	**0.01**	0.1	0.04	68
TS27L4BC	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	2	**0.001**	**0.01**	0.1	0.04	68
TS27M4C	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	10	**0.001**	0.15	1	0.6	32
TS27M4AC	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	5	**0.001**	0.15	1	0.6	32
TS27M4BC	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	2	**0.001**	0.15	1	0.6	32
LF347	GENERAL PURPOSE	JFET	8	36	10	0.02	1.4	4	16	15
LF347B	GENERAL PURPOSE	JFET	8	36	5	0.02	1.4	4	16	15
MC34004	GENERAL PURPOSE	JFET	8	36	10	0.02	1.4	4	16	15
MC34004A	GENERAL PURPOSE	JFET	8	36	2	0.02	1.4	4	16	15
MC34004B	GENERAL PURPOSE	JFET	8	36	5	0.02	1.4	4	16	15
TL064C	LOW CONSUMPTION	JFET	4	36	15	0.03	**0.2**	1	3.5	42
TL064AC	LOW CONSUMPTION	JFET	4	36	6	0.03	**0.2**	1	3.5	42
TL064BC	LOW CONSUMPTION	JFET	4	36	3	0.03	**0.2**	1	3.5	42
TL074C	GENERAL PURPOSE	JFET	8	36	10	0.02	1.4	4	16	15
TL074AC	GENERAL PURPOSE	JFET	8	36	6	0.02	1.4	4	16	15
TL074BC	GENERAL PURPOSE	JFET	8	36	3	0.02	1.4	4	16	15
TL084C	GENERAL PURPOSE	JFET	8	36	10	0.02	1.4	4	16	15
TL084AC	GENERAL PURPOSE	JFET	8	36	6	0.02	1.4	4	16	15
TL084BC	GENERAL PURPOSE	JFET	8	36	3	0.02	1.4	4	16	15
LM324	SINGLE SUPPLY	BIPOLAR	3	32	7	20	0.17	1.3	0.4	40
LM324A	SINGLE SUPPLY	BIPOLAR	3	32	3	20	0.17	1.3	0.4	40

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QUAD OP-AMPs (0 to +70°C) (continued)										
LM346	PROGRAMMABLE	BIPOLAR	3	44	5	30	Prog	Prog	Prog	Prog
LM348	GENERAL PURPOSE	BIPOLAR	4	44	5	30	0.5	1.3	0.5	40
LS404C	LOW NOISE SINGLE SUPPLY	BIPOLAR	3	36	5	100	0.4	2.5	1	**8**
MC3403	GENERAL PURPOSE	BIPOLAR	3	36	5	40	0.7	1	0.7	43
TEB4033	LOW NOISE	BIPOLAR	4	36	**1**	50	0.5	2	1	**8**

INDUSTRIAL TEMPERATURE RANGE (-40 to +105°C)

SINGLE OP-AMPs (-40 to +105°C)

TSH150I*	**VERY HIGH SPEED BIP INPUTs**	BICMOS	6	12	5	100	23	**150**	**190**	**7**
TSH151I*	**VERY HIGH SPEED CMOS INPUTs SINGLE SUPPLY**	BICMOS	6	12	10	**0.025**	23	**150**	**200**	20
TS271I	PROGRAMMABLE **SINGLE SUPPLY**	CMOS	3	18	10	**0.001**	Prog	Prog	Prog	Prog
TS271AI	PROGRAMMABLE **SINGLE SUPPLY**	CMOS	3	18	5	**0.001**	Prog	Prog	Prog	Prog
TS271BI	PROGRAMMABLE **SINGLE SUPPLY**	CMOS	3	18	2	**0.001**	Prog	Prog	Prog	Prog
LF251	GENERAL PURPOSE	JFET	8	36	10	0.02	1.4	4	16	15
LF255	GENERAL PURPOSE	JFET	4	44	5	0.02	2	2.5	5	20
LF256	MEDIUM SPEED	JFET	4	44	5	0.02	5	5	12	12
LF257	HIGH SPEED	JFET	4	44	5	0.02	5	**20**	**50**	12
MC33001	GENERAL PURPOSE	JFET	8	36	10	0.02	1.4	4	16	15
MC33001A	GENERAL PURPOSE	JFET	8	36	2	0.02	1.4	4	16	15
MC33001B	GENERAL PURPOSE	JFET	8	36	5	0.02	1.4	4	16	15
TL061I	LOW CONSUMPTION	JFET	4	36	6	0.03	**0.2**	1	3.5	42
TL061AI	LOW CONSUMPTION	JFET	4	36	6	0.03	**0.2**	1	3.5	42
TL061BI	LOW CONSUMPTION	JFET	4	36	3	0.03	**0.2**	1	3.5	42
TL071I	GENERAL PURPOSE	JFET	8	36	6	0.02	1.4	4	16	15
TL071AI	GENERAL PURPOSE	JFET	8	36	6	0.02	1.4	4	16	15

Note : All devices are available in DIP and SO packages.

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SELECTION GUIDE

DEVICE NUMBER	DESCRIPTION	TECHNOLOGY	ELECTRICAL CHARACTERISTICS (25°C)							
			V_{CC} (V) Min.	V_{CC} (V) Max.	Vio (mV) Max.	Iib (nA) Typ.	Icc (mA) Typ/amp	GBP (MHz) Typ.	SR (V/µS) Typ.	en (nV/√Hz) Typ.
SINGLE OP-AMPs (-40 to +105°C) (continued)										
TL071BI	GENERAL PURPOSE	JFET	8	36	3	0.02	1.4	4	16	15
TL081I	GENERAL PURPOSE	JFET	8	36	6	0.02	1.4	4	16	15
TL081AI	GENERAL PURPOSE	JFET	8	36	6	0.02	1.4	4	16	15
TL081BI	GENERAL PURPOSE	JFET	8	36	3	0.02	1.4	4	16	15
LM201A	GENERAL PURPOSE	BIPOLAR	4	44	2	25	1.8	1	0.5	25
LM208	GENERAL PURPOSE	BIPOLAR	7	44	2	0.6	0.3	0.8	0.15	20
LM208A	PRECISION	BIPOLAR	7	44	**0.5**	0.6	0.3	0.8	0.15	20
LM218	HIGH SPEED	BIPOLAR	7	40	4	160	5	**15**	**70**	17
MC33171*	**LOW CONSUMPTION SINGLE SUPPLY**	BIPOLAR	4	44	4.5	20	**0.2**	2.1	2	30
OP07C	HIGH PRECISION	BIPOLAR	6	44	**0.15**	2	2.7	0.5	0.2	10
OP07D	HIGH PRECISION	BIPOLAR	6	44	**0.15**	2	2.7	0.5	0.2	10
TDA7910	**MEDIUM POWER 0.5A**	BIPOLAR	8	36	6	80	10	1	0.5	NS
UA741I	GENERAL PURPOSE	BIPOLAR	4	44	5	10	1.7	1	0.5	23
UA748I	GENERAL PURPOSE	BIPOLAR	4	44	2	25	1.8	1	0.5	25
UA776I	PROGRAMMABLE	BIPOLAR	3	36	5	15	Prog	Prog	Prog	Prog
DUAL OP-AMPs (-40 to +105°C)										
TS272I	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	10	**0.001**	1	3.5	5.5	25
TS272AI	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	5	**0.001**	1	3.5	5.5	25
TS272BI	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	2	**0.001**	1	3.5	5.5	25
TS27L2I	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	10	**0.001**	**0.01**	0.1	0.04	68
TS27L2AI	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	5	**0.001**	**0.01**	0.1	0.04	68
TS27L2BI	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	2	**0.001**	**0.01**	0.1	0.04	68
TS27M2I	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	10	**0.001**	0.15	1	0.6	32
TS27M2AI	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	5	**0.001**	0.15	1	0.6	32

Note : All devices are available in DIP and SO packages.

* = New Product

NS : Non specified

DEVICE NUMBER	DESCRIPTION	TECHNOLOGY	ELECTRICAL CHARACTERISTICS (25°C)							
			V_{CC} (V) Min.	V_{CC} (V) Max.	Vio (mV) Max.	Iib (nA) Typ.	Icc (mA) Typ/amp	GBP (MHz) Typ.	SR (V/µS) Typ.	en (nV/√Hz) Typ.
DUAL OP-AMPs (-40 to +105°C) (continued)										
TS27M2BI	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	2	**0.001**	0.15	1	0.6	32
TS902I*	**RAIL to RAIL LOW POWER STANDBY**	CMOS	**2.7**	18	12	**0.001**	0.35	1	1	32
TS902AI*	**RAIL to RAIL LOW POWER STANDBY**	CMOS	**2.7**	18	5	**0.001**	0.35	1	1	40
TS902BI*	**RAIL to RAIL LOW POWER STANDBY**	CMOS	**2.7**	18	**1.5**	**0.001**	0.35	1	1	40
TS912I*	**RAIL to RAIL LOW POWER**	CMOS	**2.7**	18	12	**0.001**	0.35	1	1	40
TS912AI*	**RAIL to RAIL LOW POWER**	CMOS	**2.7**	18	5	**0.001**	0.35	1	1	40
TS912BI*	**RAIL to RAIL LOW POWER**	CMOS	**2.7**	18	**1.5**	**0.001**	0.35	1	1	40
LF253	GENERAL PURPOSE	JFET	8	36	10	0.02	1.4	4	16	15
MC33002	GENERAL PURPOSE	JFET	8	36	10	0.02	1.4	4	16	15
MC33002A	GENERAL PURPOSE	JFET	8	36	2	0.02	1.4	4	16	15
MC33002B	GENERAL PURPOSE	JFET	8	36	5	0.02	1.4	4	16	15
TL062I	LOW CONSUMPTION	JFET	4	36	6	0.03	**0.2**	1	3.5	42
TL062AI	LOW CONSUMPTION	JFET	4	36	6	0.03	**0.2**	1	3.5	42
TL062BI	LOW CONSUMPTION	JFET	4	36	3	0.03	**0.2**	1	3.5	42
TL072I	GENERAL PURPOSE	JFET	8	36	6	0.02	1.4	4	16	15
TL072AI	GENERAL PURPOSE	JFET	8	36	6	0.02	1.4	4	16	15
TL072BI	GENERAL PURPOSE	JFET	8	36	3	0.02	1.4	4	16	15
TL082I	GENERAL PURPOSE	JFET	8	36	6	0.02	1.4	4	16	15
TL082AI	GENERAL PURPOSE	JFET	8	36	6	0.02	1.4	4	16	15
TL082BI	GENERAL PURPOSE	JFET	8	36	3	0.02	1.4	4	16	15
LM258	SINGLE SUPPLY	BIPOLAR	3	32	5	20	0.35	1.1	0.6	55
LM258A	SINGLE SUPPLY	BIPOLAR	3	32	3	20	0.35	1.1	0.6	55
LM2904	SINGLE SUPPLY	BIPOLAR	3	32	7	20	0.35	1.1	0.6	55
LM833*	**VERY LOW NOISE SINGLE SUPPLY**	BIPOLAR	4	36	5	300	2	**15**	7	**4.5**

Note : All devices are available in DIP and SO packages.

* = New Product

DEVICE NUMBER	DESCRIPTION	TECHNOLOGY	ELECTRICAL CHARACTERISTICS (25°C)							
			V_{CC} (V) Min.	V_{CC} (V) Max.	Vio (mV) Max.	Iib (nA) Typ.	Icc (mA) Typ/amp	GBP (MHz) Typ.	SR (V/µS) Typ.	en (nV/√Hz) Typ.
DUAL OP-AMPs (-40 to +105°C) (continued)										
LS204I	LOW NOISE	BIPOLAR	3	36	2.5	50	0.4	3	1.5	**8**
MC1458I	GENERAL PURPOSE	BIPOLAR	4	44	5	30	1.15	1	0.8	45
MC33078*	**VERY LOW NOISE SINGLE SUPPLY**	BIPOLAR	4	36	**2**	250	2	**15**	7	**4.5**
MC33172*	**LOW CONSUMPTION SINGLE SUPPLY**	BIPOLAR	4	44	4.5	20	**0.2**	**2.1**	2	30
MC4558I	GENERAL PURPOSE	BIPOLAR	4	44	5	50	1.1	5.5	2.2	12
TDA2320	**REMOTE CONTROL PREAMPLIFIER**	BIPOLAR	4	20	5	100	0.4	3	1.5	20
TDA2320A	**STEREO PREAMPLIFIER**	BIPOLAR	3	36	5	150	0.4	2.5	1.6	10
TEF1033	LOW NOISE	BIPOLAR	4	36	**1**	50	0.5	2	1	**8**
QUAD OP-AMPs (-40 to +105°C)										
TS274I	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	10	**0.001**	1	3.5	5.5	
TS274AI	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	5	**0.001**	1	3.5	5.5	25
TS274BI	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	2	**0.001**	1	3.5	5.5	25
TS27L4I	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	10	**0.001**	0.01	0.1	0.04	25
TS27L4AI	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	5	**0.001**	0.01	0.1	0.04	68
TS27L4BI	LOW CONSUMPTION SINGLE SUPPLY	CMOS	3	18	2	**0.001**	0.01	0.1	0.04	68
TS27M4I	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	10	**0.001**	0.15	1	0.6	68
TS27M4AI	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	5	**0.001**	0.15	1	0.6	32
TS27M4BI	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	2	**0.001**	0.15	1	0.6	32
LF247	GENERAL PURPOSE	JFET	8	36	10	0.02	1.4	4	16	15
MC33004	GENERAL PURPOSE	JFET	8	36	10	0.02	1.4	4	16	15
MC33004A	GENERAL PURPOSE	JFET	8	36	2	0.02	1.4	4	16	15
MC33004B	GENERAL PURPOSE	JFET	8	36	5	0.02	1.4	4	16	15

Note : All devices are available in DIP and SO packages.

* = New Product

DEVICE NUMBER	DESCRIPTION	TECHNOLOGY	ELECTRICAL CHARACTERISTICS (25°C)							
			V_{CC} (V) Min.	V_{CC} (V) Max.	Vio (mV) Max.	Iib (nA) Typ.	Icc (mA) Typ/amp	GBP (MHz) Typ.	SR (V/µS) Typ.	en (nV/√Hz) Typ.
QUAD OP-AMPs (-40 to +105°C) (continued)										
TL064I	LOW CONSUMPTION	JFET	4	36	6	0.03	**0.2**	1	3.5	42
TL064AI	LOW CONSUMPTION	JFET	4	36	6	0.03	**0.2**	1	3.5	42
TL064BI	LOW CONSUMPTION	JFET	4	36	3	0.03	**0.2**	1	3.5	42
TL074I	GENERAL PURPOSE	JFET	8	36	6	0.02	1.4	4	16	15
TL074AI	GENERAL PURPOSE	JFET	8	36	6	0.02	1.4	4	16	15
TL074BI	GENERAL PURPOSE	JFET	8	36	3	0.02	1.4	4	16	15
TL084I	GENERAL PURPOSE	JFET	8	36	6	0.02	1.4	4	16	15
TL084AI	GENERAL PURPOSE	JFET	8	36	6	0.02	1.4	4	16	15
TL084BI	GENERAL PURPOSE	JFET	8	36	3	0.02	1.4	4	16	15
LM224	SINGLE SUPPLY	BIPOLAR	3	32	5	20	0.17	1.3	0.4	40
LM224A	SINGLE SUPPLY	BIPOLAR	3	32	3	20	0.17	1.3	0.4	40
LM2902	SINGLE SUPPLY	BIPOLAR	3	32	7	20	0.17	1.3	0.4	40
LM246	PROGRAMMABLE	BIPOLAR	3	44	5	30	Prog	Prog	Prog	Prog
LM248	GENERAL PURPOSE	BIPOLAR	4	44	5	30	0.5	1.3	0.5	40
LS404I	LOW NOISE SINGLE SUPPLY	BIPOLAR	3	36	2.5	50	0.4	3	1.5	**8**
MC3303	GENERAL PURPOSE	BIPOLAR	3	36	5	40	0.7	1	0.7	43
MC33174*	**LOW CONSUMPTION SINGLE SUPPLY**	BIPOLAR	4	44	4.5	20	**0.2**	2.1	2	30
TEF4033	LOW NOISE	BIPOLAR	4	36	1	50	0.5	2	1	**8**

Note : All devices are available in DIP and SO packages.

* = New Product

MILITARY TEMPERATURE RANGE (-55 to +125°C)

DEVICE NUMBER	DESCRIPTION	TECHNOLOGY	ELECTRICAL CHARACTERISTICS (25°C)							
			V_{CC} (V) Min.	V_{CC} (V) Max.	Vio (mV) Max.	Iib (nA) Typ.	Icc (mA) Typ/amp	GBP (MHz) Typ.	SR (V/µS) Typ.	en (nV/√Hz) Typ.
SINGLE OP-AMPs (-55 to +125°C)										
TSH150M*	**VERY HIGH SPEED BIP INPUTs**	BICMOS	6	12	5	100	23	**150**	**190**	**7**
TSH151M*	**VERY HIGH SPEED CMOS INPUTs SINGLE SUPPLY**	BICMOS	6	12	10	**0.025**	23	**150**	**200**	20
TS271M	PROGRAMMABLE **SINGLE SUPPLY**	CMOS	3	18	10	**0.001**	Prog	Prog	Prog	Prog
TS271AM	PROGRAMMABLE **SINGLE SUPPLY**	CMOS	3	18	5	**0.001**	Prog	Prog	Prog	Prog
TS271BM	PROGRAMMABLE **SINGLE SUPPLY**	CMOS	3	18	2	**0.001**	Prog	Prog	Prog	Prog
LF151	GENERAL PURPOSE	JFET	8	36	10	0.02	1.4	4	16	15
LF155	GENERAL PURPOSE	JFET	4	44	5	0.02	2	2.5	5	20
LF156	MEDIUM SPEED	JFET	4	44	5	0.02	5	5	12	12
LF157	HIGH SPEED	JFET	4	44	5	0.02	5	**20**	**50**	12
MC35001	GENERAL PURPOSE	JFET	8	36	10	0.02	1.4	4	16	15
MC35001A	GENERAL PURPOSE	JFET	8	36	2	0.02	1.4	4	16	15
MC35001B	GENERAL PURPOSE	JFET	8	36	5	0.02	1.4	4	16	15
TL061M	LOW CONSUMPTION	JFET	4	36	6	0.03	**0.2**	1	3.5	42
TL061AM	LOW CONSUMPTION	JFET	4	36	6	0.03	**0.2**	1	3.5	42
TL061BM	LOW CONSUMPTION	JFET	4	36	3	0.03	**0.2**	1	3.5	42
TL071M	GENERAL PURPOSE	JFET	8	36	6	0.02	1.4	4	16	15
TL071AM	GENERAL PURPOSE	JFET	8	36	6	0.02	1.4	4	16	15
TL071BM	GENERAL PURPOSE	JFET	8	36	3	0.02	1.4	4	16	15
TL081M	GENERAL PURPOSE	JFET	8	36	6	0.02	1.4	4	16	15
TL081AM	GENERAL PURPOSE	JFET	8	36	6	0.02	1.4	4	16	15
TL081BM	GENERAL PURPOSE	JFET	8	36	3	0.02	1.4	4	16	15
LM101A	GENERAL PURPOSE	BIPOLAR	4	44	2	25	1.8	1	0.5	25
LM108	GENERAL PURPOSE	BIPOLAR	7	44	2	0.6	0.3	0.8	0.15	20
LM108A	PRECISION	BIPOLAR	7	44	**0.5**	0.6	0.3	0.8	0.15	20
LM118	HIGH SPEED	BIPOLAR	7	40	4	160	5	**15**	**70**	17

Note : All devices are available in DIP and SO packages.

* = New Product

DEVICE NUMBER	DESCRIPTION	TECHNOLOGY	ELECTRICAL CHARACTERISTICS (25°C)							
			V_{CC} (V) Min.	V_{CC} (V) Max.	Vio (mV) Max.	Iib (nA) Typ.	Icc (mA) Typ/amp	GBP (MHz) Typ.	SR (V/µS) Typ.	en (nV/√Hz) Typ.
SINGLE OP-AMPs (-55 to +125°C) (continued)										
MC35171*	**LOW CONSUMPTION SINGLE SUPPLY**	BIPOLAR	4	44	4.5	20	**0.2**	2.1	2	30
UA741A	GENERAL PURPOSE	BIPOLAR	4	44	5	10	1.7	1	0.5	23
UA741M	GENERAL PURPOSE	BIPOLAR	4	44	2	25	1.8	1	0.5	25
UA748M	GENERAL PURPOSE	BIPOLAR	4	44	2	25	1.8	1	0.5	23
UA776M	PROGRAMMABLE	BIPOLAR	3	36	5	15	Prog	Prog	Prog	Prog
DUAL OP-AMPs (-55 to +125°C)										
TS272M	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	10	**0.001**	1	3.5	5.5	25
TS272AM	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	5	**0.001**	1	3.5	5.5	25
TS272BM	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	2	**0.001**	1	3.5	5.5	25
TS27L2M	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	10	**0.001**	**0.01**	0.1	0.04	25
TS27L2AM	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	5	**0.001**	**0.01**	0.1	0.04	68
TS27L2BM	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	2	**0.001**	**0.01**	0.1	0.04	68
TS27M2M	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	10	**0.001**	0.15	1	0.6	32
TS27M2AM	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	5	**0.001**	0.15	1	0.6	32
TS27M2BM	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	2	**0.001**	0.15	1	0.6	32
TS902M*	**RAIL to RAIL LOW POWER STANDBY**	CMOS	2.7	18	12	**0.001**	0.35	1	1	40
TS902AM*	**RAIL to RAIL LOW POWER STANDBY**	CMOS	2.7	18	5	**0.001**	0.35	1	1	40
TS902BM*	**RAIL to RAIL LOW POWER STANDBY**	CMOS	2.7	18	**1.5**	**0.001**	0.35	1	1	40
TS912M*	**RAIL to RAIL LOW POWER**	CMOS	2.7	18	12	**0.001**	0.35	1	1	40
TS912AM*	**RAIL to RAIL LOW POWER**	CMOS	2.7	18	5	**0.001**	0.35	1	1	40
TS912BM*	**RAIL to RAIL LOW POWER**	CMOS	2.7	18	**1.5**	**0.001**	0.35	1	1	40

Note : All devices are available in DIP and SO packages.

* = New Product

SELECTION GUIDE

DEVICE NUMBER	DESCRIPTION	TECHNOLOGY	ELECTRICAL CHARACTERISTICS (25°C)							
			V_{CC} (V) Min.	V_{CC} (V) Max.	Vio (mV) Max.	Iib (nA) Typ.	Icc (mA) Typ/amp	GBP (MHz) Typ.	SR (V/µS) Typ.	en (nV/√Hz) Typ.
DUAL OP-AMPs (-55 to +125°C) (continued)										
LF153	GENERAL PURPOSE	JFET	8	36	10	0.02	1.4	4	16	15
MC35002	GENERAL PURPOSE	JFET	8	36	10	0.02	1.4	4	16	15
MC35002A	GENERAL PURPOSE	JFET	8	36	2	0.02	1.4	4	16	15
MC35002B	GENERAL PURPOSE	JFET	8	36	5	0.02	1.4	4	16	15
TL062M	LOW CONSUMPTION	JFET	4	36	6	0.03	**0.2**	1	3.5	42
TL062AM	LOW CONSUMPTION	JFET	4	36	6	0.03	**0.2**	1	3.5	42
TL062BM	LOW CONSUMPTION	JFET	4	36	3	0.03	**0.2**	1	3.5	42
TL072M	GENERAL PURPOSE	JFET	8	36	6	0.02	1.4	4	16	15
TL072AM	GENERAL PURPOSE	JFET	8	36	6	0.02	1.4	4	16	15
TL072BM	GENERAL PURPOSE	JFET	8	36	3	0.02	1.4	4	16	15
TL082M	GENERAL PURPOSE	JFET	8	36	6	0.02	1.4	4	16	15
TL082AM	GENERAL PURPOSE	JFET	8	36	6	0.02	1.4	4	16	15
TL082BM	GENERAL PURPOSE	JFET	8	36	3	0.02	1.4	4	16	15
LM158	SINGLE SUPPLY	BIPOLAR	3	32	5	20	0.35	1.1	0.6	55
LM158A	SINGLE SUPPLY	BIPOLAR	3	32	2	20	0.35	1.1	0.6	55
LS204M	LOW NOISE	BIPOLAR	3	36	2.5	50	0.4	3	1.5	**8**
MC1558	GENERAL PURPOSE	BIPOLAR	4	44	5	30	1.15	1	0.8	45
MC35172*	**LOW CONSUMPTION SINGLE SUPPLY**	BIPOLAR	4	44	4.5	20	**0.2**	2.1	2	30
TEC1033	LOW NOISE	BIPOLAR	4	36	**1**	50	0.5	2	1	**8**
QUAD OP-AMPs (-55 to +125°C)										
TS274M	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	10	**0.001**	1	3.5	5.5	
TS274AM	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	5	**0.001**	1	3.5	5.5	25
TS274BM	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	2	**0.001**	1	3.5	5.5	25
TS27L4M	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	10	**0.001**	**0.01**	0.1	0.04	68
TS27L4AM	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	5	**0.001**	**0.01**	0.1	0.04	68
TS27L4BM	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	2	**0.001**	**0.01**	0.1	0.04	68

Note : All devices are available in DIP and SO packages.

* = New Product

DEVICE NUMBER	DESCRIPTION	TECHNOLOGY	ELECTRICAL CHARACTERISTICS (25°C)							
			V_{CC} (V) Min.	V_{CC} (V) Max.	Vio (mV) Max.	Iib (nA) Typ.	Icc (mA) Typ/amp	GBP (MHz) Typ.	SR (V/µS) Typ.	en (nV/√Hz) Typ.
QUAD OP-AMPs (-55 to +125°C) (continued)										
TS27M4M	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	10	**0.001**	0.15	1	0.6	32
TS27M4AM	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	5	**0.001**	0.15	1	0.6	32
TS27M4BM	LOW CONSUMPTION **SINGLE SUPPLY**	CMOS	3	18	2	**0.001**	0.15	1	0.6	32
LF147	GENERAL PURPOSE	JFET	8	36	10	0.02	1.4	4	16	15
MC35004	GENERAL PURPOSE	JFET	8	36	10	0.02	1.4	4	16	15
MC35004A	GENERAL PURPOSE	JFET	8	36	2	0.02	1.4	4	16	15
MC35004B	GENERAL PURPOSE	JFET	8	36	5	0.02	1.4	4	16	15
TL064M	LOW CONSUMPTION	JFET	4	36	6	0.03	**0.2**	1	3.5	42
TL064AM	LOW CONSUMPTION	JFET	4	36	6	0.03	**0.2**	1	3.5	42
TL064BM	LOW CONSUMPTION	JFET	4	36	3	0.03	**0.2**	1	3.5	42
TL074M	GENERAL PURPOSE	JFET	8	36	6	0.02	1.4	4	16	42
TL074AM	GENERAL PURPOSE	JFET	8	36	6	0.02	1.4	4	16	15
TL074BM	GENERAL PURPOSE	JFET	8	36	3	0.02	1.4	4	16	15
TL084M	GENERAL PURPOSE	JFET	8	36	6	0.02	1.4	4	16	15
TL084AM	GENERAL PURPOSE	JFET	8	36	6	0.02	1.4	4	16	15
TL084BM	GENERAL PURPOSE	JFET	8	36	3	0.02	1.4	4	16	15
LM124	SINGLE SUPPLY	BIPOLAR	3	32	5	20	0.17	1.3	0.4	40
LM124A	SINGLE SUPPLY	BIPOLAR	3	32	3	20	0.17	1.3	0.4	40
LM146	PROGRAMMABLE	BIPOLAR	3	44	3	30	Prog	Prog	Prog	Prog
LM148	GENERAL PURPOSE	BIPOLAR	4	44	5	30	0.5	1.3	0.5	40
LS404M	LOW NOISE SINGLE SUPPLY	BIPOLAR	3	36	2.5	50	0.4	3	1.5	**8**
MC3503	GENERAL PURPOSE	BIPOLAR	3	36	5	40	0.7	1	0.7	43
MC35174*	**LOW CONSUMPTION SINGLE SUPPLY**	BIPOLAR	4	44	4.5	20	**0.2**	2.1	2	30
TEC4033	LOW NOISE	BIPOLAR	4	36	**1**	50	0.5	2	1	**8**

Note : All devices are available in DIP and SO packages.

* = New Product

COMPARATORS SELECTION GUIDE

COMMERCIAL TEMPERATURE RANGE (0 to +70°C)

DEVICE NUMBER	DESCRIPTION	TECHNOLOGY	ELECTRICAL CHARACTERISTICS (25°C)					
			V_{CC} (V) Min.	V_{CC} (V) Max.	Vio (mV) Max.	Iib (nA) Typ.	Icc (mA) Typ/comp	Tre (ns) Typ.
SINGLE								
LM311	GENERAL PURPOSE	BIPOLAR	5	36	7.5	100	5	200
DUAL								
TS3702C	VERY LOW CONSUMPTION **PUSH PULL OUTPUTS**	CMOS	3	18	5	**0.001**	**0.01**	700
TS393C	VERY LOW CONSUMPTION	CMOS	3	18	5	**0.001**	**0.01**	700
TS372C	LOW CONSUMPTION	CMOS	3	18	10	**0.001**	0.15	200
LM319	HIGH SPEED	BIPOLAR	5	36	8	250	4	**3.5**
LM393	GENERAL PURPOSE	BIPOLAR	2	36	5	25	0.2	300
LM393A	GENERAL PURPOSE	BIPOLAR	2	36	**2**	25	0.2	300
QUAD								
TS3704C	VERY LOW CONSUMPTION **PUSH PULL OUTPUTS**	CMOS	3	18	5	**0.001**	**0.01**	700
TS339C	VERY LOW CONSUMPTION	CMOS	3	18	5	**0.001**	**0.01**	700
TS374C	LOW CONSUMPTION	CMOS	3	18	10	**0.001**	0.15	200
LM339	GENERAL PURPOSE	BIPOLAR	2	36	5	25	0.2	300
LM339A	GENERAL PURPOSE	BIPOLAR	2	36	**2**	25	0.2	300

Note : All devices are available in DIP and SO packages.

INDUSTRIAL TEMPERATURE RANGE (-40 to +105°C)

DEVICE NUMBER	DESCRIPTION	TECHNOLOGY	ELECTRICAL CHARACTERISTICS (25°C)					
			V_{CC} (V) Min.	V_{CC} (V) Max.	Vio (mV) Max.	Iib (nA) Typ.	Icc (mA) Typ/comp	Tre (ns) Typ.
SINGLE								
LM211	GENERAL PURPOSE	BIPOLAR	5	36	3	60	5	200
DUAL								
TS3702I	VERY LOW CONSUMPTION **PUSH PULL OUTPUTS**	CMOS	3	18	5	**0.001**	**0.01**	700
TS393I	VERY LOW CONSUMPTION	CMOS	3	18	5	**0.001**	**0.01**	700
TS372I	LOW CONSUMPTION	CMOS	3	18	10	**0.001**	0.15	200
LM219	HIGH SPEED	BIPOLAR	5	36	4	150	4	**3.5**
LM293	GENERAL PURPOSE	BIPOLAR	2	36	5	25	0.2	300
LM293A	GENERAL PURPOSE	BIPOLAR	2	36	**2**	25	0.2	300
LM2903	GENERAL PURPOSE	BIPOLAR	2	36	7	25	0.2	300
QUAD								
TS3704I	VERY LOW CONSUMPTION **PUSH PULL OUTPUTS**	CMOS	3	18	5	**0.001**	**0.01**	700
TS339I	VERY LOW CONSUMPTION	CMOS	3	18	5	**0.001**	**0.01**	700
TS374I	LOW CONSUMPTION	CMOS	3	18	10	**0.001**	0.15	200
LM239	GENERAL PURPOSE	BIPOLAR	2	36	5	25	0.2	300
LM239A	GENERAL PURPOSE	BIPOLAR	2	36	**2**	25	0.2	300
LM2901	GENERAL PURPOSE	BIPOLAR	2	36	7	25	0.2	300

Note : All devices are available in DIP and SO packages.

MILITARY TEMPERATURE RANGE (-55 to +125°C)

DEVICE NUMBER	DESCRIPTION	TECHNOLOGY	ELECTRICAL CHARACTERISTICS (25°C)					
			V_{CC} (V) Min.	V_{CC} (V) Max.	Vio (mV) Max.	Iib (nA) Typ.	Icc (mA) Typ/comp	Tre (ns) Typ.
SINGLE								
LM111	GENERAL PURPOSE	BIPOLAR	5	36	7.5	60	5	200
DUAL								
TS3702M	VERY LOW CONSUMPTION **PUSH PULL OUTPUTS**	CMOS	3	18	5	**0.001**	**0.01**	700
TS393M	VERY LOW CONSUMPTION	CMOS	3	18	5	**0.001**	**0.01**	700
TS372M	LOW CONSUMPTION	CMOS	3	18	10	**0.001**	0.15	200
LM119	HIGH SPEED	BIPOLAR	5	36	4	150	4	**3.5**
LM193	GENERAL PURPOSE	BIPOLAR	2	36	5	25	0.2	300
LM193A	GENERAL PURPOSE	BIPOLAR	2	36	**2**	25	0.2	300
QUAD								
TS3704M	VERY LOW CONSUMPTION **PUSH PULL OUTPUTS**	CMOS	3	18	5	**0.001**	**0.01**	700
TS339M	VERY LOW CONSUMPTION	CMOS	3	18	5	**0.001**	**0.01**	700
TS374M	LOW CONSUMPTION	CMOS	3	18	10	**0.001**	0.15	200
LM139	GENERAL PURPOSE	BIPOLAR	2	36	5	25	0.2	300
LM139A	GENERAL PURPOSE	BIPOLAR	2	36	**2**	25	0.2	300

Note : All devices are available in DIP and SO packages.

TIMERS SELECTION GUIDE

COMMERCIAL TEMPERATURE RANGE (0 to +70°C)

DEVICE NUMBER	DESCRIPTION	TECHNOLOGY	ELECTRICAL CHARACTERISTICS (25°C)			
			V_{CC} (V) Min.	V_{CC} (V) Max.	Icc (mA) Typ/timer	Ma x. Frequency (MHz) Typ
SINGLE						
TS555C	LOW POWER	CMOS	2	18	**0.1**	**2.7**
TS3V555C*	**LOW POWER**	CMOS	2	18	**0.1**	**2.7**
TS3V555AC*	**LOW POWER (1.5V)**	CMOS	**1.5**	18	**0.1**	**2.7**
NE555	GENERAL PURPOSE	BIPOLAR	4.5	16	3	0.5
DUAL						
TS556C	LOW POWER	CMOS	2	18	**0.1**	**2.7**
NE556	GENERAL PURPOSE	BIPOLAR	4.5	16	3	0.5

INDUSTRIAL TEMPERATURE RANGE (-40 to +105°C)

DEVICE NUMBER	DESCRIPTION	TECHNOLOGY	ELECTRICAL CHARACTERISTICS			
			V_{CC} (V) Min.	V_{CC} (V) Max.	Icc (mA) Typ/timer	Ma x. Frequency (MHz) Typ
SINGLE						
TS555I	LOW POWER	CMOS	2	18	**0.1**	**2.7**
TS3V555I*	**LOW POWER**	CMOS	2	18	**0.1**	**2.7**
TS3V555AI*	**LOW POWER (1.5V)**	CMOS	**1.5**	18	**0.1**	**2.7**
SA555	GENERAL PURPOSE	BIPOLAR	4.5	16	3	0.5
DUAL						
TS556I	LOW POWER	CMOS	2	18	**0.1**	**2.7**
SA556	GENERAL PURPOSE	BIPOLAR	4.5	16	3	0.5

Note : All devices are available in DIP and SO packages.

* = New Product

MILITARY TEMPERATURE RANGE (-55 to +125°C)

DEVICE NUMBER	DESCRIPTION	TECHNOLOGY	ELECTRICAL CHARACTERISTICS			
			V_{CC} (V) Min.	V_{CC} (V) Max.	Icc (mA) Typ/timer	Ma x. Frequency (MHz) Typ
SINGLE						
TS555M	LOW POWER	CMOS	2	18	**0.1**	**2.7**
TS3V555M*	**LOW POWER**	CMOS	2	18	**0.1**	**2.7**
TS3V555AM*	**LOW POWER (1.5V)**	CMOS	**1.5**	18	**0.1**	**2.7**
SE555	GENERAL PURPOSE	BIPOLAR	4.5	16	3	0.5
DUAL						
TS556M	LOW POWER	CMOS	2	18	**0.1**	**2.7**
SE556	GENERAL PURPOSE	BIPOLAR	4.5	16	3	0.5

Note : All devices are available in DIP and SO packages.

* = New Product

SELECTION BY DESIGN PARAMETERS

LOW OFFSET VOLTAGE

Max Input Offset Voltage (25°C)

≤150µV	≤1mV	≤2mV
OP07C	LM308A	MC33078
OP07D	TEB1033	MC34001A
	TEB4033	MC34002A
		MC34004A
		TS271B
		TS272B
		TS27L2B
		TS27M2B
		TS274B
		TS27L4B
		TS27M4B
		TS902B
		TS912B

LOW NOISE

Typ Equivalent Input Noise Voltage

(f = 1kHz, R_s = 100Ω, 25°C)

≤5nV/√Hz	≤8nV/√Hz	≤15nV/√Hz	≤25nV/√Hz
LM833	LS204	LF347	LF355
MC33078	LS404	LF351	LF356
	TEB1033	LF353	LF357
	TEB4033	MC34001	LM301A
	TSH150	MC34002	LM308
		MC34004	LM318
		MC4558	TDA2320
		OP07C	TS271
		OP07D	TS272
		TDA2320A	TS274
		TL071	TSH151
		TL072	UA741
		TL074	UA748
		TL081	UA776
		TL082	
		TL084	

VERY LOW BIAS CURRENT

Typ Input Bias Current (25°C)

≤1pA	≤20pA
TS271	LF347
TS272	LF351
TS27L2	LF353
TS27M2	LF355
TS274	LF356
TS27L4	LF357
TS27M4	MC34001
TS902	MC34002
TS912	MC34004
TSH151	TL061
	TL062
	TL064
	TL071
	TL072
	TL074
	TL081
	TL082
	TL084

LOW CONSUMPTION

Typ Supply Current per Amplifier (25°C)

≤10µA	≤250µA	≤500µA
TS271	LM346	LM308
TS27L2	MC33171	LM324
TS27L4	MC33172	LM346
	MC33174	LM348
	TL061	LM358
	TL062	LS204
	TL064	LS404
	TS27M2	TDA2320
	TS27M4	TDA2320A
	UA776	TEB1033
		TEB4033
		TS902
		TS912

SELECTION BY DESIGN PARAMETERS

HIGH SPEED

Typ Gain Bandwidth Product (25°C)

≤3MHz	≤10MHz	≤100MHz
LF347	LF357	TSH150
LF351	LM318	TSH151
LF353	LM833	
LF356	MC33078	
LS204		
LS404		
MC34001		
MC34002		
MC34004		
MC4558		
TDA2320		
TDA2320A		
TL071		
TL072		
TL074		
TL081		
TL082		
TL084		
TS271		
TS272		
TS274		

LOW VOLTAGE

Min Operating Supply Voltage

≤2.7V	≤3V	≤5V
TS902*	LM324	LF355
TS912*	LM348	LF356
	LM358	LF357
	LS204	LM301A
	LS404	LM348
	MC3403	LM833
	TDA2320	MC1458
	TDA2320A	MC33078
	TS271	MC33171
	TS272	MC33172
	TS27L2	MC33174
	TS27M2	TEB1033
	TS274	TEB4033
	TS27L4	TL061
	TS27M4	TL062
	UA776	TL064
		UA741
		UA748

SWITCHING REGULATORS SELECTION GUIDE

BCD HIGH CURRENT

PARAMETER	L4970A	L4977A	L4975A	L4974A	L4972A	L4972AD
Max. Input Op. Voltage	50V	50V	50V	50V	50V	50V
Output Voltage Range	5.1V to 40V ±2% (Internal Reference)					
Max. Output Current	10A	7A	5A	3.5A	2A	2A
Power Switch	DMOS R_{DSON} 0.1Ω (Typ.)					
Switch Mode Control System	Continuous Mode, Direct Duty Cycle Control with Feed Forward (Improved Transient Response)					
Chopping Frequency	500kHz	500kHz	500kHz	200kHz	200kHz	200kHz
Efficiency V_{IN} = 35V V_O = 5.1V 100kHz	10A 83%	7A 84%	5A 84%	3.5A 84%	2A 83%	2A 83%
Current Limiting	True Current Generator					
Soft Start	Yes					
Reset and Power Fail	Yes					
Crowbar	Yes					
Package	Multiwatt15	Multiwatt15	Multiwatt15	Powerdip 16+2+2	Powerdip 16+2+2	SO20 16+2+2
Max. $R_{thj\text{-}case\ (PIN)}$	3°C/W	3°C/W	3°C/W	12°C/W	12°C/W	15°C/W

BIPOLAR HIGH CURRENT

PARAMETER	L296P	L4960	L4962	L4964	L4963	L4963D
Output Current	4A	2.5A	1.5A	4A	1.5A	0.5A
fsw	100kHz				variable	
Input Voltage	9V to 46V				9V to 46V	
Output Voltage	5.1V to 40V				5.1V to 36V	
Current Limiting	Soft Start Triggers				Constant Current	
Operating Mode	Continuous Mode				Discontinuous Mode	
Soft Start	yes				no	
Reset and Power Fail	yes	no	no	yes	yes	yes
Crowbar	yes	no	no	yes	no	no
Package	Multiwatt15	Heptawatt	Powerdip 12+2+2	Multiwatt15	Powerdip 16+3+3	SO20 16+2+2
Max. $R_{thj\text{-}case\ (PIN)}$	3°C/W	4°C/W	14°C/W	3°C/W	12°C/W	15°C/W

PWM CONTROLLER SELECTION GUIDE

Operating Temperature: 0 to 70°C

Parameter	SG3524	SG3525A	SG3527A	UC3842	UC3843	UC3844	UC3845
Voltage Reference	±8%	±2%	±2%	±2%	±2%	±2%	±2%
Soft Start		●	●				
PWM Latch		●	●	●	●	●	●
Under Voltage Lockout		●	●	●	●	●	●
Pulse by Pulse Current Limiting				●	●	●	●
Shutdown Terminal	●	●	●	●	●	●	●
Output Current (A)	0.1	0.1	0.1	0.2	0.2	0.2	0.2
Max. Oscillator Frequency (KHz)	300	500	500	500	500	500	500
Dual Uncommited Outputs	●	●	●				
Single Ended Output				●	●	●	●
Totem Pole Outputs		●	●				
Separate Oscillator Synch. Terminal		●	●				
Adjustable Deadtime Control		●	●				
Low Current Start-Up				●	●	●	●
Package	DIP16			Minidip			

PWM CONTROLLER SELECTION GUIDE cont'd

Operating Temperature: –25 to 85 °C

Parameter	SG2524	SG2525A	SG2527A	UC2842	UC2843	UC2844	UC2845
Voltage Reference	±4%	±1%	±1%	±1%	±1%	±1%	±1%
Soft Start		●	●				
PWM Latch		●	●	●	●	●	●
Under Voltage Lockout		●	●	●	●	●	●
Pulse by Pulse Current Limiting				●	●	●	●
Shutdown Terminal	●	●	●	●	●	●	●
Output Current (A)	0.1	0.1	0.1	0.2	0.2	0.2	0.2
Max. Oscillator Frequency (KHz)	300	500	500	500	500	500	500
Dual Uncommited Outputs	●	●	●				
Single Ended Output				●	●	●	●
Totem Pole Outputs		●	●				
Separate Oscillator Synch. Terminal		●	●				
Adjustable Deadtime Control		●	●				
Low Current Start-Up				●	●	●	●
Package	DIP16			Minidip			

DARLINGTON ARRAYS SELECTION GUIDE

Type	N.	V_{CEX}	Io	Input	Configuration	Package
L601	8	90V	0.5A	General Purpose	● ▶|	PLASTIC DIP-16
L602	8	90V	0.4A	14-25V PMOS	● ▶|	
L603	8	90V	0.4A	5V TTL/CMOS	● ▶|	
L604	8	90V	0.4A	6-15V CMOS/PMOS	● ▶|	
L702B	4	90V	2A	5V TTL	●	
L702N	4	90V	2A	5V TTL	●	MULTIWATT 11
L7150	4	50V	1.5A	5V TTL/CMOS	● ▶|	MULTIWATT 15
L7152	4	50V	1.5A	6-15V CMOS/PMOS	● ▶|	
L7180	4	80V	1.5A	5V TTL/CMOS	● ▶|	
L7182	4	80V	1.5A	6-15V CMOS/PMOS	● ▶|	
ULN2001A/D	7	50V	0.5A	General Purpose	● ▶|	PLASTIC DIP-16 AND SO 16
ULN2002 A/D	7	50V	0.5A	14-25V PMOS	● ▶|	
ULN2003 A/D	7	50V	0.5A	5V TTL/CMOS	● ▶|	
ULN2004 A/D	7	50V	0.5A	6-15V CMOS/PMOS	● ▶|	
ULQ2001A/D	7	50V	0.5A	General Purpose	● ▶|	
ULQ2002 A/D	7	50V	0.5A	14-25V PMOS	● ▶|	
ULQ2003 A/D	7	50V	0.5A	5V TTL/CMOS	● ▶|	
ULQ2004 A/D	7	50V	0.5A	6-15V CMOS/PMOS	● ▶|	

● = Common emitters.
▶\| = Integral suppression diodes.
■ = Isolated darlingtons.
▷ = Predriver stage.

DARLINGTON ARRAYS SELECTION GUIDE cont'd

Type	N.	V_{CEX}	Io	Input	Configuration	Package
ULN2064B	4	50V	1.5A	5V TTL/CMOS	● ▶|	PLASTIC DIP-16
ULN2065B	4	80V	1.5A	5V TTL/CMOS	● ▶|	
ULN2066B	4	50V	1.5A	6-15V CMOS/PMOS	● ▶|	
ULN2067B	4	80V	1.5A	6-15V CMOS/PMOS	● ▶|	
ULN2068B	4	50V	1.5A	5V CMOS/TTL	▷ ● ▶|	
ULN2069B	4	80V	1.5A	5V CMOS/TTL	▷ ● ▶|	
ULN2070B	4	50V	1.5A	6-15V COS/PMOS	▷ ● ▶|	
ULN2071B	4	80V	1.5A	6-15V CMOS/PMOS	▷ ● ▶|	
ULN2074B	4	50V	1.5A	General Purpose	■	
ULN2075B	4	80V	1.5A	General Purpose	■	
ULN2076B	4	50V	1.5A	6-15V CMOS/PMOS	■	
ULN/ULQ2077B	4	80V	1.5A	6-15V CMOS/PMOS	■	
ULN/ULQ2801A	8	50V	0.5A	General Purpose	●	PLASTIC DIP-18
ULN/ULQ2802A	8	50V	0.5A	14-25V PMOS	●	
ULN/ULQ2803A	8	50V	0.5A	5V TTL/CMOS	●	
ULN/ULQ2804A	8	50V	0.5A	6-15V CMOS/PMOS	●	
ULN/ULQ2805A	8	50V	0.5A	High Output TTL	●	

● = Common emitters.
▶| = Integral suppression diodes.
■ = Isolated darlingtons.
▷ = Predriver stage.

MISCELLANOUS SELECTION GUIDE

Type	Description	Packages
L6180/1	Octal Line Driver	DIP28/PLCC28
L6506/D	Current Controller for Stepping Motors	DIP8/SO20
TL7700A	Supply Voltage Supervisors	MINIDIP SO-8

LINEAR DRIVERS SELECTION GUIDE

Type	Description	Packages
L165	Power Operational Amplifier	PENTAWATT
L272	Dual Power Operational Amplifier	DIP-16
L272D	Dual Power Operational Amplifier	SO16
L272M	Dual Power Operational Amplifier	MINIDIP
L2720	Dual Power Operational Amplifier	8+8
L2722	Dual Power Operational Amplifier	MINIDIP
L2724	Dual Power Operational Amplifier	SIP-9
L2726	Dual Power Operational Amplifier	SO20
L2750	Dual High Power Operational Amplifier	MULTIWATT 11
L6242	Voice Coil Motor Driver	SO20

LINEAR DRIVERS/RECEIVERS SELECTION GUIDE

Type	Function	Temperature Range (°C)	Rise Time (ns)	Delay Time (ns)	Supply Current (mA)	Max Supply (V)	Package
L5170	Driver	0 to 70	–	–	30	15	DIP28/PLCC28
MC1488 D	Driver	0 to 75	55	110/275	18	30	SO-14
MC1489 D MC1489 AD	Receivers	0 to 75	120 120	25 25	16 16	10	SO-14
MC1488 P	Driver	0 to 75	55	110/275	18	30	DIP-14
MC1489 AP MC1489 P	Receivers	0 to 75	120 120	25 25	16 16	10	DIP-14
MC1488 L	Driver	0 to 75	55	110/275	18	30	CERAMIC DIP-14
MC1489 AL MC1489 L	Receivers	0 to 75	120 120	25 25	16 10	10	CERAMIC DIP-14

OTHER PROPRIETARY REGULATORS SELECTION GUIDE

Io Max. (A)	Type	Output Voltage				Package	Notes
		5V	8.5V	10V	12V		
2	L200	5.1V <— Adjustable —> 40V				Pentawatt	
1	TDA8137 (*)	●				Heptawatt	
	TDA8138 (*)	●			●	SIP9	
	TDA8138A (*)	●			●	Heptawatt	+ Disable
	TDA8138B (*)	●			●		+ Reset
	TDA8139 (*)	5.1V + Adjustable				SIP9	+ Reset + Disable
0.6	TDA8134 (*)	●			●	Heptawatt	
	TDA8135 (*)	5.1V + Adjustable					
	TDA8136 (*)				●		
0.5	L4901A (*)	●				Heptawatt	+ Reset
	L4902A (*)	●				Heptawatt	+ Reset + Disable
	L4903 (*)	●				Minidip	+ Reset + Disable
	L4904A (*)	●				Minidip	+ Reset
	L4905 (*)	●				Heptawatt	+ Reset

(*) DUAL

AUTOMATIC VOLTAGE SWITCH SELECTION GUIDE

Type Number	Description	Packages
AVS08	Automatic Mains Selector (110/220V AC) for SMPS<200W	DIP8/TO220AB
AVS10	Automatic Mains Selector (110/220V AC) for SMPS<300W	DIP8/TO220AB
AVS12	Automatic Mains Selector (110/220V AC) for SMPS<500W	DIP8/TO220AB
AVS20	Automatic Mains Selector (110/220V AC) for SMPS<300W	DIP8/TO220AB

INDUSTRY STANDARD	NEAREST SGS-THOMSON TYPE
BURR BROWN	
OPA620KP	TSH150CN
OPA620KU	TSH150CD
ELANTEC	
EL2073CN	TSH150CN
EL2073CS	TSH150CD
HARRIS (Including GE/RCA/INTERSIL)	
CA081AE	TL081ACN
CA081BE	TL081BCN
CA081E	TL081CN
CA082AE	TL082ACN
CA082BE	TL082BCN
CA082E	TL082CN
CA084AE	TL084ACN
CA084BE	TL084BCN
CA084E	TL084CN
CA124E	LM124N
CA139AF	LM139AJ
CA139E	LM139N
CA139F	LM139J
CA1458E	MC1458N
CA1558E	MC1558N
CA158E	LM158N
CA224E	LM224N
CA239AE	LM239AN
CA239AF	LM239AJ
CA239E	LM239N
CA239F	LM239J
CA258E	LM258N
CA2901E	LM2901N
CA2901F	LM2901J
CA2902E	LM2902N
CA2904E	LM2904N
CA301AE	LM301AN
CA311E	LM311N
CA324E	LM324N
CA3290E	LM393N
CA339AE	LM339AN
CA339AF	LM339AJ
CA339E	LM339N
CA339F	LM339J
CA358AE	LM358AN
CA358E	LM358N

INDUSTRY STANDARD	NEAREST SGS-THOMSON TYPE
CA555E	NE555N
CA741CE	UA741CN
CA741CT	UA741CH
CA741E	UA741EN
CA741T	UA741H
CA748CE	UA748CN
CA748CT	UA748CH
CA748T	UA748J
ICM7555CBA	TS555CD
ICM7555IPA	TS555IN
ICM7556IPD	TS556IN
MOTOROLA	
LF347BN	LF347BN
LF347N	LF347N
LF351D	LF351D
LF351N	LF351N
LF353D	LF353D
LF353N	LF353N
LF355J	LF355J
LF356J	LF356J
LF357J	LF357J
LM124J	LM124J
LM139AJ	LM139AJ
LM139J	LM139J
LM148J	LM148J
LM158J	LM158J
LM201AD	LM201AD
LM201AN	LM201AN
LM208AD	LM208AD
LM208AN	LM208AN
LM208D	LM208D
LM208N	LM208N
LM211D	LM211D
LM224D	LM224D
LM224J	LM224J
LM239AJ	LM239AJ
LM239D	LM239D
LM239J	LM239J
LM248J	LM248J
LM258D	LM258D
LM2901D	LM2901D
LM2901J	LM2901J
LM2901N	LM2901N
LM2902D	LM2902D

INDUSTRY STANDARD	NEAREST SGS-THOMSON TYPE
LM2902J	LM2902J
LM2902N	LM2902N
LM2903D	LM2903D
LM2903N	LM2903N
LM2904D	LM2904D
LM2904N	LM2904N
LM301AD	LM301AD
LM301AJ	LM301AJ
LM301AN	LM301AN
LM308AD	LM308AD
LM308AJ-8	LM308AJ
LM308AN	LM308AN
LM308D	LM308D
LM308J	LM308J
LM308N	LM308N
LM311D	LM311D
LM311J	LM311J
LM311N	LM311N
LM324AD	LM324AD
LM324AN	LM324AN
LM324AJ	LM324AJ
LM324D	LM324D
LM324J	LM324J
LM324N	LM324N
LM339AJ	LM339AJ
LM339AN	LM339AN
LM339D	LM339D
LM339N	LM339N
LM348D	LM348D
LM348J	LM348J
LM348N	LM348N
LM358D	LM358D
LM358J	LM358J
LM358N	LM358N
LM393AN	LM393AN
LM393D	LM393D
LM393N	LM393N
LM833D	LM833D
LM833N	LM833N
MC1455D	NE555D
MC1455P1	NE555N
MC1455U	NE555J
MC1458D	MC1458D
MC1458P1	MC1458N

INDUSTRY STANDARD	NEAREST SGS-THOMSON TYPE
MOTOROLA (cont'd)	
MC1458U	MC1458J
MC1555U	SE555J
MC1558U	MC1558J
MC1741CD	UA741CD
MC1741CG	UA741CH
MC1741CP1	UA741CN
MC1741CU	UA741CJ
MC1741G	UA741MH
MC1741U	UA741MJ
MC1748CD	UA748CD
MC1748CG	UA748CH
MC1748CP1	UA748CN
MC1748CU	UA748CJ
MC1748G	UA748MH
MC1748U	UA748MJ
MC1776CD	UA776CD
MC1776CG	UA776CH
MC1776CP1	UA776CN
MC1776G	UA776MH
MC3302D	LM239D
MC3302L	LM239J
MC3302P	LM239N
MC3303D	MC3303D
MC3303L	MC3303J
MC3303P	MC3303N
MC33078D	MC33078D
MC33078P	MC33078N
MC33171D	MC33171D
MC33171P	MC33171N
MC33172D	MC33172D
MC33172P	MC33172N
MC33174D	MC33174D
MC33174P	MC33174N
MC34001AP	MC34001AN
MC34001BP	MC34001BN
MC34001P	MC34001N
MC34002AP	MC34002AN
MC34002BP	MC34002BN
MC34002P	MC34002N
MC34004AP	MC34004AN
MC34004BP	MC34004BN
MC34004P	MC34004N
MC3403D	MC3403D
MC3403L	MC3403J
MC3403P	MC3403N
MC3456L	NE556J
MC3456P	NE556N
MC3503L	MC3503J
MC3556L	SE556J
MC4558CD	MC4558CN
MC4558CP1	MC4558CN
MC4558CU	MC4558CJ
TL061ACD	TL061ACD
TL061ACP	TL061ACN
TL061CD	TL061CD
TL061CP	TL061CN
TL061MJG	TL061MJ
TL061VD	TL061ID
TL061VP	TL061IN
TL062ACD	TL062ACD
TL062ACP	TL062ACN
TL062CD	TL062CD
TL062CP	TL062CN
TL062MJG	TL062MJ
TL062VD	TL062ID
TL062VP	TL062IN
TL064ACD	TL064ACD
TL064ACN	TL064ACN
TL064CD	TL064CD
TL064CN	TL064CN
TL064MJ	TL064MJ
TL064VD	TL064ID
TL064VN	TL064IN
TL071ACD	TL071ACD
TL071ACP	TL071ACN
TL071CD	TL071CD
TL071CJG	TL071CJ
TL071CP	TL071CN
TL072ACD	TL072ACD
TL072ACP	TL072ACN
TL072CD	TL072CD
TL072CJG	TL072CJ
TL072CP	TL072CN
TL074ACN	TL074ACN
TL074CN	TL074CN
TL074CJ	TL074CJ
TL081ACD	TL081ACD
TL081ACP	TL081ACN
TL081CD	TL081CD
TL081CJ	TL081CJ
TL081CP	TL081CN
TL081MJ	TL081MJ
TL082ACD	TL082ACD
TL082ACP	TL082ACN
TL082CD	TL082CD
TL082CJ	TL082CJ
TL082CP	TL082CN
TL082MJ	TL082MJ
TL084ACN	TL084ACN
TL084CN	TL084CN
TL084CJ	TL084CN
TL084MJ	TL084MJ
NATIONAL	
LF255M	LF255D
LF255N	LF255N
LF256M	LF256D
LF256N	LF256N
LF257M	LF257D
LF257N	LF257N
LF347J	LF347J
LF347M	LF347D
LF347N	LF347N
LF351M	LF351D
LF351N	LF351N
LF353M	LF353D
LF353N	LF353N
LF355M	LF355D
LF355N	LF355N
LF356M	LF356D
LF356N	LF356N
LF357M	LF357D
LF357N	LF357N
LM101AM	LM101AD
LM119J	LM119J
LM124AJ	LM124AJ
LM124J	LM124J
LM139AJ	LM139AJ
LM139J	LM139J
LM1458J	MC1458J
LM1458M	MC1458D
LM1458N	MC1458N

INDUSTRY STANDARD	NEAREST SGS-THOMSON TYPE
NATIONAL (cont'd)	
LM146J	LM146J
LM148J	LM148J
LM1558J	MC1558J
LM158AJ	LM158AJ
LM158J	LM158J
LM193AJ	LM193AJ
LM193J	LM193J
LM201AM	LM201AD
LM201AN	LM201AN
LM219J	LM219J
LM224AJ	LM224AJ
LM224J	LM224J
LM239AJ	LM239AJ
LM239J	LM239J
LM246J	LM246J
LM248J	LM248J
LM2901J	LM2901J
LM2901M	LM2901D
LM2901N	LM2901N
LM2902J	LM2902J
LM2902M	LM2902D
LM2902N	LM2902N
LM2903M	LM2903D
LM2903N	LM2903N
LM2904J	LM2904J
LM2904M	LM2904D
LM2904N	LM2904N
LM293AJ	LM293AJ
LM293J	LM293J
LM293N	LM293N
LM301AJ	LM301AJ
LM301AM	LM301AD
LM301AN	LM301AN
LM308AJ-8	LM308AJ
LM308AM	LM308AD
LM308AN	LM308AN
LM308J-8	LM308J
LM308M	LM308D
LM308N	LM308N
LM311J-8	LM311J
LM311M	LM311D
LM311N	LM311N
LM318M	LM318D
LM318N	LM318N
LM319J	LM319J
LM319M	LM319D
LM319N	LM319N
LM324AJ	LM324AJ
LM324AM	LM324AD
LM324AN	LM324AN
LM324J	LM324J
LM324M	LM324D
LM324N	LM324N
LM3302J	LM239J
LM3302N	LM239N
LM3303N	MC3303N
LM334M	LM334D
LM334Z	LM334Z
LM335AM	LM335AD
LM335AZ	LM335AZ
LM335M	LM335D
LM335Z	LM335Z
LM336BM-2.5	LM336BD
LM336BZ-2.5	LM336BZ
LM336M-2.5	LM336D
LM336Z-2.5	LM336Z
LM339AJ	LM339AJ
LM339AM	LM339AD
LM339AN	LM339AN
LM339J	LM339J
LM339M	LM339D
LM339N	LM339N
LM3403J	MC3403J
LM3403M	MC3403D
LM3403N	MC3403N
LM346J	LM346J
LM346M	LM346D
LM346N	LM346N
LM348J	LM348J
LM348M	LM348D
LM348N	LM348N
LM3503J	MC3503J
LM358AM	LM358AD
LM358AN	LM358AN
LM358J	LM358J
LM358M	LM358D
LM358N	LM358N
LM393AJ	LM393AJ
LM393AN	LM393AN
LM393J	LM393J
LM393M	LM393D
LM393N	LM393N
LM555CJ	NE555J
LM555CM	NE555D
LM555CN	NE555N
LM555J	SE555J
LM556CJ	NE556J
LM556CM	NE556D
LM556CN	NE556N
LM556J	SE556J
LM741AH	UA741AH
LM741AJ	UA741AJ
LM741CH	UA741CH
LM741CJ	UA741CJ
LM741CM	UA741CD
LM741CN	UA741CN
LM741EH	UA741EH
LM741EN	UA741EN
LM741H	UA741MH
LM741J	UA741MJ
LM776CH	UA776CH
LM776CN	UA776CN
LM776M	UA776MH
LM833M	LM833D
LM833N	LM833N
LMC555CM	TS555CD
LMC555CN	TS555CN
LMC660AIM	TS27M4BID
LMC660AIN	TS27M4BIN
LMC660CM	TS27M4ACD
LMC660CN	TS27M4ACN
LMC662AIM	TS27M2BID
LMC662AIN	TS27M2BIN
LMC662CM	TS27M2ACD
LMC662CN	TS27M2ACN
LPC660AIM	TS27L4BID
LPC660AIN	TS27L4BIN
LPC660IM	TS27L4AID
LPC660IN	TS27L4AIN
LPC662AIM	TS27L2BID
LPC662AIN	TS27L2BIN

INDUSTRY STANDARD	NEAREST SGS-THOMSON TYPE
NATIONAL (cont'd)	
LPC662IM	TS27L2AID
LPC662IN	TS27L2AIN
OP07CP	OP07CN
OP07DP	OP07DN
TL081CP	TL081CN
TL082CP	TL082CN
NEC	
UPC1458C	MC1458N
UPC1458G	MC1458D
UPC1555C	NE555N
UPC1558C	MC1558N
UPC156D	LM208N
UPC157C	LM201AN
UPC159D	LM318N
UPC251C	MC1458IN
UPC251G	MC1458ID
UPC271C	LM211N
UPC271G	LM211D
UPC272C	LM219N
UPC272D	LM219J
UPC272G	LM219D
UPC301AC	LM301AN
UPC311C	LM311N
UPC319G	LM319D
UPC324C	LM324N
UPC324G	LM324D
UPC339C	LM339N
UPC339G	LM339D
UPC3403C	MC3403N
UPC3403G	MC3403D
UPC356C	LF356N
UPC357C	LF357N
UPC358C	LM358N
UPC358G	LM358D
UPC393C	LM393N
UPC451C	LM224N
UPC451D	LM224J
UPC452C	MC3303N
UPC452G	MC3303D
UPC4558G	MC4558CD
UPC4558N	MC4558CN
UPC4741C	LM348N
UPC4741G	LM348D
UPC741C	UA741CN
UPD555C	TS555CN
UPD555G2	TS555CD
UPD556C	TS556CN
UPD556G2	TS556CD
SAMSUNG	
KS555D	TS555ID
KS555HD	TS555CD
KS555HN	TS555CN
KS555N	TS555IN
KS556D	TS556CD
KS556N	TS556CN
SIEMENS	
TBA222	UA741H
TBA222B	UA741N
TBB741G	UA741CD
SIGNETICS	
ICM7555CD	TS555CD
ICM7555CN	TS555CN
ICM7555ID	TS555ID
ICM7555IN	TS555IN
LM111D	LM111D
LM119D	LM119D
LM119F	LM119J
LM124D	LM124D
LM124F	LM124J
LM124N	LM124N
LM139AD	LM139AD
LM139AF	LM139AJ
LM139D	LM139D
LM139F	LM139J
LM139N	LM139N
LM158F	LM158J
LM158N	LM158N
LM193AF	LM193AJ
LM193D	LM193D
LM193N	LM193N
LM211D	LM211D
LM211N	LM211N
LM219D	LM219D
LM219F	LM219J
LM224D	LM224D
LM224F	LM224J
LM224N	LM224N
LM239AD	LM239AD
LM239AF	LM239AJ
LM239AN	LM239AN
LM239D	LM239D
LM239F	LM239J
LM239N	LM239N
LM258F	LM258J
LM258N	LM258N
LM2901D	LM2901D
LM2901F	LM2901J
LM2901N	LM2901N
LM2903F	LM2903J
LM2903N	LM2903N
LM293AF	LM293AJ
LM293F	LM293J
LM293N	LM293N
LM311D	LM311D
LM311F	LM311J
LM311N	LM311N
LM319D	LM319D
LM319F	LM319J
LM324D	LM324D
LM324F	LM324J
LM324N	LM324N
LM339AD	LM339AD
LM339AF	LM339AJ
LM339AN	LM339AN
LM339D	LM339D
LM339F	LM339J
LM339N	LM339N
LM358D	LM358D
LM358F	LM358J
LM358N	LM358N
LM393AF	LM393AJ
LM393AN	LM393AN
LM393D	LM393D
LM393F	LM393J
LM393N	LM393N
MC1458D	MC1458D
MC1458FE	MC1458J
MC1458N	MC1458N
MC1558D	MC1558D
MC1558FE	MC1558J
MC1558N	MC1558N

INDUSTRY STANDARD	
SIGNETICS (cont'd)	
MC3302D	LM239D
MC3302F	LM239J
MC3302N	LM239N
MC3303D	MC3303D
MC3303F	MC3303J
MC3303N	MC3303N
MC3403CF	MC3403J
MC3403CN	MC3403N
MC3403D	MC3403D
MC3503F	MC3503J
NE4558D	MC4558CD
NE4558F	MC4558CJ
NE4558N	MC4558CN
NE532D	LM358D
NE532F	LM358J
NE532N	LM358N
NE555D	NE555D
NE555F	NE555J
NE555N	NE555N
NE556D	NE556D
NE556F	NE556J
NE556N	NE556N
SA1458D	MC1458ID
SA1458N	MC1458IN
SA4558D	MC4558ID
SA4558N	MC4558IN
SA532D	LM2904D
SA532FE	LM2904J
SA532N	LM2904N
SA534D	LM2902D
SA534F	LM2902J
SA534N	LM2902N
SA741CN	UA741IN
SE555F	SE555J
SE555F	SE556J
UA741CD	UA741CD
UA741CFE	UA741CJ
UA741CN	UA741CN
UA741FE	UA741MJ
UA741N	UA741MN
TEXAS	
LM124AJ	LM124AJ
LM124J	LM124J
LM139AJ	LM139AJ

INDUSTRY STANDARD	NEAREST SGS-THOMSON TYPE
LM139J	LM139J
LM148J	LM148J
LM158AJG	LM158AJ
LM158JG	LM158J
LM193AJG	LM193AJ
LM201AD	LM201AD
LM201AP	LM201AN
LM211D	LM211D
LM211P	LM211N
LM224AD	LM224AD
LM224AJ	LM224AJ
LM224AN	LM224AN
LM224D	LM224D
LM224J	LM224J
LM224N	LM224N
LM239AD	LM239AD
LM239AJ	LM239AJ
LM239AN	LM239AN
LM239D	LM239D
LM239J	LM239J
LM239N	LM239N
LM248D	LM248D
LM248J	LM248J
LM248N	LM248N
LM258AJG	LM258AJ
LM258D	LM258D
LM258JG	LM258J
LM258P	LM258N
LM2901D	LM2901D
LM2901J	LM2901J
LM2901N	LM2901N
LM2902D	LM2902D
LM2902J	LM2902J
LM2902N	LM2902N
LM2903D	LM2903D
LM2903JG	LM2903J
LM2903P	LM2903N
LM2904D	LM2904D
LM2904JG	LM2904J
LM2904P	LM2904N
LM293AJG	LM293AJ
LM293D	LM293D
LM293JG	LM293J
LM301AD	LM301AD

INDUSTRY STANDARD	NEAREST SGS-THOMSON TYPE
LM301AJG	LM301AJ
LM301AP	LM301AN
LM311D	LM311D
LM311JG	LM311J
LM311P	LM311N
LM318D	LM318D
LM318P	LM318N
LM324AD	LM324AD
LM324AJ	LM324AJ
LM324AN	LM324AN
LM324D	LM324D
LM324J	LM324J
LM324N	LM324N
LM3302D	LM239D
LM3302J	LM239J
LM3302N	LM239N
LM339AD	LM339AD
LM339AJ	LM339AJ
LM339AN	LM339AN
LM339D	LM339D
LM339J	LM339J
LM339N	LM339N
LM348D	LM348D
LM348J	LM348J
LM348N	LM348N
LM358AD	LM358AD
LM358AJG	LM358AJ
LM358AP	LM358AN
LM358D	LM358D
LM358JG	LM358J
LM358P	LM358N
LM393AD	LM393AD
LM393AJG	LM393AJ
LM393AP	LM393AN
LM393D	LM393D
LM393JG	LM393J
LM393P	LM293N
LM393P	LM393N
MC1458D	MC1458D
MC1458JG	MC1458J
MC1458P	MC1458N
MC1558JG	MC1558J
MC3303D	MC3303D
MC3303J	MC3303J

INDUSTRY STANDARD	NEAREST SGS-THOMSON TYPE
TEXAS (cont'd)	
MC3303N	MC3303N
MC3403D	MC3403D
MC3403J	MC3403J
MC3403N	MC3403N
MC3503J	MC3503J
NE555D	NE555D
NE555JG	NE555J
NE555P	NE555N
NE556D	NE556D
NE556J	NE556J
NE556N	NE556N
OP07CP	OP07CN
OP07DP	OP07DN
RC4558D	MC4558CD
RC4558JG	MC4558CJ
RC4558P	MC4558CN
RV4558D	MC4558ID
RV4558P	MC4558IN
SA555D	SA555D
SA555JG	SA555J
SA555P	SA555N
SA556D	SA556D
SA556J	SA556J
SA556N	SA556N
SE555JG	SE555J
SE556J	SE556J
TL061ACD	TL061ACD
TL061ACP	TL061ACN
TL061BCD	TL061BCD
TL061BCP	TL061BCN
TL061CD	TL061CD
TL061CP	TL061CN
TL061ID	TL061ID
TL061IP	TL061IN
TL062ACP	TL062ACN
TL062ACPD	TL062ACD
TL062BCD	TL062BCD
TL062BCP	TL062BCN
TL062CD	TL062CD
TL062CP	TL062CN
TL062ID	TL062ID
TL062IP	TL062IN
TL064ACD	TL064ACD
TL064ACN	TL064ACN
TL064BCD	TL064BCD
TL064BCN	TL064BCN
TL064CD	TL064CD
TL064CJ	TL064CJ
TL064CN	TL064CN
TL064ID	TL064ID
TL064IJ	TL064IJ
TL064IN	TL064IN
TL071ACD	TL071ACD
TL071ACP	TL071ACN
TL071BCD	TL071BCD
TL071BCP	TL071BCN
TL071CD	TL071CD
TL071CP	TL071CN
TL071ID	TL071ID
TL071IP	TL071IN
TL072ACD	TL072ACD
TL072ACP	TL072ACN
TL072BCD	TL072BCD
TL072BCP	TL072BCN
TL072CD	TL072CD
TL072CP	TL072CN
TL072ID	TL072ID
TL072IP	TL072IN
TL074ACD	TL074ACD
TL074ACN	TL074ACN
TL074BCD	TL074BCD
TL074BCN	TL074BCN
TL074CD	TL074CD
TL074CJ	TL074CJ
TL074CN	TL074CN
TL074ID	TL074ID
TL074IN	TL074IN
TL081ACD	TL081ACD
TL081ACP	TL081ACN
TL081BCD	TL081BCD
TL081BCP	TL081BCN
TL081CD	TL081CD
TL081CP	TL081CN
TL081ID	TL081ID
TL081IP	TL081IN
TL082ACD	TL082ACD
TL082BCD	TL082BCD
TL082BCP	TL082BCN
TL082CD	TL082CD
TL082CP	TL082CN
TL082ID	TL082ID
TL082IP	TL082IN
TL084ACD	TL084ACD
TL084ACJ	TL084ACJ
TL084ACN	TL084ACN
TL084BCD	TL084BCD
TL084BCJ	TL084BCJ
TL084BCN	TL084BCN
TL084CD	TL084CD
TL084CJ	TL084CJ
TL084CN	TL084CN
TL084ID	TL084ID
TL084IJ	TL084IJ
TL084IN	TL084IN
TL084MJ	TL084MJ
TLC271ACD	TS271ACD
TLC271ACP	TS271ACN
TLC271AID	TS271AID
TLC271AIP	TS271AIN
TLC271BCD	TS271BCD
TLC271BCP	TS271BCN
TLC271BID	TS271BID
TLC271BIP	TS271BIN
TLC271CD	TS271CD
TLC271CP	TS271CN
TLC271ID	TS271ID
TLC271IP	TS271IN
TLC272ACD	TS272ACD
TLC272ACP	TS272ACN
TLC272AID	TS272AID
TLC272AIP	TS272AIN
TLC272BCD	TS272BCD
TLC272BCP	TS272BCN
TLC272BID	TS272BID
TLC272BIP	TS272BIN
TLC272CD	TS272CD
TLC272CP	TS272CN
TLC272ID	TS272ID
TLC272IP	TS272IN
TLC274ACD	TS274ACD
TLC274ACN	TS274ACN

INDUSTRY STANDARD	NEAREST SGS-THOMSON TYPE
TEXAS (cont'd)	
TLC274AID	TS274AID
TLC274AIP	TS274AIN
TLC274BCD	TS274BCD
TLC274BCN	TS274BCN
TLC274BID	TS274BID
TLC274BIP	TS274BIN
TLC274CD	TS274CD
TLC274CN	TS274CN
TLC274ID	TS274ID
TLC274IN	TS274IN
TLC27L2ACD	TS27L2ACD
TLC27L2ACP	TS27L2ACN
TLC27L2AID	TS27L2AID
TLC27L2AIP	TS27L2AIN
TLC27L2BCD	TS27L2BCD
TLC27L2BCP	TS27L2BCN
TLC27L2BID	TS27L2BID
TLC27L2BIP	TS27L2BIN
TLC27L2CD	TS27L2CD
TLC27L2CP	TS27L2CN
TLC27L2ID	TS27L2ID
TLC27L2IP	TS27L2IN
TLC27L4ACD	TS27L4ACD
TLC27L4ACN	TS27L4ACN
TLC27L4AID	TS27L4AID
TLC27L4AIN	TS27L4AIN
TLC27L4BCD	TS27L4BCD
TLC27L4BCN	TS27L4BCN
TLC27L4BID	TS27L4BID
TLC27L4BIN	TS27L4BIN
TLC27L4CD	TS27L4CD
TLC27L4CN	TS27L4CN
TLC27L4ID	TS27L4ID
TLC27L4IN	TS27L4IN
TLC27M2ACD	TS27M2ACD
TLC27M2ACP	TS27M2ACN
TLC27M2AID	TS27M2AID
TLC27M2AIP	TS27M2AIN
TLC27M2BCD	TS27M2BCD
TLC27M2BCP	TS27M2BCN
TLC27M2BID	TS27M2BID
TLC27M2BIP	TS27M2BIN
TLC27M2CD	TS27M2CD

INDUSTRY STANDARD	NEAREST SGS-THOMSON TYPE
TLC27M2CP	TS27M2CN
TLC27M2ID	TS27M2ID
TLC27M2IP	TS27M2IN
TLC27M4ACD	TS27M4ACD
TLC27M4ACN	TS27M4ACN
TLC27M4AID	TS27M4AID
TLC27M4AIN	TS27M4AIN
TLC27M4BCD	TS27M4BCD
TLC27M4BCN	TS27M4BCN
TLC27M4BID	TS27M4BID
TLC27M4BIN	TS27M4BIN
TLC27M4CD	TS27M4CD
TLC27M4CN	TS27M4CN
TLC27M4ID	TS27M4ID
TLC27M4IN	TS27M4IN
TLC339CD	TS339CD
TLC339CN	TS339CN
TLC339ID	TS339ID
TLC339IN	TS339IN
TLC3702CD	TS3702CD
TLC3702CP	TS3702CN
TLC3702ID	TS3702ID
TLC3702IP	TS3702IN
TLC3704CD	TS3704CD
TLC3704CN	TS3704CN
TLC3704ID	TS3704ID
TLC3704IN	TS3704IN
TLC372CD	TS372CD
TLC372CP	TS372CN
TLC372ID	TS372ID
TLC372IP	TS372IN
TLC374CD	TS374CD
TLC374CN	TS374CN
TLC374ID	TS374ID
TLC374IN	TS374IN
TLC393CD	TS393CD
TLC393CP	TS393CN
TLC393ID	TS393ID
TLC393IP	TS393IN
TLC555CD	TS555CD
TLC555CP	TS555CN
TLC555ID	TS555ID
TLC555IP	TS555IN
TLC556CD	TS556CD

INDUSTRY STANDARD	NEAREST SGS-THOMSON TYPE
TLC556CN	TS556CN
TLC556ID	TS556ID
TLC556IN	TS556IN
UA741CD	UA741CD
UA741CJG	UA741CJ
UA741CP	UA741CN
UA741MJG	UA741J
UA748CD	UA748CD
UA748CJG	UA748CJ
UA748CP	UA748CN
UA748MJG	UA748J
TOSHIBA	
TA7504P	UA741CN
TA75061P	TL061CN
TA75062F	TL062CD
TA75062P	TL062CN
TA75064F	TL064CD
TA75064P	TL064IN
TA75064P	TL064CN
TA7506P	LM301AN
TA75071F	TL071CD
TA75071P	TL071CN
TA75072F	TL072CD
TA75072P	TL072CN
TA75074F	TL074CD
TA75074P	TL074CN
TA75339F	LM2901D
TA75339P	LM2901N
TA75358CF	LM358D
TA75358CP	LM358N
TA75358F	LM2904D
TA75358P	LM2904N
TA75393F	LM2903D
TA75393P	LM2903N
TA7540P	UA776IN
TA75458F	MC1458D
TA75558F	MC4558CD
TA75558P	MC4558CN
TA7555F	NE555D
TA7555P	NE555N
TA75902F	LM2902D
TA75902P	LM2902N

TAPE AND REEL SPECIFICATION

TAPE AND REEL PACKING SPECIFICATION FOR SOIC

1 - PURPOSE :

This specification is formulated to provide dimensions, tolerances and characteristics about tape and reel necessary to surface mount components such that they may be automatically placed. This specification covers taping for active surface mount components in SOIC package type.

2 - REFERENCE DOCUMENTS

2 - 1 . "EIA 481-A"

2 - 2 . "IEC 286-3"

2 - 3 . "Special customer request"

3 - GENERAL

3 - 1 . Reel material = Plastic antistatic or conductive

3 - 2 . Cavity tape material = Black conductive (less than $10^5\Omega$ per square)

3 - 3 . Cover tape material = Transparent antistatic (less than $10^{10}\Omega$ per square) or conductive (less than $10^5\Omega$ per square)

4 - QUANTITY AND DIMENSIONS

All drawings dimensions are in millimeters.

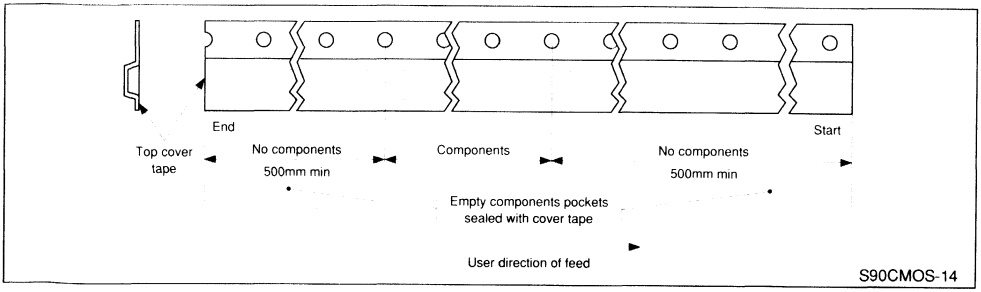
4.1 - QUANTITY AND DIMENSIONS - See table 1

Table 1.

PACKAGE	TAPE WIDTH (mm)	QTY / REEL
SO8	12	2500
SO14	16	2500
SO16 (narrow)	16	2500

4.2 - LEADER AND TRAINER

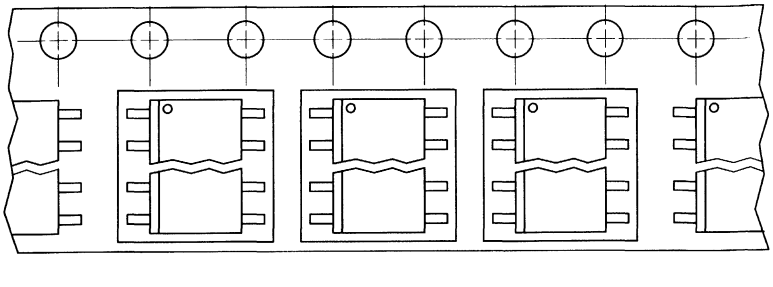
Figure 1.



The trailer end of the tape carrier is secured to the reel.
The devices are oriented with the terminals facing to the bottom of the carrier pocket.

4.3 - DEVICES ORIENTATION

Figure 2.

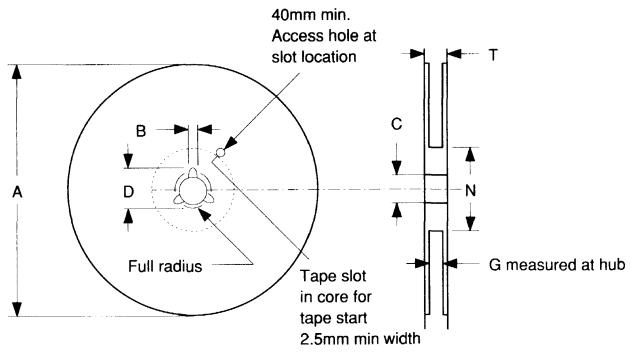


S90CMOS-15

The devices are oriented in the carrier pocket with pin number 1 adjacent to the sprocket holes.

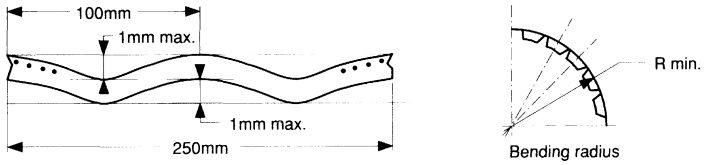
4.4 - OVERALL REEL DIMENSIONS

Figure 3.



S90CMOS-16

Figure 4.



Camber (top view)
Allowable camber to be 1mm / 100mm nonaccumulative over 250mm

S90CMOS-17

4.4 - OVERALL REEL DIMENSIONS (continued)

Table 2.

Tape Size	A max	B min	C	D min	N min	G	T max	R min
12 mm	330	1.5	13 ± 0.2	20.2	50	12.4 +2/-0	18.4	30
16 mm	330	1.5	13 ± 0.2	20.2	50	12.4 +2/-0	22.4	40

4.5 - CARRIER POCKET DIMENSIONS

Figure 5.

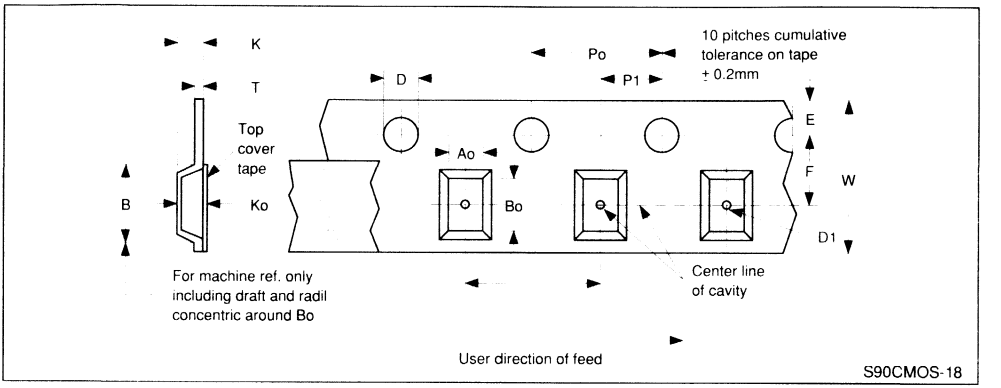


Table 3.

Tape Size	D	E	P_O	T	A_O	B_O	K_O
12 / 16mm	1.5 +0.1/0	1.75 ± 0.1	4 ± 0.1	0.4	See note		

Table 4.

Tape Size	B_1 max	D_1 min	F	K max	P_1	W
12mm	8.2	1.5	5.5 ± 0.05	4.5	2 ± 0.05	12 ± 0.3
16mm	12.1	1.5	7.5 ± 0.1	6.5	2 ± 0.1	16 ± 0.3

Note : Ao, Bo and Ko are determined by components size. The clearance between the component and the carrier pocket is :

a - 0.05 mm minimum to 0.65 mm maximum for 12 mm tape

b - 0.05 mm minimum to 0.90 mm maximum for 16 mm tape

DATASHEETS

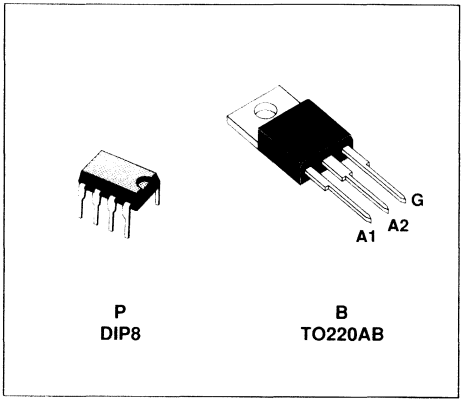
AUTOMATIC VOLTAGE SWITCH (SMPS < 200W)

CONTROLLER

- 50/60Hz FULL COMPATIBILITY
- INTEGRATED VOLTAGE REGULATOR
- TRIGGERING PULSE TRAIN OF THE TRIAC
- PARASITIC FILTER
- LOW POWER CONSUMPTION

TRIAC

- HIGH EFFICIENCY AND SAFETY SWITCHING
- UNINSULATED PACKAGE : AVS08CB
- INSULATED PACKAGE 2500V(RMS) : AVS08CBI
- $V_{DRM} = \pm 500$ V
- $I_{T(RMS)}$: 5A

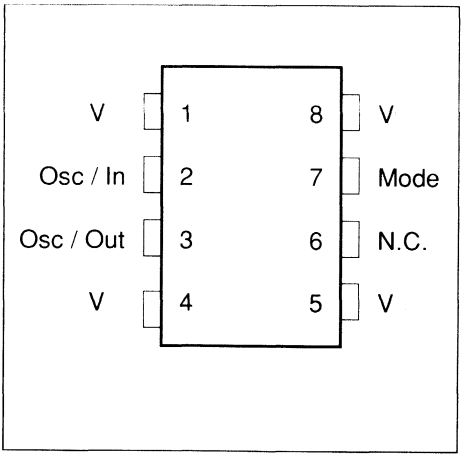


DESCRIPTION

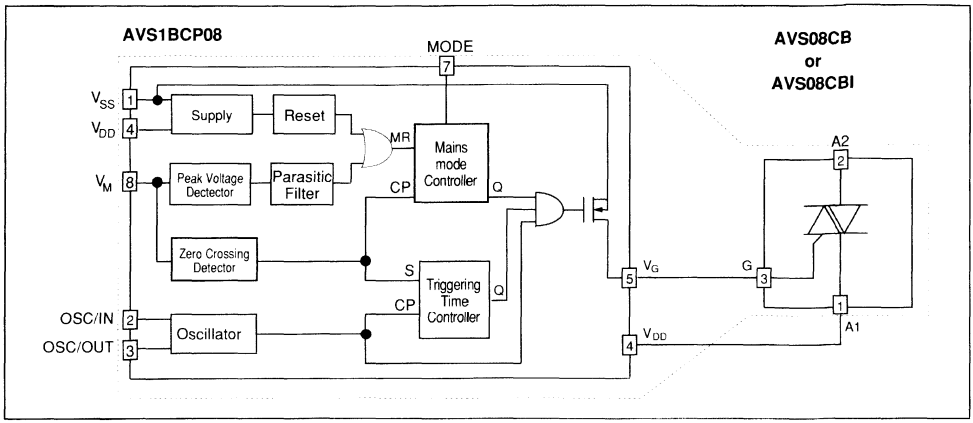
The AVS08 kit is an automatic mains selector (110/220V AC) to be used in SMPS < 200 W. It is composed of 2 devices :

- The **Controller** is optimized for low consumption and high security triggering of the triac. When connected to V_{SS}, the **mode** input activates an additional **option**. If the main power drops from 220V to 110V, the triac control remains locked to the 220V mode and avoids any high voltage spike when the voltage is restored to 220V.
  When connected to V_{DD}, the **mode** input desactivates this **option**.
- The TRIAC is specially designed for this application. An optimization between sensitivity and dynamic parameters of the triac gate highly reduces the losses of supply resistor and allows excellent immunity against disturbances.

PIN CONNECTION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

CONTROLLER AVS1BCP08

Symbol	Parameter	Value		Unit
		Min.	Max.	
V_{SS}	Supply voltage	- 12	0.5	V
V_I / V_O	I / O voltage	V_{SS} - 0.5	0.5	V
I_I / I_O	I / O current	- 40	+ 40	mA
T_{stg}	Storage Temperature	- 60	+ 150	°C
T_{oper}	Operating Temperature code " C " " T "	0 - 40	+ 70 + 105	°C

TRIAC AVS08CB / AVS08CBI T_j = +25°C (unless otherwise specified)

Symbol	Parameter			Value	Unit
V_{DRM}	Repetitive peak off-state voltage (2)			± 500	V
$I_{T(RMS)}$	RMS on-state current (360° conduction angle)	AVS08CB	T_C = 100°C	5	A
		AVS08CBI	T_C = 95°C		
I_{TSM}	Non repetitive surge peak on-state current (T_j initial = 25°C)		t = 8.3ms t = 10ms	70 65	A
I^2t	I^2t value		t = 10ms	21	A^2s
dI/dt	Critical rate of rise of on-state current (1)		Repetitive F = 50Hz	20	A/µs
			Non Repetitive	100	
T_{stg} T_j	Storage Temperature Junction Temperature Range			- 40 + 125 - 10 + 125	°C

(1) Gate supply : I_G = 100mA – di/dt = 1A/µs
(2) T_j = 125°C

THERMAL RESISTANCES

TRIAC AVS08CB / AVS08CBI

Symbol	Parameter		Value	Unit
Rth (j-a)	Junction-to-ambient		60	°C/W
Rth (j-c) DC	Junction-to-case for DC	AVS08CB	5.4	°C/W
		AVS08CBI	6.3	
Rth (j-c) AC	Junction-to-case for 360° conduction angle (F = 50Hz)	AVS08CB	4.0	°C/W
		AVS08CBI	4.7	

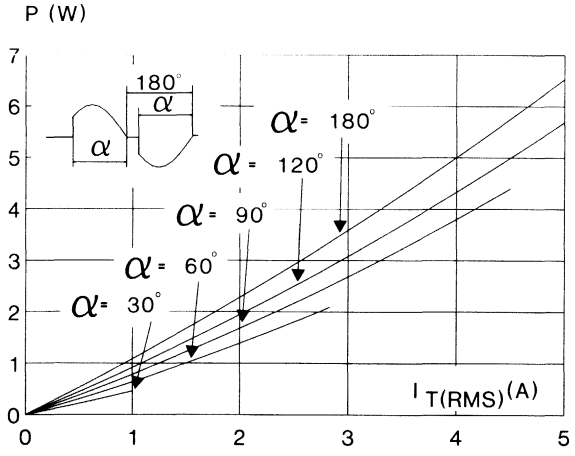
DC GENERAL ELECTRICAL CHARACTERISTICS

TRIAC AVS08CB / AVS08CBI

Symbol	Parameter		Value		Unit
			Min.	Max.	
V_{TM} *	I_{TM} = 7A t_p = 10ms	T_j = 25°C		1.65	V
I_{DRM} *	V_{DRM} rated Gate open	T_j = 25°C		10	µA

* For either polarity of electrode A2 voltage with reference to electrode A1.

Fig. 1 :Maximum RMS power dissipation versus RMS on-state current (F = 60Hz).
(Curves are cut off by (dI/dt)c limitation)



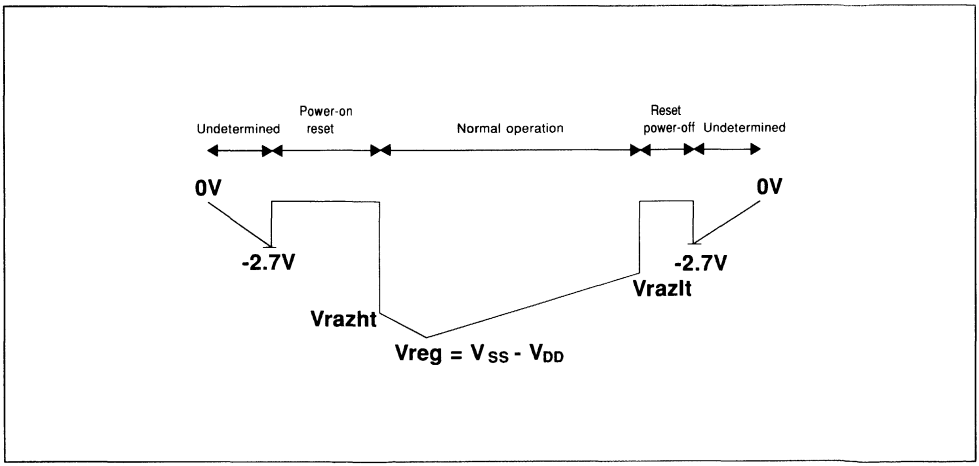
DC GENERAL ELECTRICAL CHARACTERISTICS (continued)

CONTROLLER AVS1BCP08 T_{oper} = 25°C (unless otherwise specified)

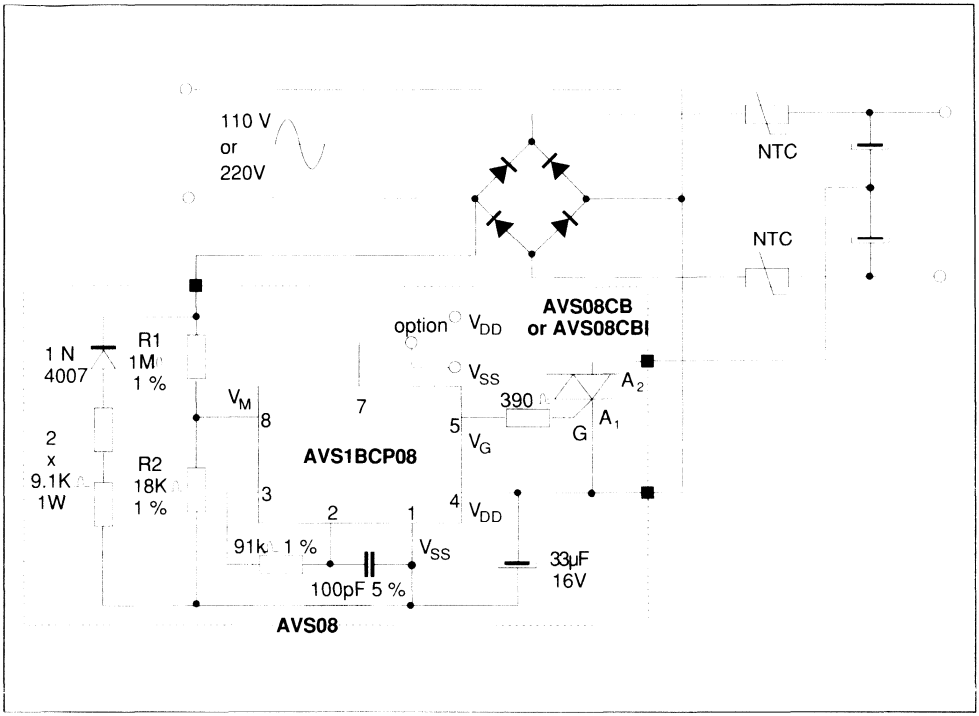
Symbol	Parameter	Value			Unit
		Min	Typ	Max	
V_{SS} (pin 1) (Vreg)	Shunt regulator	- 10	- 9	- 8	V
I_{SS} (pin 1) (Vreg) (@ V_{SS} = 9V)	Supply current	0.4		25	mA
I_{SS} (pin 1) (@ triac gate non connected)	Quiescent current			1	mA
F (pin 3) (@ R = 91kΩ) (C = 100pF)	Oscillator frequency	42	44	46	KHz
V_M (pin 8) Vth (3)	Peak voltage of detection high-threshold	4.08	4.25	4.42	V
V_M (pin 8) Vh (3)	Peak voltage of detection hysteresis	0.370	0.4	0.420	V
(1) V_M (pin 8) Vth (3)	Zero-crossing detection high-threshold	95	110	125	mV
V_M (pin 8) Vh (3)	Zero-crossing detection hysteresis	27	50	80	mV
(2) Vrazht (4)	Power-on-reset activation threshold		Vreg x 0.89		V
(2) Vrazlt (4)	Power-down-reset activation threshold	3		6.95	V
Mode (pin 7)	V_{IL} (4) V_{IH} (4)	0.7 Vreg		0.3 Vreg	V
V_G (pin 5)	V_{OL} (I_{VG} = 25mA) Leakage current (V_G = V_{DD})			1 + 50	V µA

NOTES :
(1) : This value gives a typical noise immunity on the zero-crossing detectionof 110mV x 1018/18 = 6.20V on the main supply
(2) : See following diagram
(3) : Voltage referred to VSS
(4) : Voltage referred to VDD

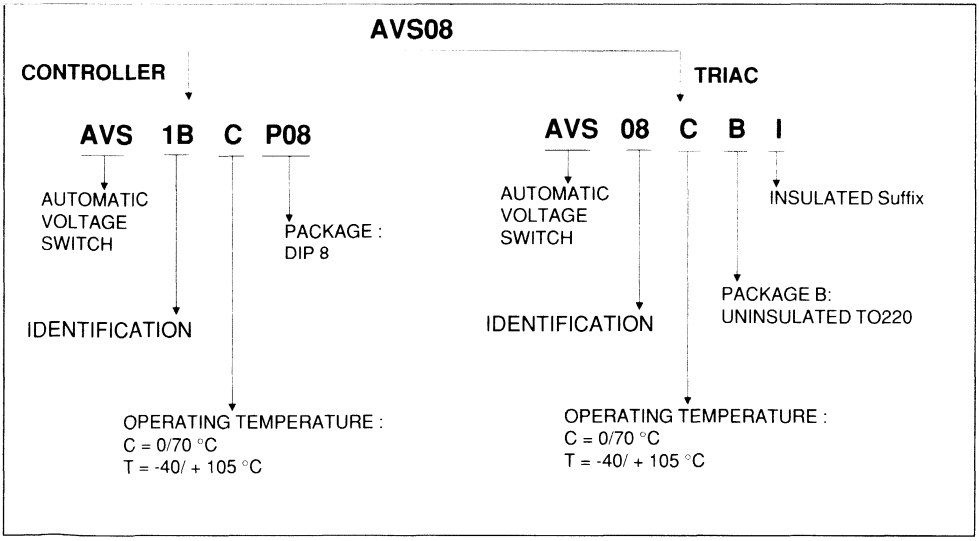
POWER-ON AND POWER-OFF RESET BEHAVIOUR



TYPICAL APPLICATION



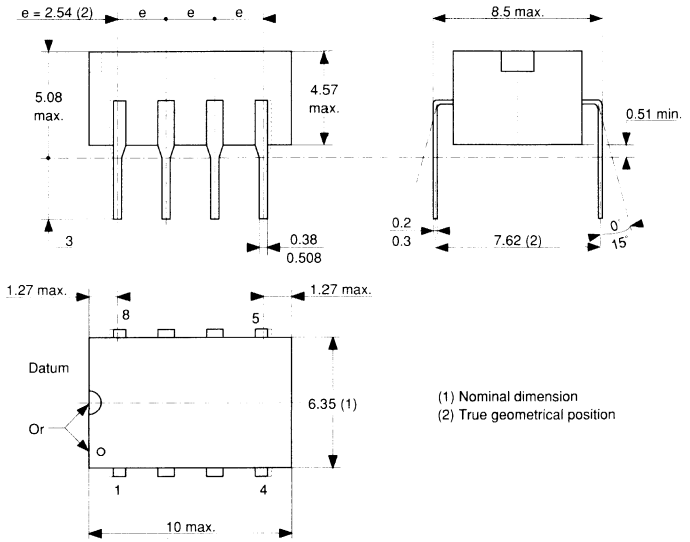
ORDERING INFORMATION



PACKAGE MECHANICAL DATA

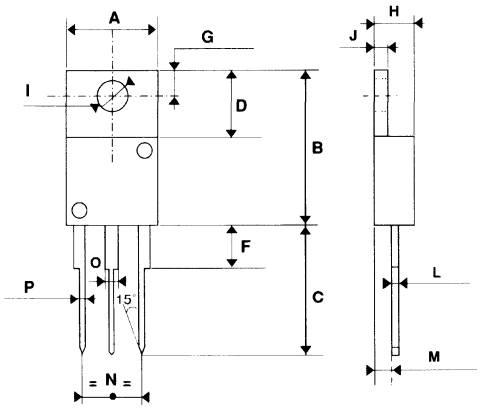
8 PINS - PLASTIC DIP

CONTROLLER



TO220AB (Plastic) (in millimeters)

TRIAC



REF.	DIMENSIONS			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	10.20	10.40	0.401	0.401
B	14.23	15.87	0.560	0.625
C	12.70	14.70	0.500	0.579
D	5.85	6.85	0.230	0.270
F		4.50		0.178
G	2.54	3.00	0.100	0.119
H	4.48	4.82	0.176	0.190
I	3.55	4.00	0.139	0.158
J	1.15	1.39	0.045	0.055
L	0.35	0.65	0.013	0.026
M	2.10	2.70	0.082	0.107
N	4.58	5.58	0.18	0.22
O	0.80	1.20	0.031	0.048
P	0.64	0.96	0.025	0.038

Cooling method : by conduction (method C)
Marking : Type number
Weight : 2.3 g
Polarity : N A
Stud torque : N A

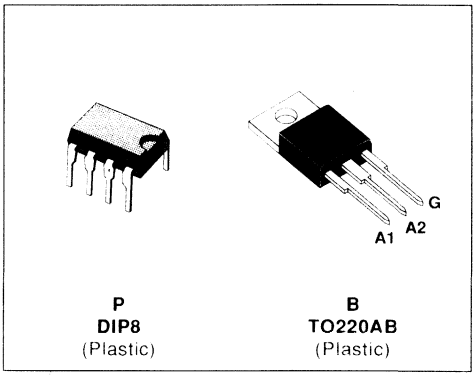
AUTOMATIC VOLTAGE SWITCH (SMPS < 300W)

CONTROLLER

- 50/60Hz FULL COMPATIBILITY
- INTEGRATED VOLTAGE REGULATOR
- TRIGGERING PULSE TRAIN OF THE TRIAC
- PARASITIC FILTER
- LOW POWER CONSUMPTION

TRIAC

- HIGH EFFICIENCY AND SAFETY SWITCHING
- UNINSULATED PACKAGE : AVS10CB
- INSULATED PACKAGE 2500$V_{(RMS)}$: AVS10CBI
- V_{DRM} = ± 600V
- $I_{T(RMS)}$: 8A



P
DIP8
(Plastic)

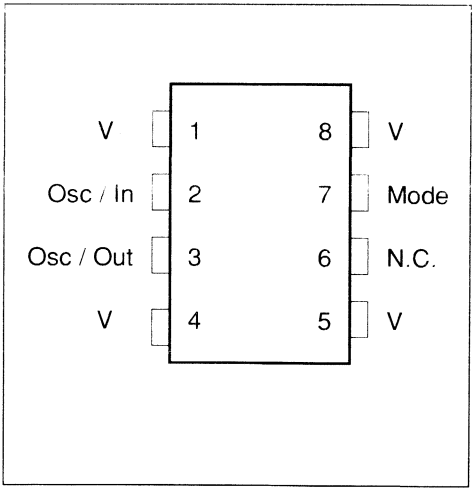
B
TO220AB
(Plastic)

DESCRIPTION

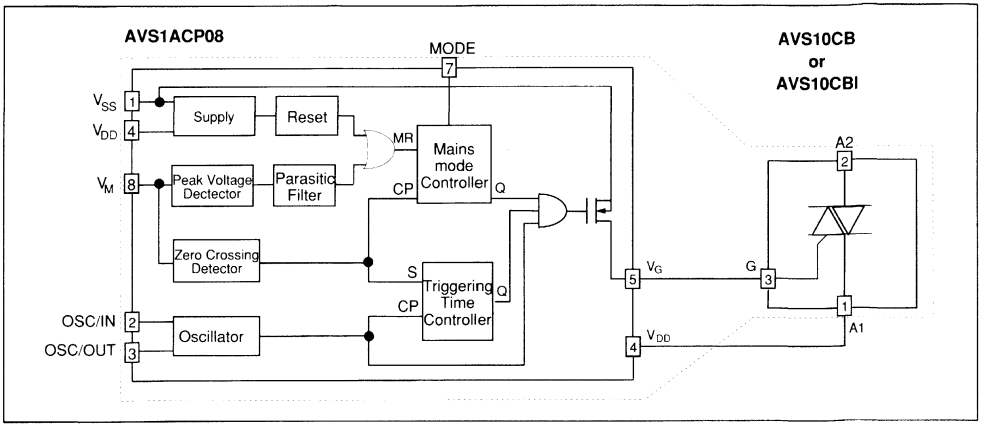
The AVS10 kit is an automatic mains selector (110/220V AC) to be used in SMPS < 300 W. It is composed of 2 devices :

- The **Controller** is optimized for low consumption and high security triggering of the triac. When connected to V_{SS}, the **mode** input activates an additional **option**. If the main power drops from 220V to 110V, the triac control remains locked to the 220V mode and avoids any high voltage spike when the voltage is restored to 220V.
  When connected to V_{DD}, the **mode** input desactivates this **option**.
- The TRIAC is specially designed for this application. An optimization between sensitivity and dynamic parameters of the triac gate highly reduces the losses of supply resistor and allows excellent immunity against disturbances.

PIN CONNECTION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

CONTROLLER AVS1ACP08

Symbol	Parameter	Value		Unit
		Min.	Max.	
V_{SS}	Supply voltage	- 12	0.5	V
V_I / V_O	I / O voltage	V_{SS} - 0.5	0.5	V
I_I / I_O	I / O current	- 40	+ 40	mA
T_{stg}	Storage Temperature	- 60	+ 150	°C
T_{oper}	Operating Temperature code " C "	0	+ 70	°C

TRIAC AVS10CB / AVS10CBI T_j = +25°C (unless otherwise specified)

Symbol	Parameter			Value	Unit
V_{DRM}	Repetitive peak off-state voltage (2)			± 600	V
$I_{T(RMS)}$	RMS on-state current (360° conduction angle)	AVS10CB	T_C = 80°C	8	A
		AVS10CBI	T_C = 70°C		
I_{TSM}	Non repetitive surge peak on-state current (T_j initial = 25°C)		t = 8.3ms t = 10ms	85 80	A
I^2t	I^2t value		t = 10ms	32	A^2s
dI/dt	Critical rate of rise of on-state current (1)		Repetitive F = 50Hz	20	A/µs
			Non Repetitive	100	
dv/dt *	Linear slope up to 0.67 V_{DRM} Gate open		T_j = 110°C	50	V/µs
T_{stg} T_j	Storage Temperature Operating Junction Temperature			- 40 + 150 0 + 110	°C

(1) Gate supply : IG = 100mA – di/dt = 1A/µs
(2) T_j = 110°C

* For either polarity of electrode A2 voltage with reference to electrode A1

THERMAL RESISTANCES

TRIAC AVS10CB / AVS10CBI

Symbol	Parameter		Value	Unit
Rth (j-a)	Junction-to-ambient		60	°C/W
Rth (j-c) DC	Junction-to-case for DC	AVS10CB	3.5	°C/W
		AVS10CBI	4.4	
Rth (j-c) AC	Junction-to-case for 360° conduction angle (F = 50Hz)	AVS10CB	2.6	°C/W
		AVS10CBI	3.3	

DC GENERAL ELECTRICAL CHARACTERISTICS

TRIAC AVS10CB / AVS10CBI

Symbol	Parameter		Value		Unit
			Min.	Max.	
V_{GD}	$V_D = V_{DRM}$ $R_L = 3.3k\Omega$ Pulse duration> 20µs	Tj = 110°C	0.2		V
V_{TM} *	$I_{TM} = 11A$ $t_p = 10ms$	Tj = 25°C		1.75	V
I_{DRM} *	V_{DRM} rated Gate open	Tj = 25°C		10	µA
		Tj = 110°C		500	

* For either polarity of electrode A2 voltage with reference to electrode A1.

Fig.1 :Maximum RMS power dissipation versus RMS on-state current (F = 60Hz).
(Curves are cut off by (dI/dt)c limitation)

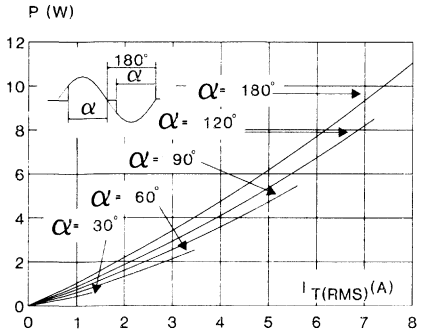


Fig. 2 :Correlation between maximum mean power dissipation and maximum allowable temperatures (Tamb and Tcase) for different thermal resistances heatsink + contact (AVS10CB).

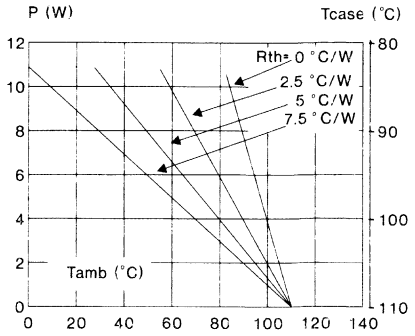


Fig. 3 :Correlation between maximum mean power dissipation and maximum allowable temperatures (Tamb and Tcase) for different thermal resistances heatsink + contact (AVS10CBI).

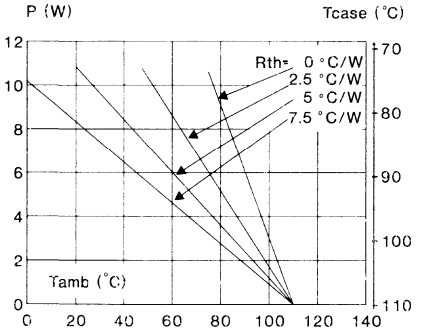


Fig. 4 :Non repetitive surge peak on-state current for a sinusoidal pulse with width : t ≤ 10ms, and corresponding value of I^2t.

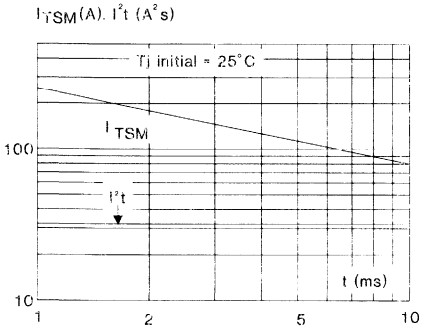
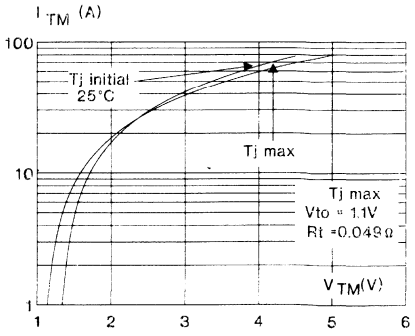


Fig. 5 :On-state characteristics (maximum values).



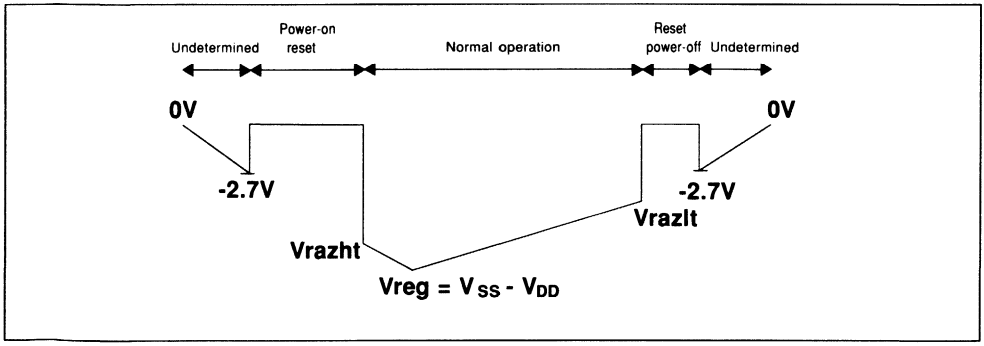
DC GENERAL ELECTRICAL CHARACTERISTICS (continued)

CONTROLLER AVS1ACP08 T_{oper} = 25°C (unless otherwise specified)

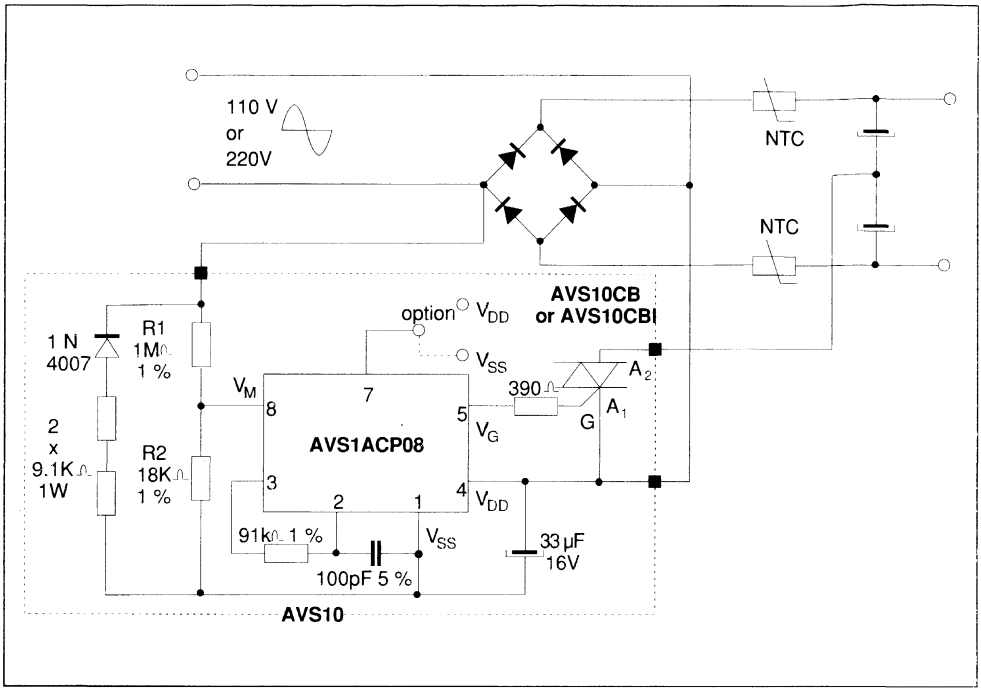
Symbol	Parameter	Value			Unit
		Min	Typ	Max	
V_{SS} (pin 1) (Vreg)	Shunt regulator	- 10	- 9	- 8	V
I_{SS} (pin 1) (Vreg) (@ V_{SS} = 9V)	Supply current	0.4		30	mA
I_{SS} (pin 1) (@ triac gate non connected)	Quiescent current			0.7	mA
f (pin 3) (@ R = 91kΩ) (C = 100pF)	Oscillator frequency	42	44	46	kHz
V_M (pin 8) Vth (3)	Peak voltage of detection high-threshold	4.08	4.25	4.42	V
V_M (pin 8) Vh (3)	Peak voltage of detection hysteresis	0.370	0.4	0.420	V
(1) V_M (pin 8) Vth (3)	Zero-crossing detection high-threshold	95	110	125	mV
V_M (pin 8) Vh (3)	Zero-crossing detection hysteresis	27	50	80	mV
(2) Vrazht (4)	Power-on-reset activation threshold		Vreg x 0.89		V
(2) Vrazlt (4)	Power-down-reset activation threshold	3		6.5	V
Mode (pin 7)	V_{IL} (4) V_{IH} (4)	0.7 Vreg		0.3 Vreg	V
V_G (pin 5)	V_{OL} (I_{VG} = 25mA) Leakage current (V_G = V_{DD})			650 + 10	mV µA

NOTES :
(1) : This value gives a typical noise immunity on the zero-crossing detectionof 110mV x 1018/18 = 6.20V on the main supply
(2) : See following diagram
(3) : Voltage referred to VSS
(4) : Voltage referred to VDD

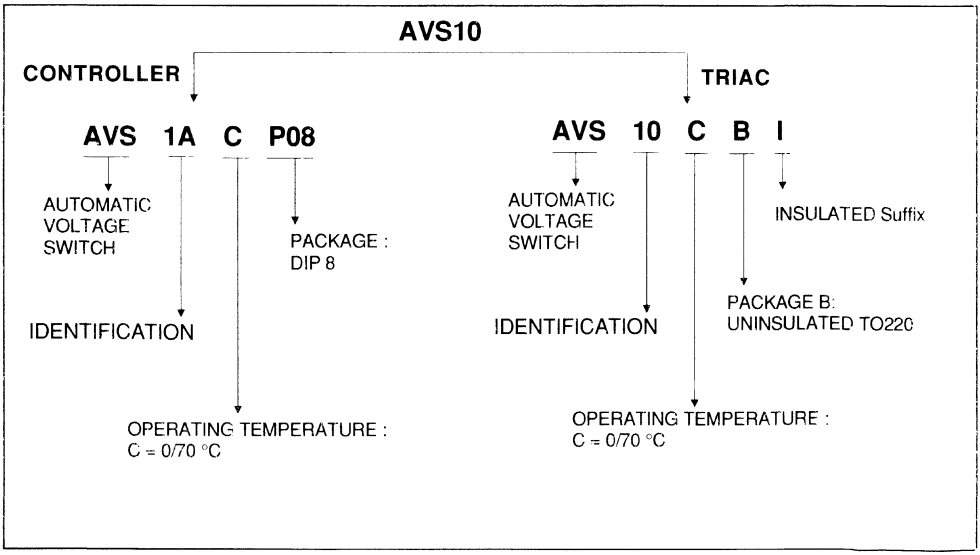
POWER-ON AND POWER-OFF RESET BEHAVIOUR



TYPICAL APPLICATION



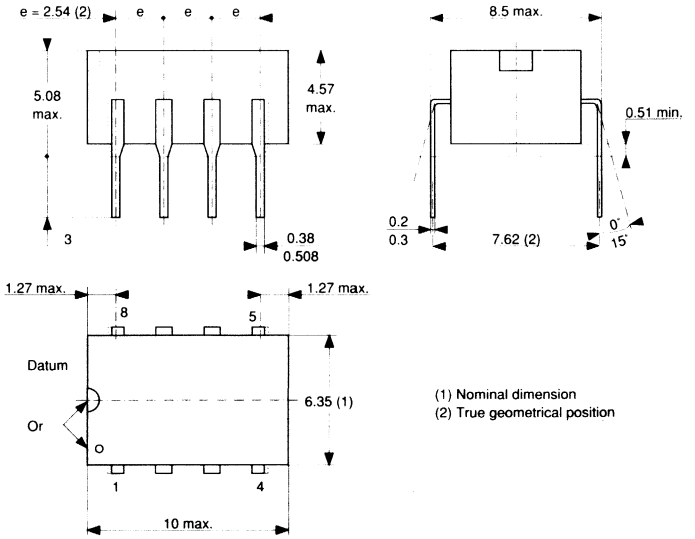
ORDERING INFORMATION



PACKAGE MECHANICAL DATA

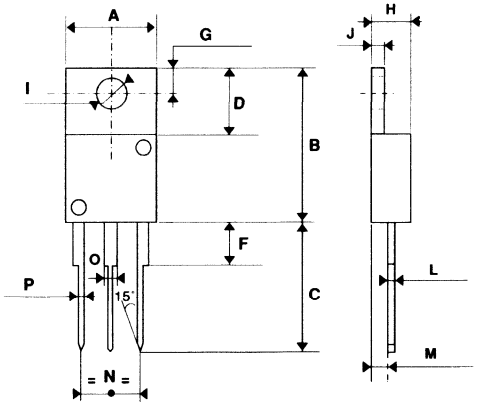
8 PINS - PLASTIC DIP

CONTROLLER



TO220AB (Plastic) (in millimeters)

TRIAC



REF.	DIMENSIONS			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	10.20	10.40	0.401	0.401
B	14.23	15.87	0.560	0.625
C	12.70	14.70	0.500	0.579
D	5.85	6.85	0.230	0.270
F		4.50		0.178
G	2.54	3.00	0.100	0.119
H	4.48	4.82	0.176	0.190
I	3.55	4.00	0.139	0.158
J	1.15	1.39	0.045	0.055
L	0.35	0.65	0.013	0.026
M	2.10	2.70	0.082	0.107
N	4.58	5.58	0.18	0.22
O	0.80	1.20	0.031	0.048
P	0.64	0.96	0.025	0.038

Cooling method : by conduction (method C)
Marking : Type number
Weight : 2.3 g
Polarity : N A
Stud torque : N A

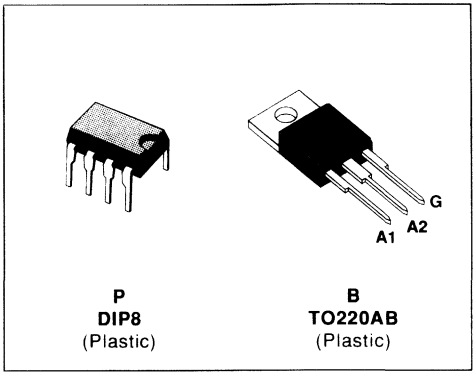
AUTOMATIC VOLTAGE SWITCH (SMPS < 500W)

CONTROLLER

- 50/60Hz FULL COMPATIBILITY
- INTEGRATED VOLTAGE REGULATOR
- TRIGGERING PULSE TRAIN OF THE TRIAC
- PARASITIC FILTER
- LOW POWER CONSUMPTION

TRIAC

- HIGH EFFICIENCY AND SAFETY SWITCHING
- UNINSULATED PACKAGE : AVS12CB
- V_{DRM} = ± 600V
- $I_{T(RMS)}$: 12A



P
DIP8
(Plastic)

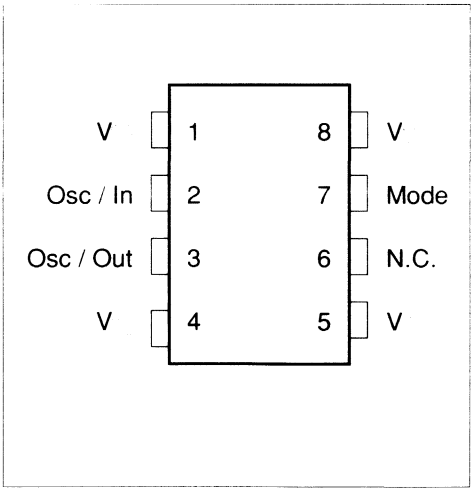
B
TO220AB
(Plastic)

DESCRIPTION

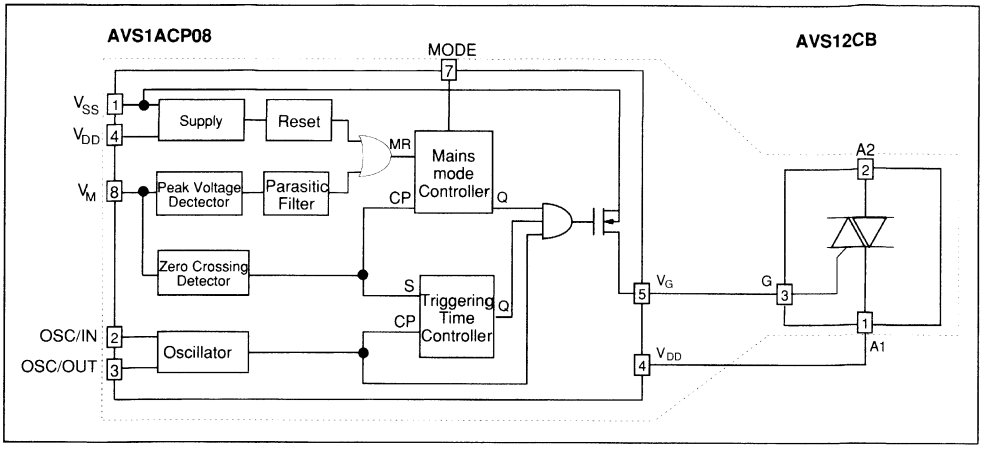
The AVS12 kit is an automatic mains selector (110/220V AC) to be used in SMPS < 500 W. It is composed of 2 devices :

- The **Controller** is optimized for low consumption and high security triggering of the triac. When connected to V_{SS}, the **mode** input activates an additional **option**. If the main power drops from 220V to 110V, the triac control remains locked to the 220V mode and avoids any high voltage spike when the voltage comes back to 220V.
  When connected to V_{DD}, the **mode** input desactivates this **option**.
- The TRIAC is specially designed for this application. An optimization between sensitivity and dynamic parameters of the triac gate highly reduces the losses of supply resistor and allows excellent immunity against disturbances.

PIN CONNECTION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

CONTROLLER AVS1ACP08

Symbol	Parameter	Value		Unit
		Min.	Max.	
V_{SS}	Supply voltage	- 12	0.5	V
V_I / V_O	I / O voltage	V_{SS} - 0.5	0.5	V
I_I / I_O	I / O current	- 40	+ 40	mA
T_{stg}	Storage Temperature	- 60	+ 150	°C
T_{oper}	Operating Temperature code " C "	0	+ 70	°C

TRIAC AVS12CB T_j = 25°C (unless otherwise specified)

Symbol	Parameter		Value	Unit
V_{DRM}	Repetitive peak off-state voltage (2)		± 600	V
$I_{T(RMS)}$	RMS on-state current (360° conduction angle)	T_C = 70°C	12	A
I_{TSM}	Non repetitive surge peak on-state current (T_j initial = 25°C)	t = 8.3ms t = 10ms	105 100	A
I^2t	I^2t value	t = 10ms	50	A^2s
dI/dt	Critical rate of rise of on-state current (1)	Repetitive F = 50Hz	20	A/µs
		Non Repetitive	100	
dv/dt *	Linear slope up to 0.67 V_{DRM} Gate open	T_j = 110°C	50	V/µs
T_{stg} T_j	Storage Temperature Operating Junction Temperature		- 40 + 150 0 + 110	°C

(1) Gate supply : I_G =100mA – di/dt = 1A/µs
(2) T_j = 110°C
* For either polarity of electrode A2 voltage with reference to electrode A1

THERMAL RESISTANCES

TRIAC AVS12CB

Symbol	Parameter	Value	Unit
Rth (j-a)	Junction-to-ambient	60	°C/W
Rth (j-c) DC	Junction-to-case for DC	3	°C/W
Rth (j-c) AC	Junction-to-case for 360° conduction angle (f= 50Hz)	2.3	°C/W

DC GENERAL ELECTRICAL CHARACTERISTICS

TRIAC AVS12CB

Symbol	Parameter		Value		Unit
			Min.	Max.	
V_{GD}	$V_D = V_{DRM}$ $R_L = 3.3k\Omega$ Pulse duration> 20µs	Tj = 110°C	0.2		V
V_{TM} *	I_{TM} = 17A tp = 10ms	Tj = 25°C		1.75	V
I_{DRM} *	V_{DRM} rated Gate open	Tj = 25°C		10	µA
		Tj = 110°C		500	

* For either polarity of electrode A2 voltage with reference to electrode A1.

Fig. 1 :Maximum RMS power dissipation versus RMS on-state current
(F = 60Hz).
(Curves are cut off by (dI/dt)c limitation)

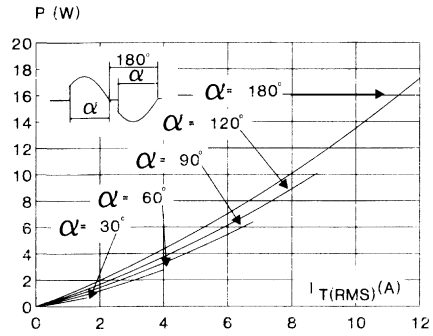


Fig. 2 :Correlation between maximum mean power dissipation and maximum allowable temperatures (Tamb and Tcase) for different thermal resistances heatsink + contact.

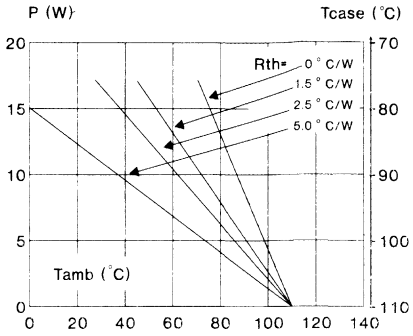


Fig. 3 :Non repetitive surge peak on state current for a sinusoidal pulse with width : t ≤ 10ms, and corresponding value of I^2t.

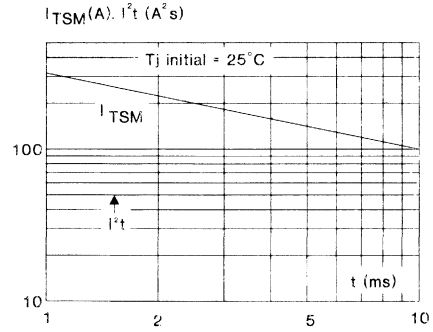
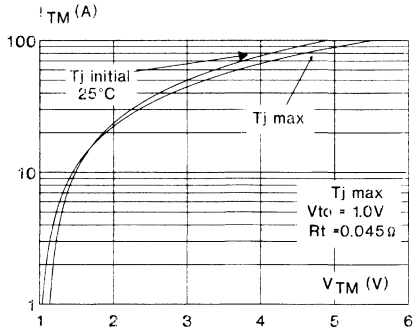


Fig. 4 :On-state characteristics (maximum values).



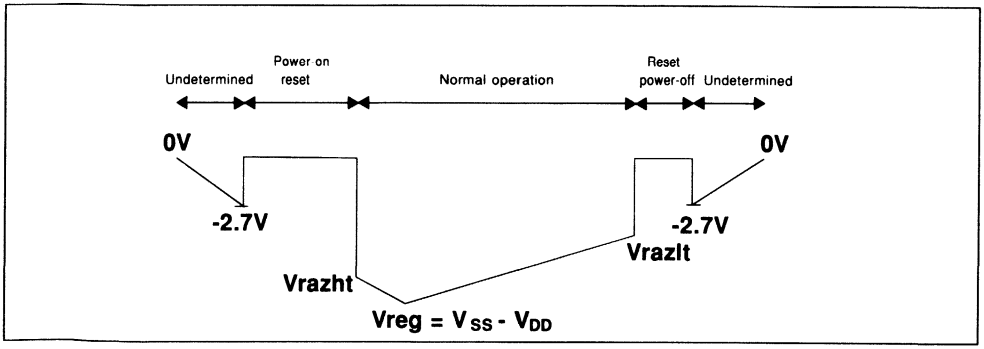
DC GENERAL ELECTRICAL CHARACTERISTICS (continued)

CONTROLLER AVS1ACP08 T_{oper} = 25°C (unless otherwise specified)

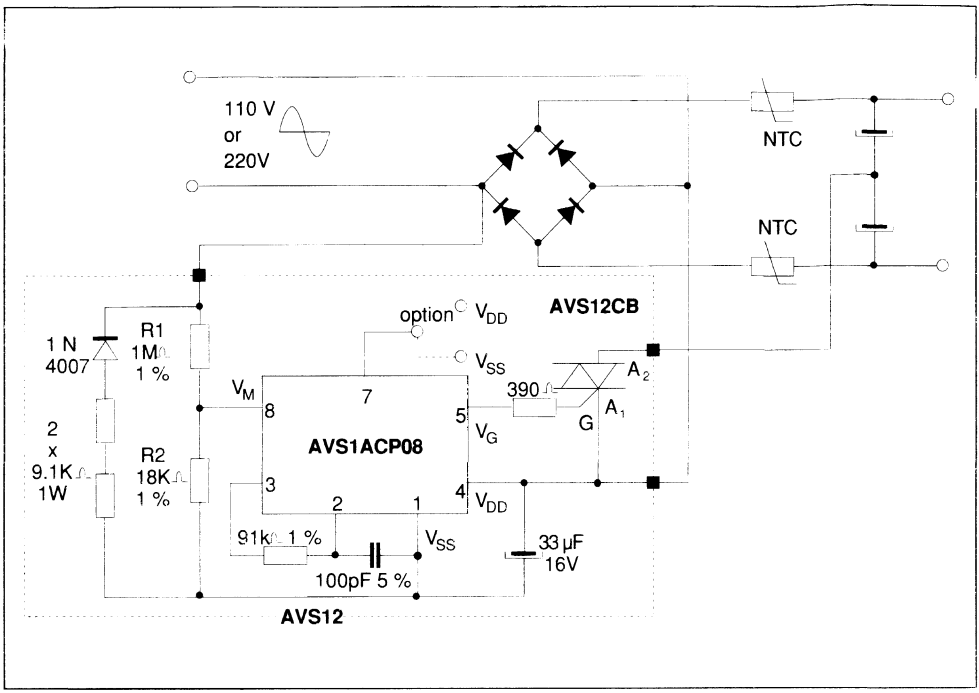
Symbol	Parameter	Value			Unit
		Min	Typ	Max	
V_{SS} (pin 1) (Vreg)	Shunt regulator	- 10	- 9	- 8	V
I_{SS} (pin 1) (Vreg) (@ V_{SS} = 9V)	Supply current	0.4		30	mA
I_{SS} (pin 1) (@ triac gate non connected)	Quiescent current			0.7	mA
f (pin 3) (@ R = 91kΩ) (C = 100pF)	Oscillator frequency	42	44	46	kHz
V_M (pin 8) Vth (3)	Peak voltage of detection high-threshold	4.08	4.25	4.42	V
V_M (pin 8) Vh (3)	Peak voltage of detection hysteresis	0.370	0.4	0.420	V
(1) V_M (pin 8) Vth (3)	Zero-crossing detection high-threshold	95	110	125	mV
V_M (pin 8) Vh (3)	Zero-crossing detection hysteresis	27	50	80	mV
(2) Vrazht (4)	Power-on-reset activation threshold		Vreg x 0.89		V
(2) Vrazlt (4)	Power-down-reset activation threshold	3		6.5	V
Mode (pin 7)	V_{IL} (4) V_{IH} (4)	0.7 Vreg		0.3 Vreg	V
V_G (pin 5)	V_{OL} (I_{VG} = 25mA) Leakage current (V_G = V_{DD})			650 + 10	mV µA

NOTES :
(1) : This value gives a typical noise immunity on the zero-crossing detection of 110mV x 1018/18 = 6.20V on the main supply
(2) : See following diagram
(3) : Voltage referred to VSS
(4) : Voltage referred to VDD

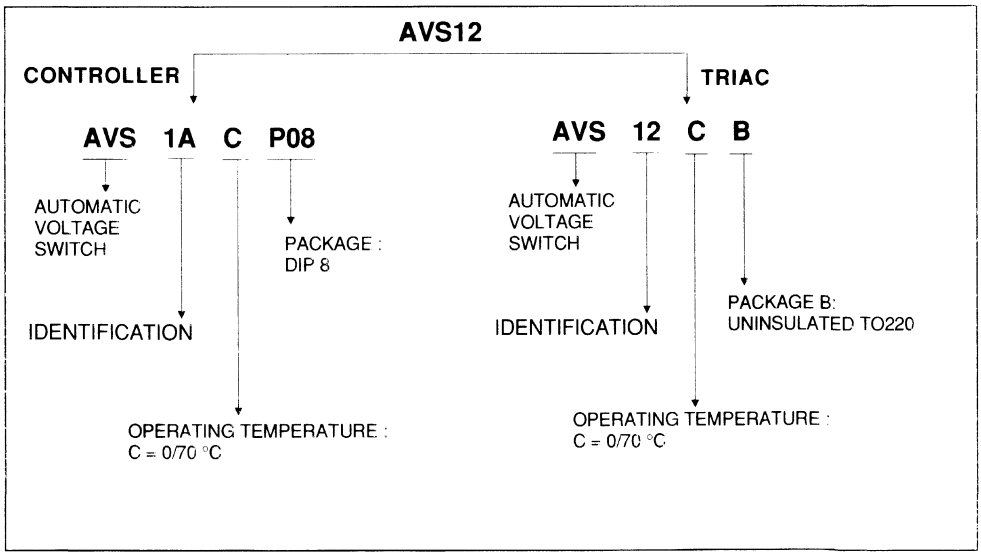
POWER-ON AND POWER-OFF RESET BEHAVIOUR



TYPICAL APPLICATION



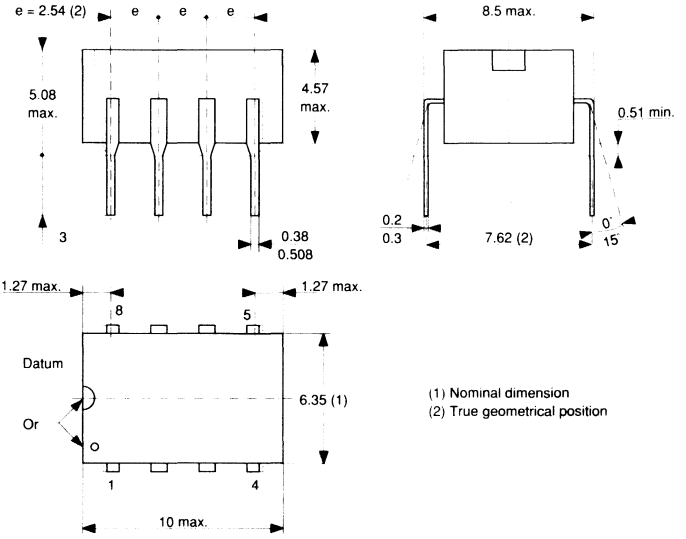
ORDERING INFORMATION



PACKAGE MECHANICAL DATA

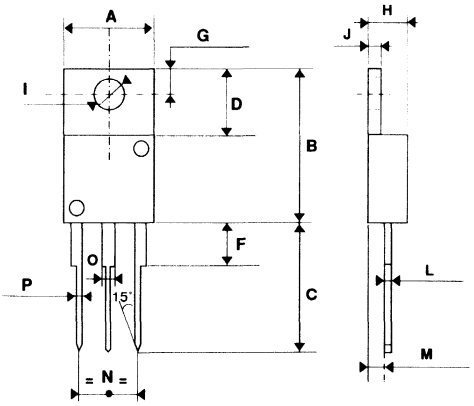
8 PINS - PLASTIC DIP

CONTROLLER



TO220AB (Plastic) (in millimeters)

TRIAC



REF.	DIMENSIONS			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	10.20	10.40	0.401	0.401
B	14.23	15.87	0.560	0.625
C	12.70	14.70	0.500	0.579
D	5.85	6.85	0.230	0.270
F		4.50		0.178
G	2.54	3.00	0.100	0.119
H	4.48	4.82	0.176	0.190
I	3.55	4.00	0.139	0.158
J	1.15	1.39	0.045	0.055
L	0.35	0.65	0.013	0.026
M	2.10	2.70	0.082	0.107
N	4.58	5.58	0.18	0.22
O	0.80	1.20	0.031	0.048
P	0.64	0.96	0.025	0.038

Cooling method : by conduction (method C)
Marking : Type number
Weight : 2.3 g
Polarity : N A
Stud torque : N A

AUTOMATIC VOLTAGE SWITCH (SMPS < 300W)

CONTROLLER

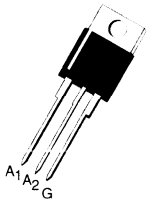
- 50/60Hz FULL COMPATIBILITY
- INTEGRATED VOLTAGE REGULATOR
- TRIAC TRIGGERING BY PULSE TRAIN
- HIGH IMMUNITY TO AC DISTURBANCES (SPIKES, MISSING CYCLE)
- HIGH RELIABILITY ON LINE VOLTAGE, DETECTION (PARASITIC FILTER ON SIGNAL INPUT)
- FAST DIGITAL START-UP TIME (< 2 LINE CYCLES)
- LOW POWER CONSUMPTION

TRIAC

- HIGH EFFICIENCY AND SAFETY SWITCHING
- UNINSULATED PACKAGE : AVS10CB/AVS100CB
- INSULATED PACKAGE (2500V_{RMS}) : AVS10CBI
- V_{DRM} = ±600V (AVS10CB), ±800V (AVS100CB)
- $I_{T(RMS)}$: 8A

P
DIP8
(Plastic Package)

ORDER CODE : AVS2ACP08



B
TO220AB
(Plastic Package)

ORDER CODES : AVS10CB-AVS10CBI-AVS100CB

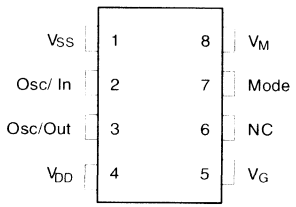
DESCRIPTION

The AVS20 (AVS200) kit is an automatic mains selector (120/230V AC) to be used in SMPS with input power < 300 W. It is composed of 2 devices :

- The **Controller** is optimized for low consumption and high security triggering of the triac. When connected to V_{SS}, the **mode** input activates an additional **option** "the **latched** option". If the main power drops from 230V to 120V, the triac control remains locked to the 230V mode and avoids any high voltage spike when the voltage is restored to 230V.
  When connected to V_{DD}, the **mode** input desactivates this **option** "this is the **follower** option".
- The TRIAC is specially designed for this application. An optimization between sensitivity and dynamic parameters of the triac gate highly reduces the losses of supply resistor and allows excellent immunity against line disturbances.

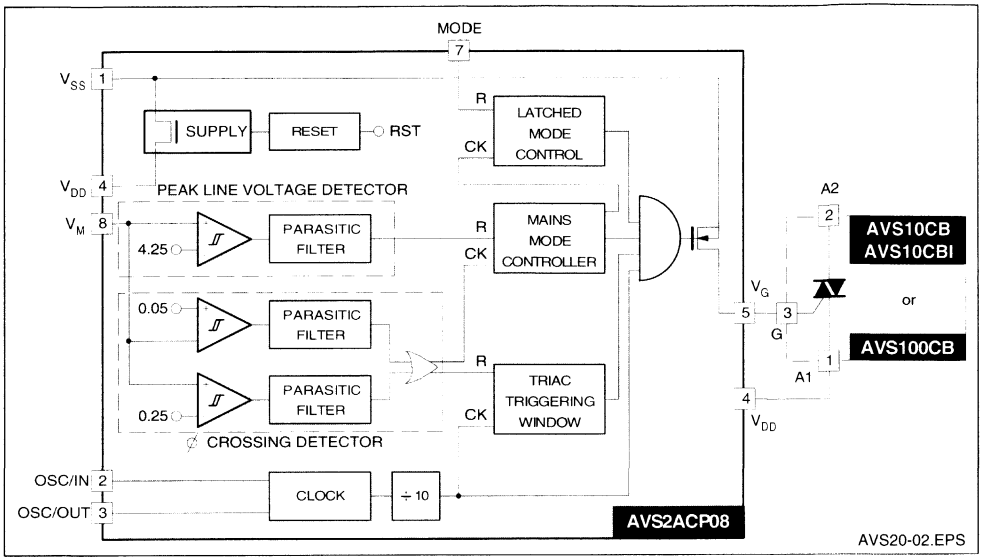
PIN CONNECTIONS

DIP8



AVS20-01.EPS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

CONTROLLER AVS2ACP08

Symbol	Parameter	Min.	Max.	Unit
V_{SS}	Supply voltage	- 12	0.5	V
V_I / V_O	I / O voltage	V_{SS} - 0.5	0.5	V
I_I / I_O	I / O current	- 40	+ 40	mA
T_{stg}	Storage Temperature	- 60	+ 150	°C
T_{oper}	Operating Temperature code " C "	0	+ 70	°C

AVS20-01.TBL

TRIAC AVS10CB / AVS10CBI / AVS100CB T_j = +25°C (unless otherwise specified)

Symbol	Parameter	Value	Unit
V_{DRM}	Repetitive peak off-state voltage (2) AVS10 AVS100	 ±600 ±800	 V V
$I_{T(RMS)}$	RMS on-state current (360° conduction angle) T_C = 80°C, AVS10CB/AVS100CB T_C = 70°C, AVS10CBI	 8 8	 A A
I_{TSM}	Non repetitive surge peak on-state current (T_j initial = 25°C) t = 8.3ms t = 10ms	 85 80	 A A
I^2t	I^2t value (t = 10ms)	32	A^2s
di/dt	Critical rate of rise of on-state current (1) Repetitive f = 50Hz Non Repetitive	 20 100	 A/µs A/µs
dv/dt (3)	Linear slope up to 400V (Gate open) (T_j = 70°C) AVS10 AVS100	 75 150	 V/µs V/µs
T_{stg}	Storage Temperature	-40, +150	°C
T_j	Operating Junction Temperature	0, +110	°C

AVS20-02.TBL

(1) Gate supply : I_G = 100mA – di/dt = 1A/µs
(2) T_j = 110°C
(3) For either polarity of electrode A_2 voltage with reference to electrode A_1

THERMAL RESISTANCES

TRIAC AVS10CB / AVS10CBI / AVS100CB

Symbol	Parameter	Value	Unit
$R_{th\ (j-a)}$	Junction-to-ambient	60	°C/W
$R_{th\ (j-c)}$ DC	Junction-to-case for DC		
	AVS10CB / AVS100CB	3.5	°C/W
	AVS10CBI	4.4	°C/W
$R_{th\ (j-c)}$ AC	Junction-to-case for 360° conduction angle (f = 50Hz)		
	AVS10CB / AVS100CB	2.6	°C/W
	AVS10CBI	3.3	°C/W

AVS20-03.TBL

DC GENERAL ELECTRICAL CHARACTERISTICS

TRIAC AVS10CB / AVS10CBI / AVS100CB

Symbol	Parameter	Min.	Max.	Unit
V_{GD}	$V_D = V_{DRM}$ $R_L = 3.3k\Omega$ Pulse duration> 20µs (T_j = 110°C)	0.2		V
V_{TM} (1)	I_{TM} = 11A (t_p = 10ms, T_j = 25°C)		1.75	V
I_{DRM} (1)	V_{DRM} rated Gate open			
	T_j = 25°C AVS10/AVS100		10	µA
	T_j = 110°C AVS10		500	µA
	T_j = 700°C AVS100		500	µA

AVS20-04.TBL

CONTROLLER AVS2ACP08 T_{oper} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
MAIN CHARACTERISTICS					
V_{SS} (pin 1) (Vreg)	Shunt Regulator Voltage	- 10	- 9	- 8	V
I_{SS} (pin 1) (Vreg) (@ V_{SS} = -9V)	Supply Current	0.4		30	mA
I_{SS} (pin 1) (@ triac gate non connected)	Quiescent Current		0.6	0.7	mA
F (pin 3) (@ R = 91kΩ) (C = 100pF)	Oscillator Frequency	42	44	46	kHz
V_{PWRON} (2)	Power-on-reset Threshold		0.89 Vreg		
V_{PWROFF} (2)	Power-off-reset Threshold		4.6		V
Mode (pin 7)	V_{IL} (2)			0.3 Vreg	
	V_{IH} (2)	0.7 Vreg			
V_G (pin 5)	V_{OL} (I_{VG} = 25mA)			650	mV
	Leakage Current ($V_G = V_{DD}$)			+ 10	µA
PEAK LINE VOLTAGE DETECTOR					
V_{SWON} (pin 8)	Low Threshold of Trip Point (switching-on of triac triggering) (3)	3.89	4.05	4.22	V
V_{SWOFF} (pin 8)	High Threshold of Trip Point (switching-off of triac triggering) (3)	4.08	4.25	4.42	V
t_{ON} (pin 5)	Triac Turn-on Delay Time (V_{AC} = 120V)	1		2	Line cycles
ZERO VOLTAGE CROSSING DETECTOR					
V_{0CR}PH (pin8)	High Threshold on Positive AC Side (3)		250		mV
V_{0CR}PL (pin8)	Low Threshold on Positive AC Side (3) (4)		200		mV
V_{0CR}NH (pin8)	High Threshold on Negative AC Side (3)		100		mV
V_{0CR}NL (pin8)	Low Threshold on Negative AC Side (3) (4)		60		mV

AVS20-05.TBL

NOTES :

(1) : For either polarity of electrode A_2 voltage with reference to electrode A_1.

(2) : Voltage referred to V_{DD}.

(3) : Voltage referred to V_{SS}.

(4) : These values give a typical noise immunity on the zero-crossing detection of 100mV x $\frac{1018}{18}$ = 5.65V on the mains supply.

Figure 1: Maximum RMS power dissipation versus RMS on-state current (f=60Hz) (Curves are cut-off $(di/dt)_c$ limitation)

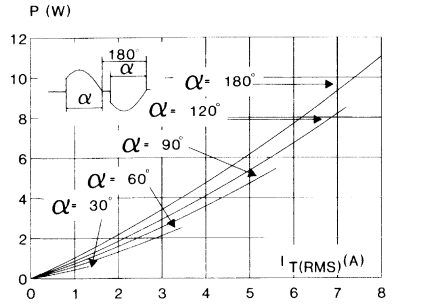


Figure 2a : Correlation between maximum mean power dissipation and maximum allowable temperatures (T_A and T_C) for different thermal resistances heat-sink + contact (AVS10CB/AVS100CB)

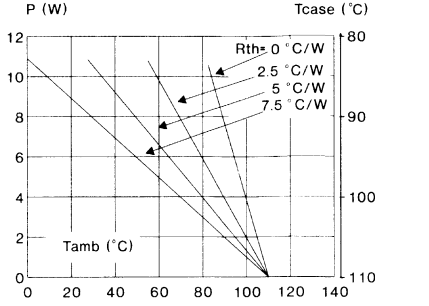
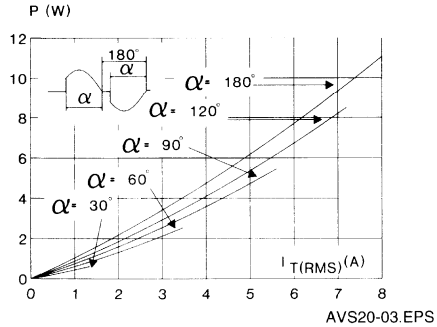


Figure 2b : Correlation between maximum mean power dissipation and maximum allowable temperatures (T_A and T_C) for different thermal resistances heat-sink + contact (AVS10CBI)



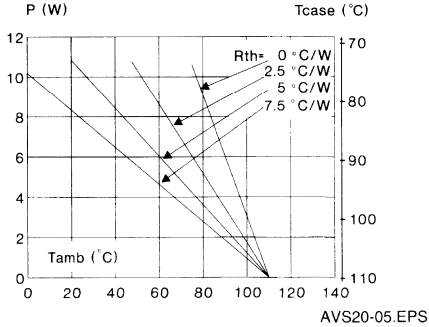


Figure 3 : Non-repetitive surge peak on-state current for a sinusoidal pulse with width : $t \leq 10ms$, and corresponding value of I^2t.

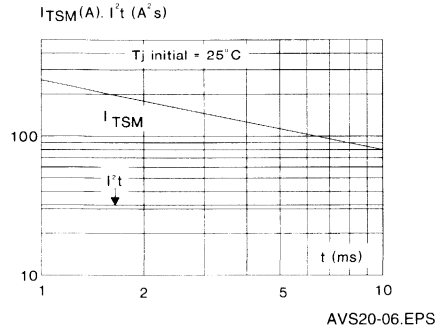
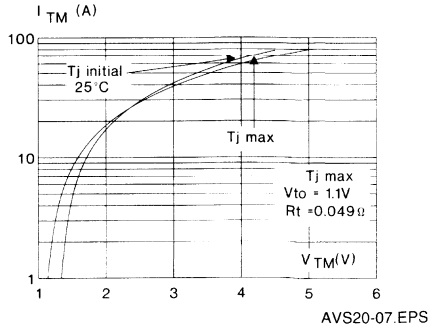
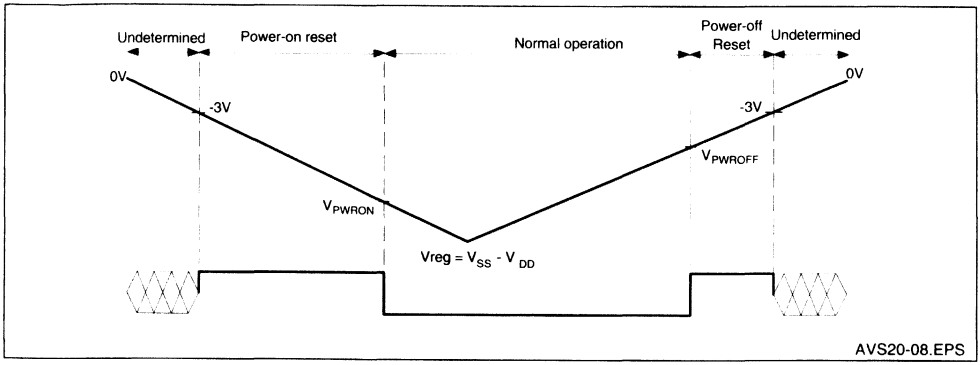


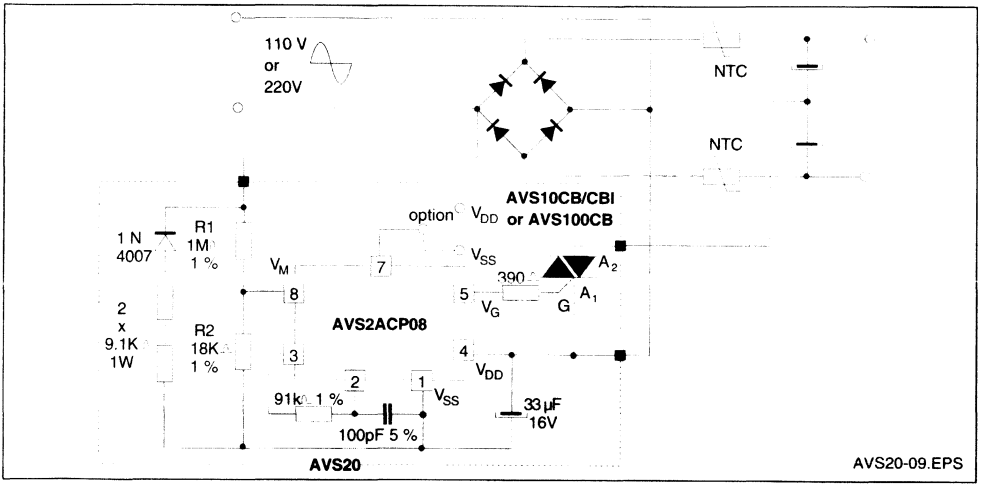
Figure 4 : On-state characteristics (maximum values).



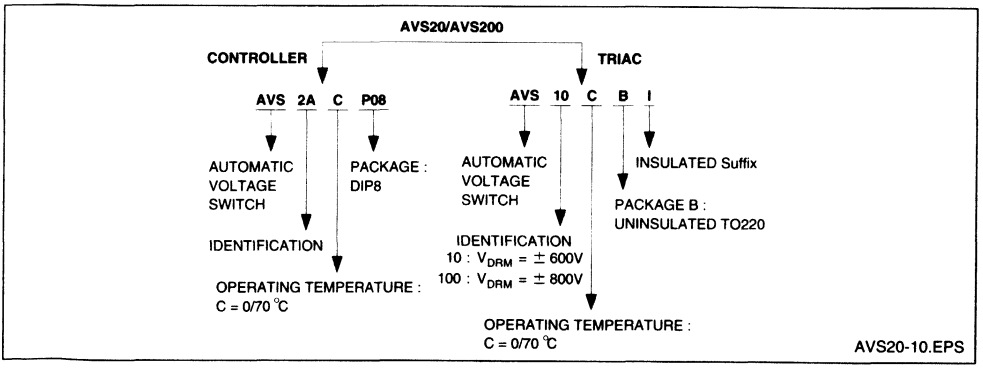
POWER-ON AND POWER-OFF RESET BEHAVIOUR



TYPICAL APPLICATION DIAGRAM

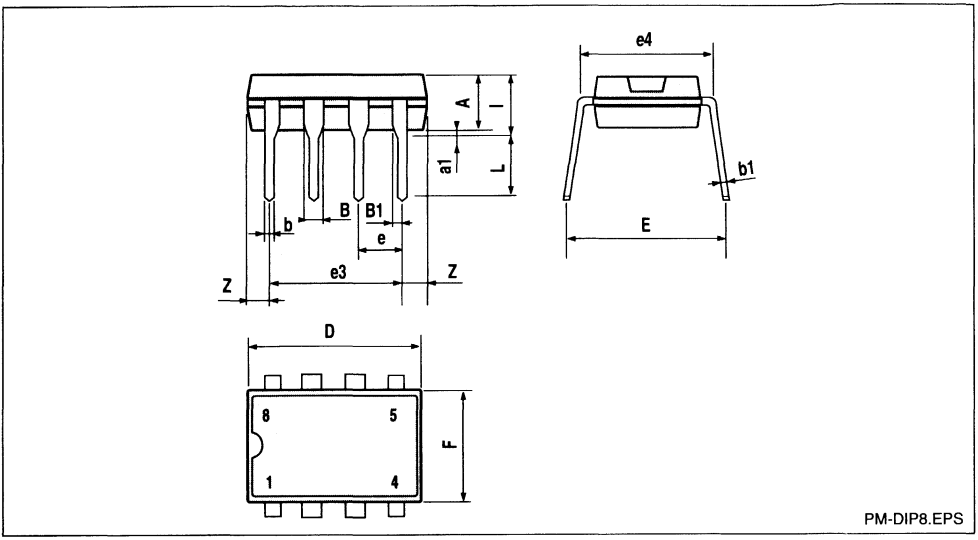


ORDERING INFORMATION



PACKAGE MECHANICAL DATA

CONTROLLER
8 PINS - PLASTIC DIP



PM-DIP8.EPS

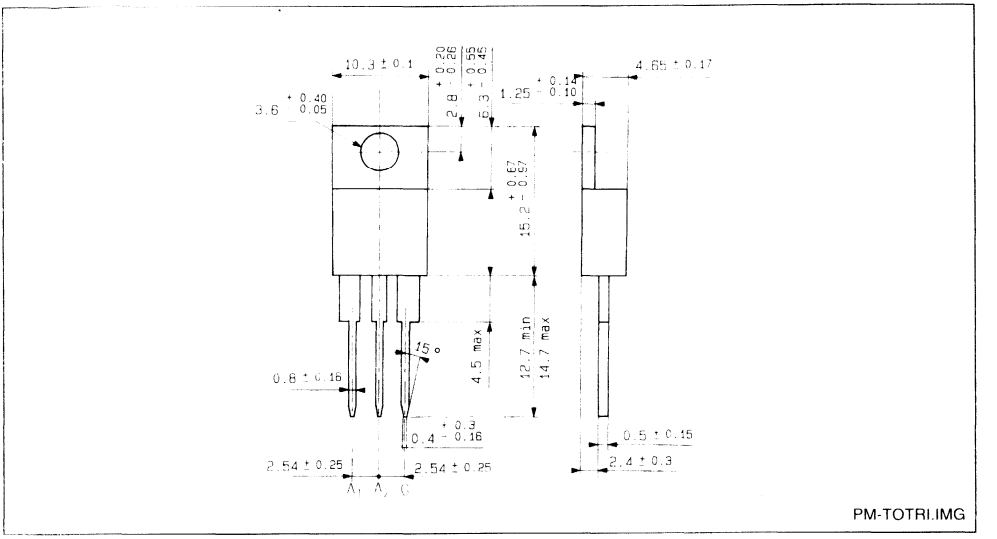
Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0260
i			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

DIP8.TBL

PACKAGE MECHANICAL DATA

TRIAC

3 PINS - PLASTIC TO220AB



Cooling method : by conduction (method C)
Weight : 2 g

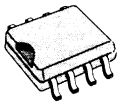
SGS-THOMSON MICROELECTRONICS

C78L00 SERIES

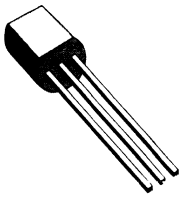
CMOS POSITIVE VOLTAGE REGULATORS VERY LOW DROP - VERY LOW QUIESCENT

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST/1)

- LOW CURRENT CONSUMPTION (TYP. 19µA)
- WIDE OPERATING VOLTAGE RANGE
- VERY LOW DROP OUT VOLTAGE (V_i - V_o < 0.2 V, I_o = 40 mA)
- CMOS TECHNOLOGY



SO-8



TO-92

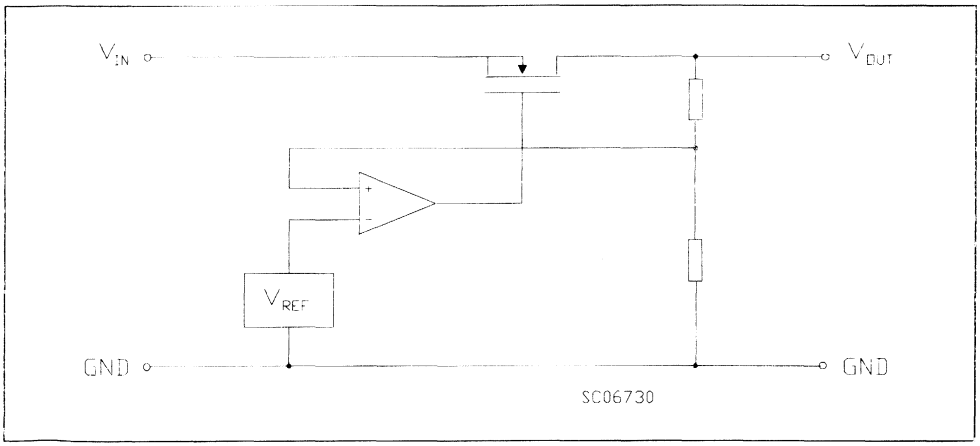
DESCRIPTION

The C78L00 series is a CMOS Positive Voltage Regulators. These regulators contains internal precision voltage reference, error amplifier, control transistor and output voltage setting resistor.

The regulation voltage is fixed by internal circuits and the following lines of different output voltages are available.

This series is suitable for battery operated items and battery back-up systems because of low current consumption and low drop out voltage

SCHEMATIC DIAGRAM



3A POWER OPERATIONAL AMPLIFIER

- OUTPUT CURRENT UP TO 3A
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGES
- SOA PROTECTION
- THERMAL PROTECTION
- ± 18V SUPPLY

The L165 is a monolithic integrated circuit in Pentawatt package, intended for use as power operational amplifier in a wide range of applications, including servo amplifiers and power supplies. The high gain and high output power capability provide superior performance wherever an operational amplifier/power booster combination is required.

Pentawatt

ORDER CODE : L165V

ABSOLUTE MAXIMUM RATINGS

V_S	Supply voltage	± 18	V
$V_5 - V_4$	Upper power transistor V_{CE}	36	V
$V_4 - V_3$	Lower power transistor V_{CE}	36	V
V_i	Input voltage	V_S	
V_i	Differential input voltage	± 15	V
I_o	Peak output current (internally limited)	3.5	A
P_{tot}	Power dissipation at T_{case} = 90 C	20	W
T_{stg}, T_j	Storage and junction temperature	– 40 to 150	C

APPLICATION CIRCUITS

Figure 1 : Gain > 10.

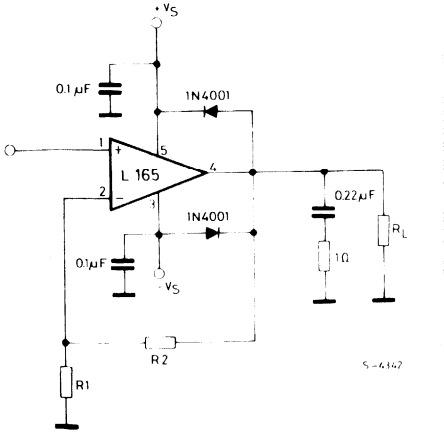
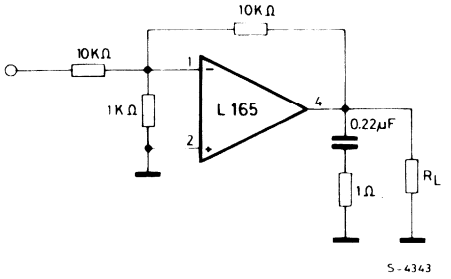
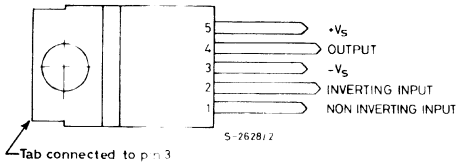


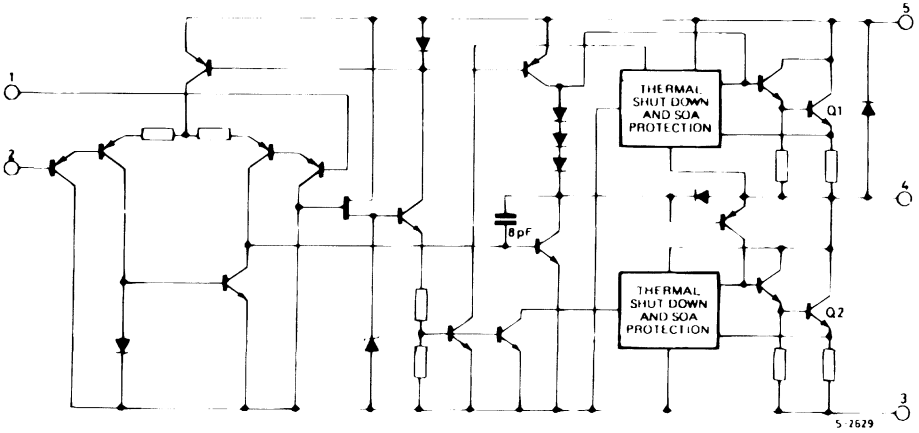
Figure 2 : Unity gain configuration.



CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	C/W

ELECTRICAL CHARACTERISTICS (V_S = ± 15 V, T_j = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		± 6		± 18	V
I_d	Quiescent Drain Current			40	60	mA
I_b	Input Bias Current	V_s = ± 18 V		0.2	1	µA
V_{os}	Input Offset Voltage			± 2	± 10	mV
I_{os}	Input Offset Current			± 20	± 200	nA
SR	Slew-rate	G_v = 10		8		V/µs
		G_v = 1 ( )		6		
V_o	Output Voltage Swing	f = 1 kHz I_p = 0.3 A		27		V_{pp}
		f = 1 kHz I_p = 3 A		24		V_{pp}
		f = 10 kHz I_p = 0.3 A		27		V_{PP}
		f = 10 kHz I_p = 3 A		23		V_{PP}
R	Input Resistance (pin 1)		100	500		KΩ
G_v	Voltage Gain (open loop)	f = 1 KHz		80		dB
e_N	Input Noise Voltage	B = 10 to 10 000 Hz		2		µV
i_N	Input Noise Current			100		pA
CMR	Common-mode Rejection	R_g ≤ 10 KΩ G_v = 30 dB		70		dB
SVR	Supply Voltage Rejection	R_g = 22 KΩ G_v = 10		60	dB	dB
		V_{ripple} = 0.5 V_{rms} f_{ripple} = 100 Hz dBG_v = 100		40		dB
	Efficiency	f = 1 kHz I_p = 1.6 A ; P_o = 5 W		70		%
		R_L = 4 Ω I_p = 3 A ; P_o = 18 W		60		%
T_{sd}	Thermal Shut-down Case Temperature	P_{tot} = 12 W		110		°C
		P_{tot} = 6 W		130		

Figure 3 : Open loop frequency response.

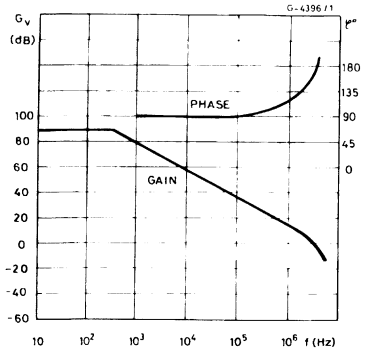


Figure 4 : Closed loop frequency response (circuit of figure 2).

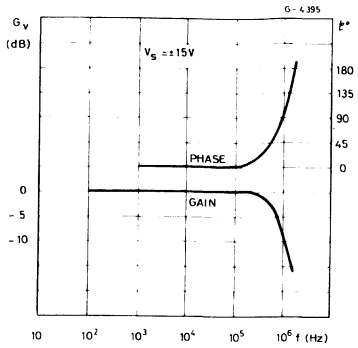


Figure 5 : Large signal frequency response.

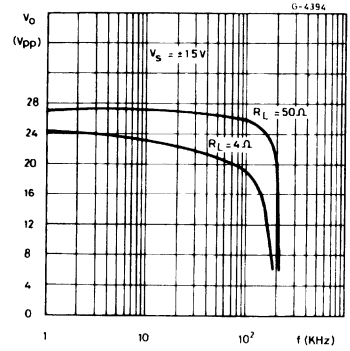


Figure 6 : Maximum output current vs. voltage [VCE] across each output transistor.

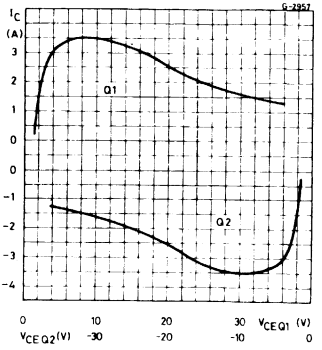


Figure 7 : Safe operating area and collector characteristics of the protected power transistor.

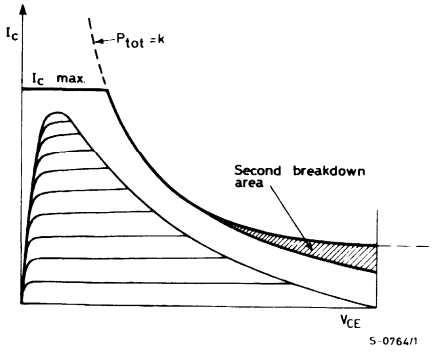


Figure 8 : Maximum allowable power dissipation vs. ambient temperature.

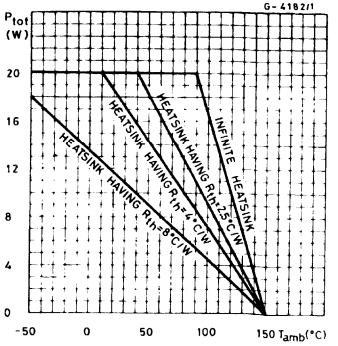
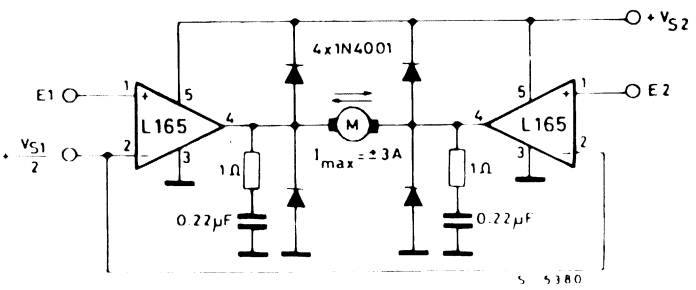
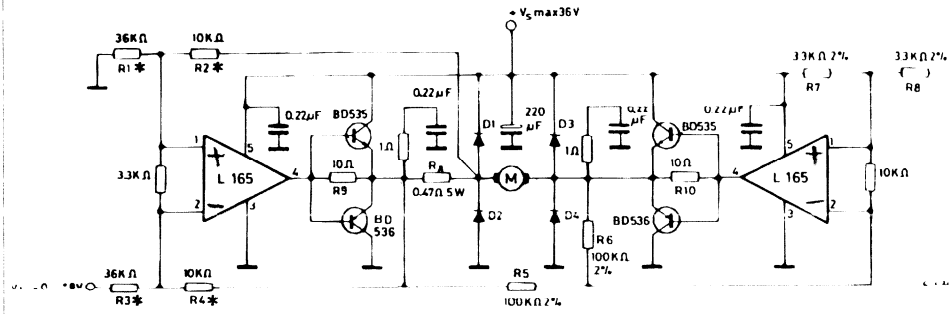


Figure 9 : Bidirectional DC motor control with TTL/CMOS/µP compatible inputs.



Must be $V_{S2} > V_{S1}$ E1, E2 = logic inputs
V_{S1} = logic supply voltage

Figure 10 : Motor current control circuit with external power transistors (I_{motor} > 3.5A).

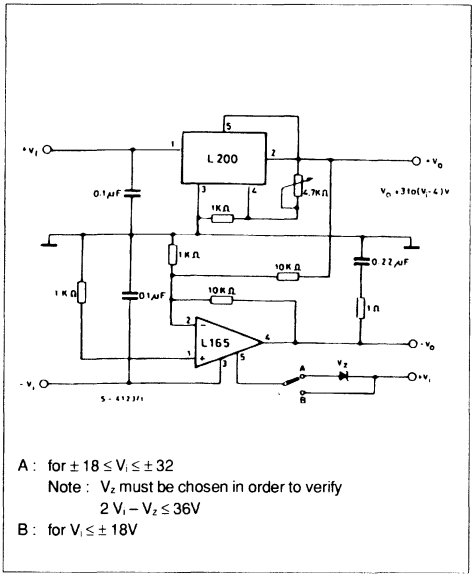


D1 to D4 : $V_F \leq 1.2$ @ $I = 4A$
$t_{rr} \leq 500$ ns

Note : The input voltage level is compatible with L291 (5-BIT D/A converter).

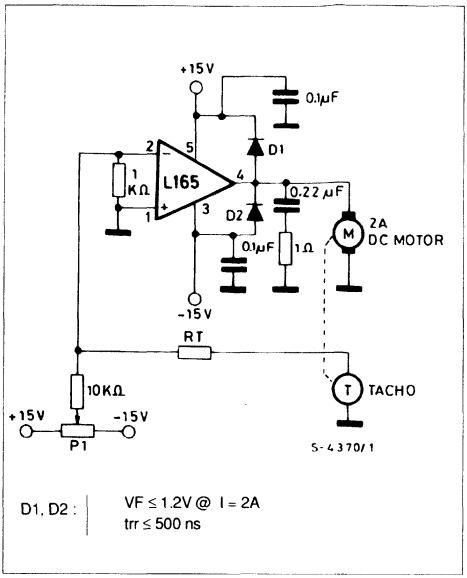
The transfer function is : $\frac{I_M}{V_i} = \frac{R4}{Rx\ R3}$

Figure 11 : High current tracking regulator.



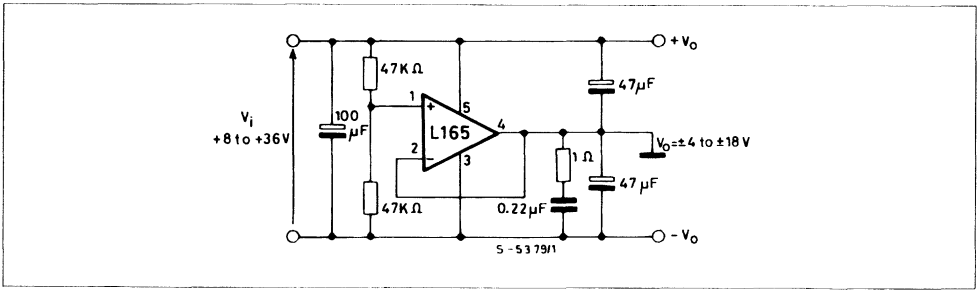
A : for $\pm 18 \leq V_i \leq \pm 32$
Note : V_z must be chosen in order to verify
$2V_i - V_z \leq 36V$
B : for $V_i \leq \pm 18V$

Figure 12 : Bidirectional speed control of DC motor (Compensation networks not shown).



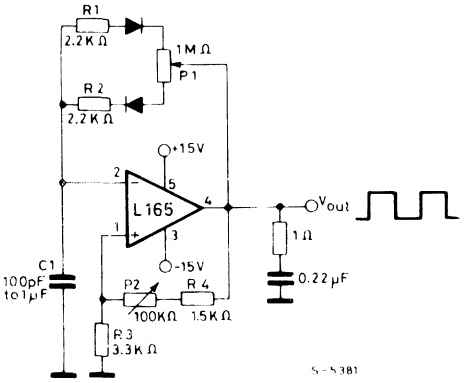
D1, D2 : VF ≤ 1.2V @ I = 2A
trr ≤ 500 ns

Figure 13 : Split power supply.



V_i +8 to +36V
$+V_o$
V_o ±4 to ±18 V
$-V_o$

Figure 14 : Power squarewave oscillator with independent adjustments for frequency and duty-cycle.



P1 : duty-cycle adjust
P2 : frequency adjust (f = 700 Hz with C1 = 10 nF, P2 = 100 KΩ, f = 25 Hz with C1 = 10 nF, P2 = 0)

SGS-THOMSON MICROELECTRONICS

L200

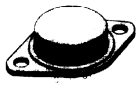
ADJUSTABLE VOLTAGE AND CURRENT REGULATOR

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST/1)

- ADJUSTABLE OUTPUT CURRENT UP TO 2 A (GUARANTEED UP TO T_j = 150 °C)
- ADJUSTABLE OUTPUT VOLTAGE DOWN TO 2.85 V
- INPUT OVERVOLTAGE PROTECTION (UP TO 60 V, 10 ms)
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTOR S.O.A. PROTECTION
- THERMAL OVERLOAD PROTECTION
- LOW BIAS CURRENT ON REGULATION PIN
- LOW STANDBY CURRENT DRAIN

metal case. Current limiting, power limiting, thermal shutdown and input overvoltage protection (up to 60 V) make the L200 virtually blow-out proof. The L200 can be used to replace fixed voltage regulators when high output voltage precision is required and eliminates the need to stock a range of fixed voltage regulators.

Pentawatt



TO-3 (4 lead)

DESCRIPTION

The L200 is a monolithic integrated circuit for voltage and current programmable regulation. It is available in Pentawatt® package or 4-lead TO-3

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	DC Input Voltage	40	V
V_i	Peak Input Voltage (10 ms)	60	V
ΔV_{i-o}	Dropout Voltage	32	V
I_o	Output Current	internally limited	
P_{tot}	Power Dissipation	internally limited	
T_{stg}	Storage Temperature	– 55 to 150	C
T_{op}	Operating Junction Temperature for L200C	– 25 to 150	C
	for L200	– 55 to 150	C

THERMAL DATA

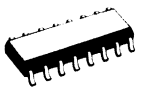
			TO-3	Pentawatt
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	4 C/W	3 C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	35 C/W	50 C/W

DUAL POWER OPERATIONAL AMPLIFIER

PRELIMINARY DATA

- OUTPUT CURRENT TO 1A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGE
- GROUND COMPATIBLE INPUTS
- LOW SATURATION VOLTAGE
- THERMAL SHUTDOWN

The L272D is a monolithic integrated circuit in SO-16 packages intended for use as power operational amplifier in a wide range of applications including servo amplifiers and power supplies, compact disc, VCR, etc. The high gain and high output power capability provide superior performance wheatever an operational amplifier/power booster combination is required.



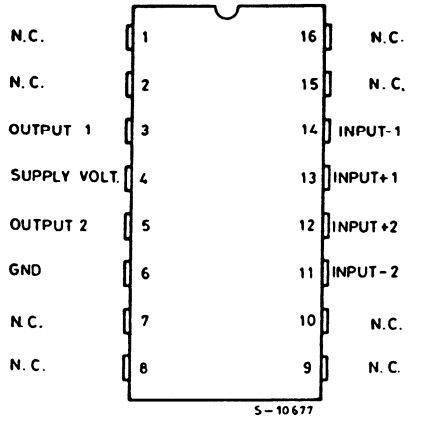
SO-16J

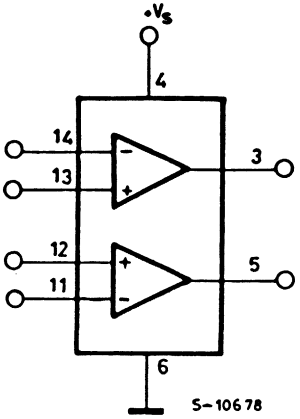
ORDERING NUMBER: L272D

ABSOLUTE MAXIMUM RATINGS

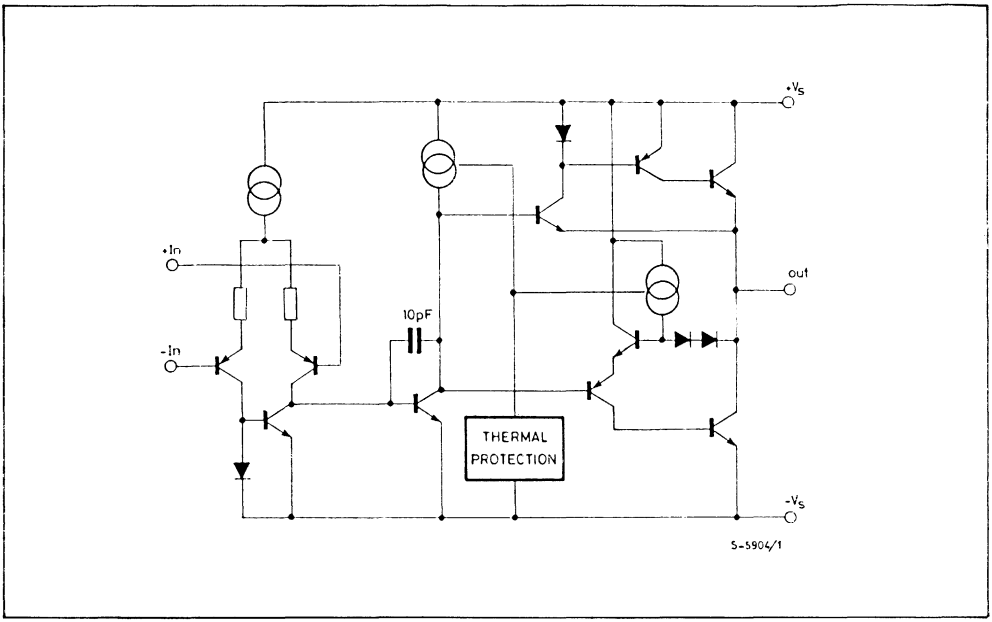
Symbol	Parameter	Value	Unit
V_s	Supply voltage	28	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	$\pm V_s$	
I_o	DC Output current	1	A
I_p	Peak output current (non repetitive)	1.5	A
P_{tot}	Power dissipation at $T_{case} = 90°C$	1.2	W
T_{op}	Operating Temperature Range	−40 to +85	°C
T_{stg}, T_j	Storage and junction temperature	−40 to 150	°C

CONNECTION DIAGRAMS





SCHEMATIC DIAGRAM (one only)



THERMAL DATA

$R_{thj\text{-}alumina(*)}$	Thermal resistance junction-alumina	max 50	°C/W

(*) Thermal resistance junctions-pins with the chip soldered on the middle of an alumina supporting substrate measuring 15 x 20 mm; 0.65 mm thickness and infinite heathsink.

ELECTRICAL CHARACTERISTICS (V_s = 24V, T_{amb} = 25°C unless otherwise specified)

	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			4		28	V
I_s	Quiescent drain current	$V_o = \frac{V_s}{2}$	V_s = 24V		8	12	mA
			V_s = 12V		7.5	11	mA
I_b	Input bias current				0.3	2.5	μA
V_{os}	Input offset voltage				15	60	mV
I_{os}	Input offset current				50	250	nA
SR	Slew rate				1		V/μs
B	Gain-bandwidth product				350		KHz
R_i	Input resistance			500			KΩ
G_v	O.L. voltage gain	f = 100Hz		60	70		dB
		f = 1KHz			50		dB
e_N	Input noise voltage	B = 20KHz			10		μV
I_N	Input noise current	B = 20KHz			200		pA
CRR	Common Mode rejection	f = 1KHz		60	75		dB
SVR	Supply voltage rejection	f = 100Hz R_G = 10KΩ V_R = 0.5V	V_s = 24V V_s = ±12V V_s = ± 6V	54	70 62 56		dB dB dB
V_o	Output voltage swing		I_p = 0.1A I_p = 0.5A	21	23 22.5		V V
C_s	Channel separation	f = 1KHz; R_L = 10Ω; G_v = 30dB	V_s = 24V V_s = ± 6V		60 60		dB dB
d	Distortion	f = 1KHz V_s = 24V	G_v = 30dB R_L = ∞		0.5		%
T_{sd}	Thermal shutdown junction temperature				145		°C

Fig. 1 - Quiescent current vs. supply voltage

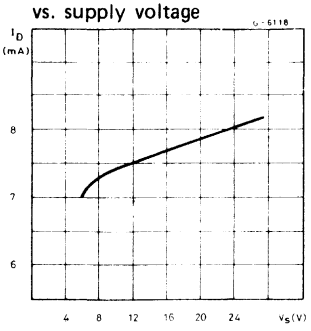


Fig. 2 - Quiescent drain current vs. temperature

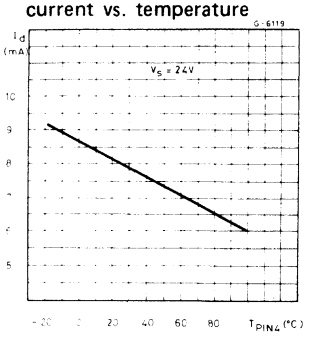


Fig. 3 - Open loop voltage gain

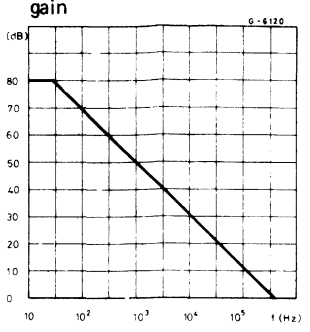


Fig. 4 - Output voltage swing vs. load current

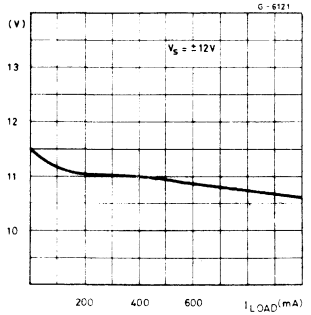


Fig. 5 - Output voltage swing vs. load current

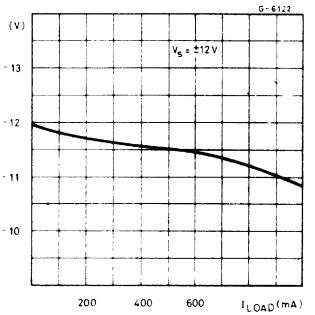


Fig. 6 - Supply voltage rejection vs. frequency

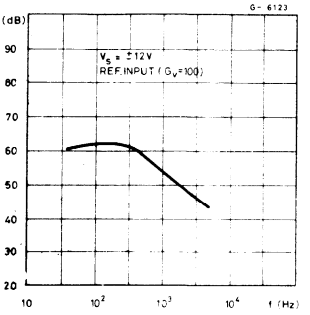


Fig. 7 - Channel separation vs. frequency

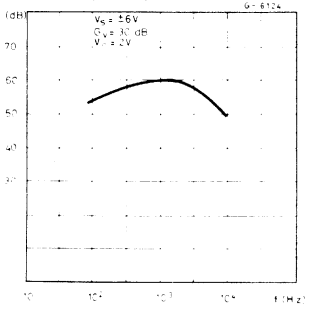
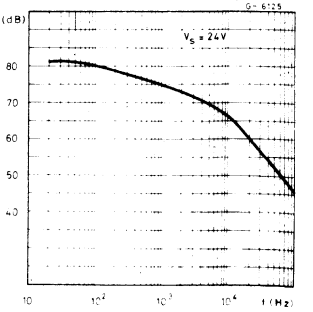


Fig. 8 - Common mode rejection vs. frequency



DUAL POWER OPERATIONAL AMPLIFIERS

- OUTPUT CURRENT TO 1A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGE
- GROUND COMPATIBLE INPUTS
- LOW SATURATION VOLTAGE
- THERMAL SHUTDOWN

The L272 and L272M are monolithic integrated circuits in powerdip and minidip packages intended for use as power operational amplifiers in a wide range of applications including servo amplifiers and power supplies, compact disc, VCR, etc.

The high gain and high output power capability provide superior performance whatever an operational amplifier/power booster combination is required.

Powerdip (8 + 8) **Minidip Plastic**

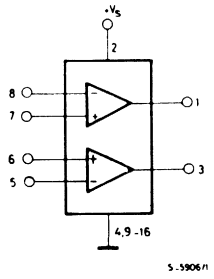
ORDERING NUMBERS:

L272 L272M

ABSOLUTE MAXIMUM RATINGS

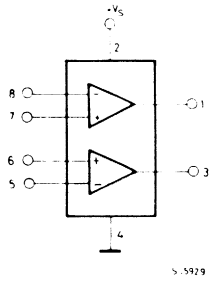
Symbol	Parameter	Value	Unit
V_s	Supply voltage	28	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	$\pm V_s$	
I_o	DC Output current	1	A
I_p	Peak output current (non repetitive)	1.5	A
P_{tot}	Power dissipation at T_{amb} = 80°C **(L272)**, T_{amb} = 50°C **(L272M)** T_{case} = 75°C **(L272)**	1.2 5	W W
T_{op}	Operating Temperature	- 40 to 85	°C
T_{stg}, T_j	Storage and junction temperature	40 to 150	°C

BLOCK DIAGRAM



S.-5906/1

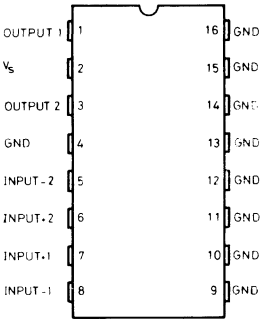
L272



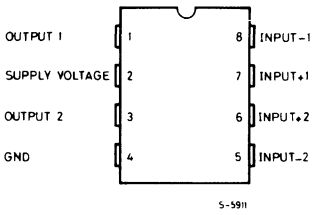
S.-5929

L272M

CONNECTION DIAGRAM
(Top view)

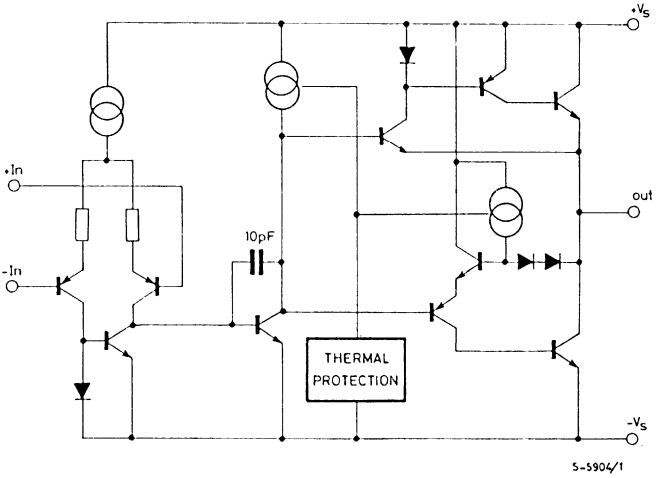


L272



L272M

SCHEMATIC DIAGRAM (one only)



THERMAL DATA

			Powerdip	Minidip
$R_{th\ j\text{-}case}$	Thermal resistance junction-pins	max	15°C/W	*70°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	70°C/W	100°C/W

* Thermal resistance junction-pin 4

ELECTRICAL CHARACTERISTICS (V_s = 24V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			4		28	V
I_s	Quiescent drain current	$V_o = \frac{V_s}{2}$	V_s = 24V		8	12	mA
			V_s = 12V		7.5	11	mA
I_b	Input bias current				0.3	2.5	μA
V_{os}	Input offset voltage				15	60	mV
I_{os}	Input offset current				50	250	nA
SR	Slew rate				1		V/μs
B	Gain-bandwidth product				350		KHz
R_I	Input resistance			500			KΩ
G_v	O.L. voltage gain	f = 100Hz		60	70		dB
		f = 1KHz			50		dB
e_N	Input noise voltage	B = 20KHz			10		μV
I_N	Input noise current	B = 20KHz			200		pA
CRR	Common Mode rejection	f = 1KHz		60	75		dB
SVR	Supply voltage rejection	f = 100Hz R_G = 10KΩ V_R = 0.5V	V_s = 24V V_s = ±12V V_s = ± 6V	54	70 62 56		dB dB dB
V_o	Output voltage swing		I_p = 0.1A I_p = 0.5A	21	23 22.5		V V
C_s	Channel separation	f = 1KHz; R_L = 10Ω; G_v = 30dB	V_s = 24V V_s = ± 6V		60 60		dB dB
d	Distortion	f = 1KHz V_s = 24V	G_v = 30dB R_L = ∞		0.5		%
T_{sd}	Thermal shutdown junction temperature				145		°C

Fig. 1 - Quiescent current vs. supply voltage

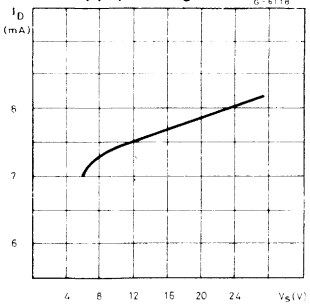


Fig. 2 - Quiescent drain current vs. temperature

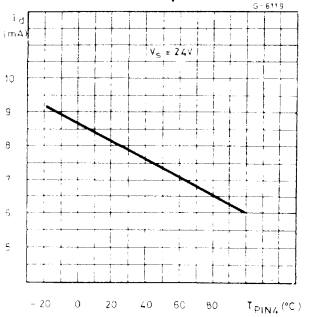


Fig. 3 - Open loop voltage gain

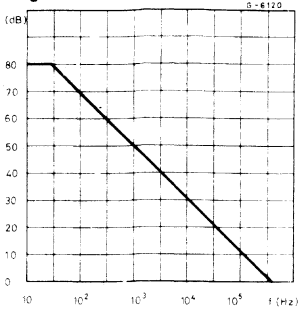


Fig. 4 - Output voltage swing vs. load current

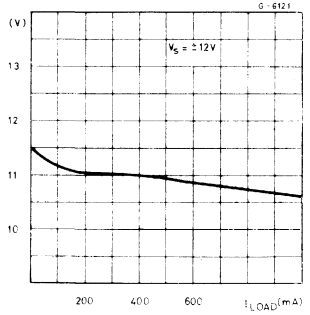


Fig. 5 - Output voltage swing vs. load current

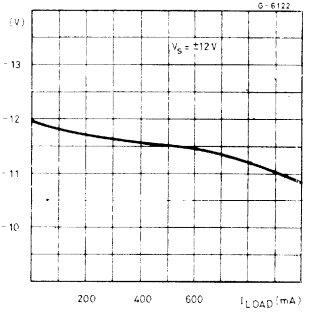


Fig. 6 - Supply voltage rejection vs. frequency

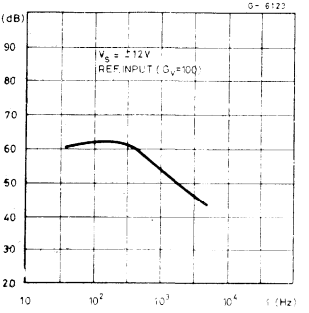


Fig. 7 - Channel separation vs. frequency

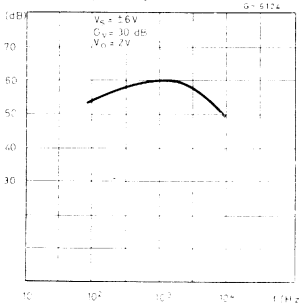
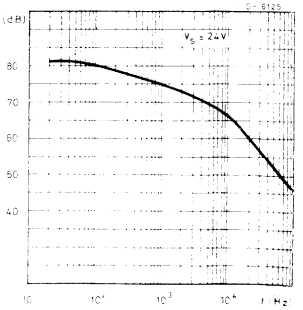


Fig. 8 - Common mode rejection vs. frequency



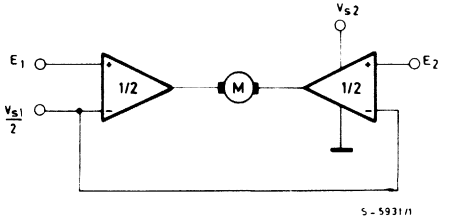
APPLICATION SUGGESTION

NOTE

In order to avoid possible instability occurring into final stage the usual suggestions for the linear power stages are useful, as for instance:

- layout accuracy;
- A 100nF capacitor corrected between supply pins and ground;
- boucherot cell (0.1 to 0.2μF + 1Ω series) between outputs and ground or across the load.

Fig. 9 - Bidirectional DC motor control with μP compatible inputs



V_{S1} = logic supply voltage

Must be $V_{S2} > V_{S1}$

E1, E2 = logic inputs

Fig. 10 - Servocontrol for compact-disc

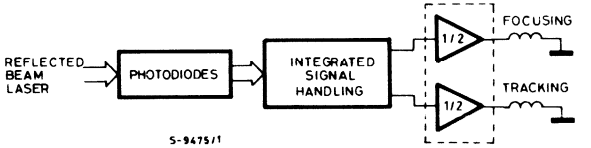


Fig. 11 - Capstan motor control in video recorders

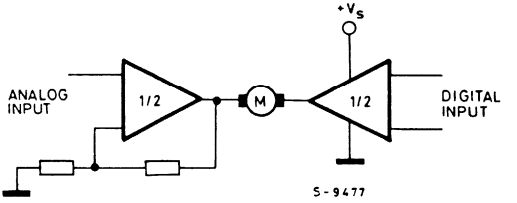
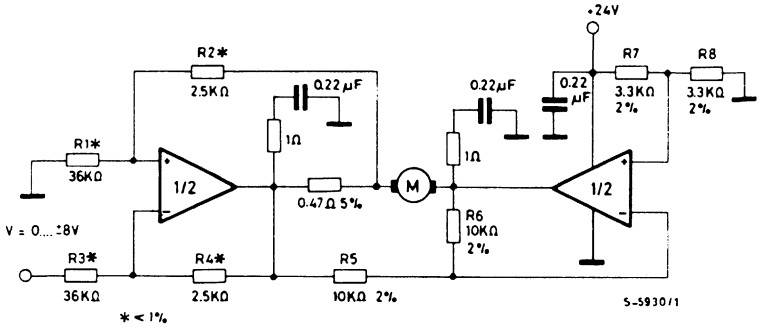


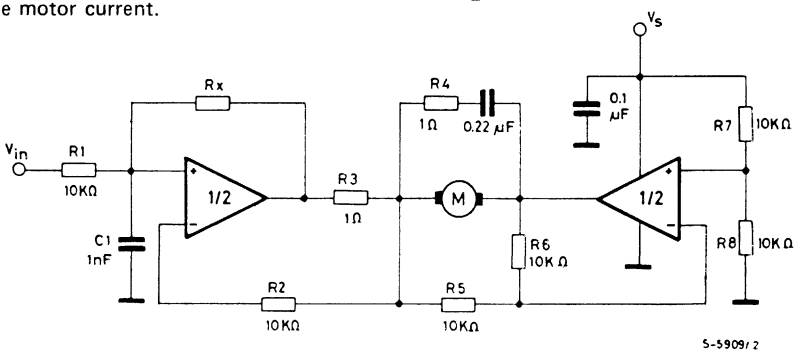
Fig. 12 - Motor current control circuit



Note: The input voltage level is compatible with L291 (5-BIT D/A converter)

Fig. 13 - Bidirectional speed control of DC motors.

For circuit stability ensure that $R_X > \frac{2R3 \circ R1}{R_M}$ where R_M = internal resistance of motor. The voltage available at the terminals of the motor is $V_M = 2\left(V_i - \frac{V_s}{2}\right) + |R_o|.\ I_M$ where $|R_o| = \frac{2R3 \circ R1}{R_X}$ and I_M is the motor current.



SGS-THOMSON MICROELECTRONICS

L296
L296P

HIGH CURRENT SWITCHING REGULATORS

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST/1)

- 4 A OUTPUT CURRENT
- 5.1 V TO 40 V OUTPUT VOLTAGE RANGE
- 0 TO 100 % DUTY CYCLE RANGE
- PRECISE (±2 %) ON-CHIP REFERENCE
- SWITCHING FREQUENCY UP TO 200 KHz
- VERY HIGH EFFICIENCY (UP TO 90 %)
- VERY FEW EXTERNAL COMPONENTS
- SOFT START
- RESET OUTPUT
- EXTERNAL PROGRAMMABLE LIMITING CURRENT (L296P)
- CONTROL CIRCUIT FOR CROWBAR SCR
- INPUT FOR REMOTE INHIBIT AND SYNCHRONUS PWM
- THERMAL SHUTDOWN

DESCRIPTION

The L296 and L296P are stepdown power switching regulators delivering 4 A at a voltage variable from 5.1 V to 40 V.

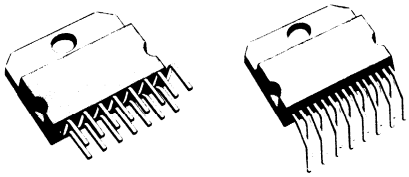
Features of the devices include soft start, remote inhibit, thermal protection, a reset output for microprocessors and a PWM comparator input for synchronization in multichip configurations.

The L296P incudes external programmable limiting current.

The L296 and L296P are mounted in a 15-lead Multiwatt® plastic power package and requires very few external components.

Efficient operation at switching frequencies up to 200 KHz allows a reduction in the size and cost of external filter components. A voltage sense input and SCR drive output are provided for optional crowbar overvoltage protection with an external SCR.

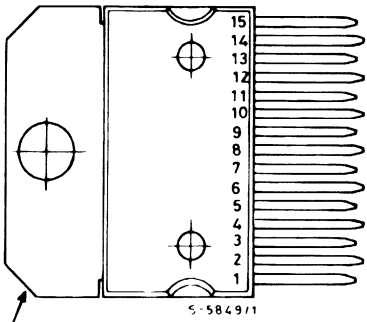
Multiwatt
(15-lead)



ORDER CODES :

L296	L296HT
L296P	L296PHT

PIN CONNECTION (top view)



CROWBAR DRIVE
RESET OUTPUT
RESET DELAY
RESET INPUT
OSCILLATOR
FEEDBACK INPUT
FREQUENCY COMPENSATION
GROUND
SYNC. INPUT
INHIBIT INPUT
SOFT-START
CURRENT LIMIT
SUPPLY VOLTAGE
OUTPUT
CROWBAR INPUT

Tab connected to pin 8

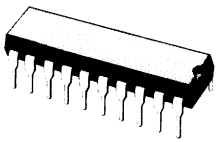
SGS-THOMSON MICROELECTRONICS

L297
L297A

STEPPER MOTOR CONTROLLERS

- NORMAL/WAWE DRIVE
- HALF/FULL STEP MODES
- CLOCKWISE/ANTICLOCKWISE DIRECTION
- SWITCHMODE LOAD CURRENT REGULATION
- PROGRAMMABLE LOAD CURRENT
- FEW EXTERNAL COMPONENTS
- RESET INPUT & HOME OUTPUT
- ENABLE INPUT
- STEP-PULSE DOUBLER (L297A only)

The L297 Stepper Motor Controller IC generates four phase drive signals for two phase bipolar and four phase unipolar step motors in microcomputer-controlled applications. The motor can be driven in half step, normal and wawe drive modes and on-chip PWM chopper circuits permit switch-mode control of the current in the windings. A feature of this device is that it requires only clock, direction and mode input signals. Since the phase are generated internally the burden on the microprocessor, and the programmer, is greatly reduced. Mounted in a 20-pin plastic package, the L297 can be used with monolithic bridge drives such as the L298N or L293E, or with discrete transistors and darlingtons. The L297A also includes a clock pulse doubler.



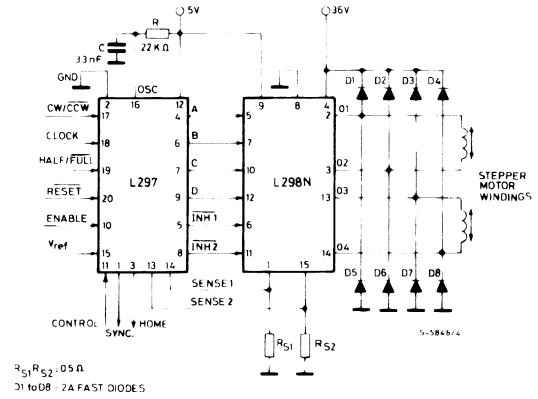
DIP-20 Plastic
(0.25)

ORDER CODES : L297 – L297A

ABSOLUTE MAXIMUM RATINGS

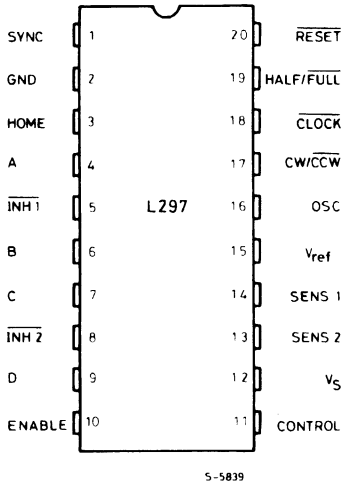
V_s	Supply voltage	10	V
V_i	Input signals	7	V
P_{tot}	Total power dissipation (T_{amb} = 70 C)	1	W
T_{stg}, T_j	Storage and junction temperature	– 40 to + 150	C

TWO PHASE BIPOLAR STEPPER MOTOR CONTROL CIRCUIT

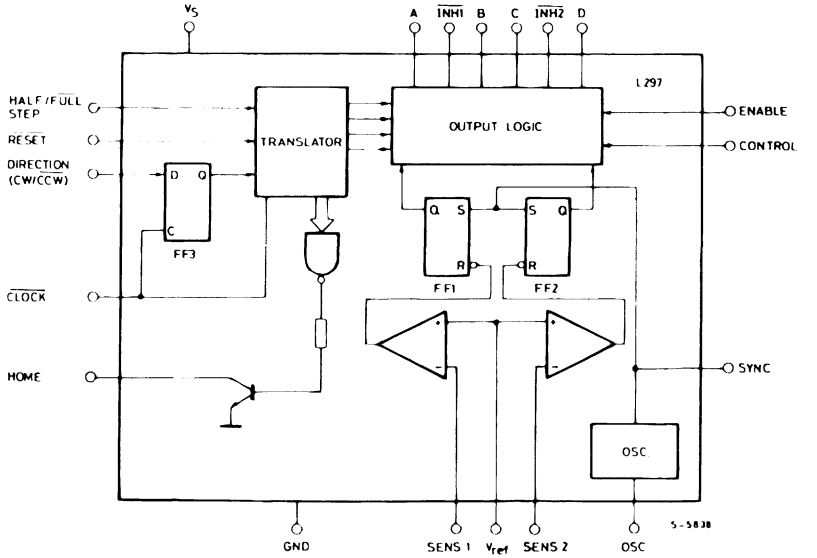


RS1 RS2 : 0.5Ω
D1 to D8 : 2A FAST DIODES

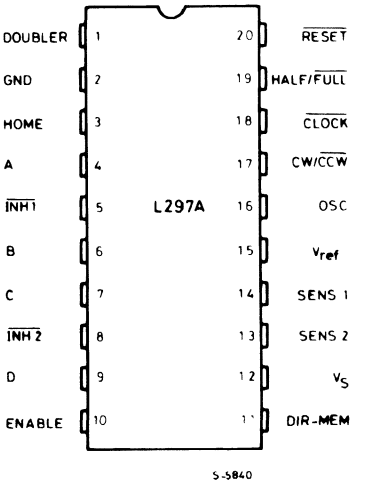
PIN CONNECTION (L297)



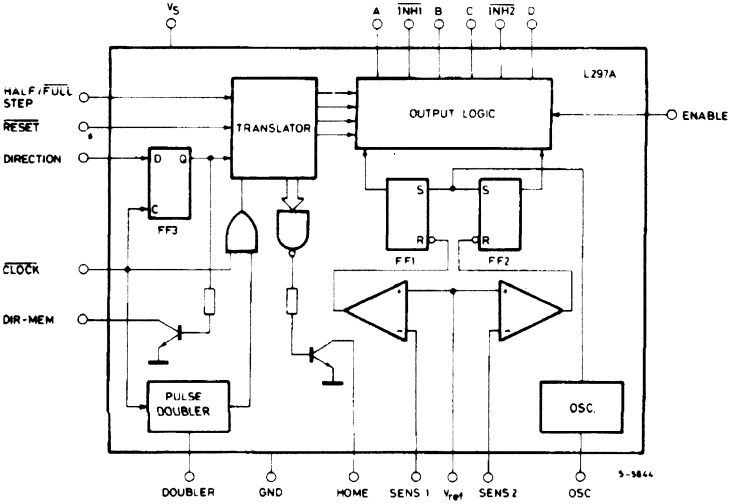
BLOCK DIAGRAM (L297)



PIN CONNECTION (L297A)



BLOCK DIAGRAM (L297A)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	C/W

PIN FUNCTIONS – L297

N°	NAME	FUNCTION
1	SYNC	Output of the on-chip chopper oscillator. The SYNC connections of all L297s to be synchronized are connected together and the oscillator components are omitted on all but one. If an external clock source is used it is injected at this terminal.
2	GND	Ground connection
3	HOME	Open collector output that indicates when the L297 is in its initial state (ABCD = 0101). The transistor is open when this signal is active.
4	A	Motor phase A drive signal for power stage.
5	$\overline{INH1}$	Active low inhibit control for driver stages of A and B phases. When a bipolar bridge is used this signal can be used to ensure fast decay of load current when a winding is de-energized. Also used by chopper to regulate load current if CONTROL input is low.
6	B	Motor phase B drive signal for power stage.
7	C	Motor phase C drive signal for power stage.
8	$\overline{INH2}$	Active low inhibit control for drive stages of C and D phases. Same functions as $\overline{INH1}$.
9	D	Motor phase D drive signal for power stage.
10	ENABLE	Chip enable input. When low (inactive) $\overline{INH1}$, $\overline{INH2}$, A, B, C and D are brought low.
11	CONTROL	Control input that defines action of chopper. When low chopper acts on $\overline{INH1}$ and $\overline{INH2}$; when high chopper acts on phase lines ABCD.
12	V_s	5V supply input.
13	$SENS_2$	Input for load current sense voltage from power stages of phases C and D.
14	$SENS_1$	Input for load current sense voltage from power stages of phases A and B.
15	V_{ref}	Reference voltage for chopper circuit. A voltage applied to this pin determines the peak load current.
16	OSC	An RC network (R to V_{CC}, C to ground) connected to this terminal determines the chopper rate. This terminal is connected to ground on all but one device in synchronized multi - L297 configurations. $f \cong 1/0.69\ RC$, $R > 10k\Omega$.
17	CW/$\overline{CCW}$	Clockwise/counterclockwise direction control input. Physical direction of motor rotation also depends on connection of windings. Synchronized internally therefore direction can be changed at any time.
18	$\overline{CLOCK}$	Step clock. An active low pulse on this input advances the motor one increment. The step occurs on the rising edge of this signal.

PIN FUNCTIONS – L297 (continued)

N	NAME	FUNCTION
19	HALF/FULL	Half/full step select input. When high selects half step operation, when low selects full step operation. One-phase-on full step mode is obtained by selecting FULL when the L297's translator is at an even-numbered state. Two-phase-on full step mode is set by selecting FULL when the translator is at an odd numbered position. (The home position is designate state 1).
20	RESET	Reset input. An active low pulse on this input restores the translator to the home position (state 1, ABCD = 0101).

PIN FUNCTIONS – L297A

Pin function of the L297A are identical to those of the L297 except for pins 1 and 11.

N	NAME	FUNCTIONS
1	DOUBLER	An RC network connected to this pin determines the delay between an input clock pulse and the corresponding ghost pulse.
11	DIR-MEM	Direction Memory. Inverted output of the direction flip flop. Open collector output.

CIRCUIT OPERATION

The L297(A) is intended for use with a dual bridge driver, quad darlington array or discrete power devices in step motor driving applications. It receives step clock, direction and mode signals from the systems controller (usually a microcomputer chip) and generates control signals for the power stage.

The principal functions are a translator, which generates the motor phase sequences, and a dual PW/M chopper circuit which regulates the current in the motor windings. The translator generates three different sequences, selected by the HALF/FULL input. These are normal (two phases energised), wave drive (one phase energised) and half-step (alternately one phase energised/two phases energised). Two inhibit signals are also generated by the L297 in half step and wave drive modes. These signals, which connect directly to the L298's enable inputs, are intended to speed current decay when a winding is de-energised. When the L297 is used to drive a unipolar motor the chopper acts on these lines.

An input called CONTROL determines whether the chopper will act on the phase lines ABCD or the inhibit lines INH1 and INH2. When the phase lines are chopped the non-active phase line of each pair (AB or CD) is activated (rather than interrupting the line then active). In L297 + L298 configurations this technique reduces dissipation in the load current sense resistors.

A common on-chip oscillator drives the dual chopper. It supplies pulses at the chopper rate which set the two flip-flops FF1 and FF2. When the current in a winding reaches the programmed peak value the voltage across the sense resistor (connected to one of the sense inputs $SENS_1$ or $SENS_2$) equals V_{ref} and the corresponding comparator resets its flip flop, interrupting the drive current until the next oscillator pulse arrives. The peak current for both windings is programmed by a voltage divider on the V_{ref} input.

Ground noise problems in multiple configurations can be avoided by synchronising the chopper oscillators. This is done by connecting all the SYNC pins together, mounting the oscillator RC network on one device only and grounding the OSC pin on all other devices.

The L297A includes a pulse doubler on the step clock line which is intended to simplify the implementation of multiple stepping. A ghost pulse is generated automatically after each input pulse, delayed by the time $0.75\ R_d\ C_d$.

The RC network should be dimensioned to place the ghost pulse roughly halfway between clock pulses. If pin 1 (DOUBLER) is grounded the doubler function is disabled.

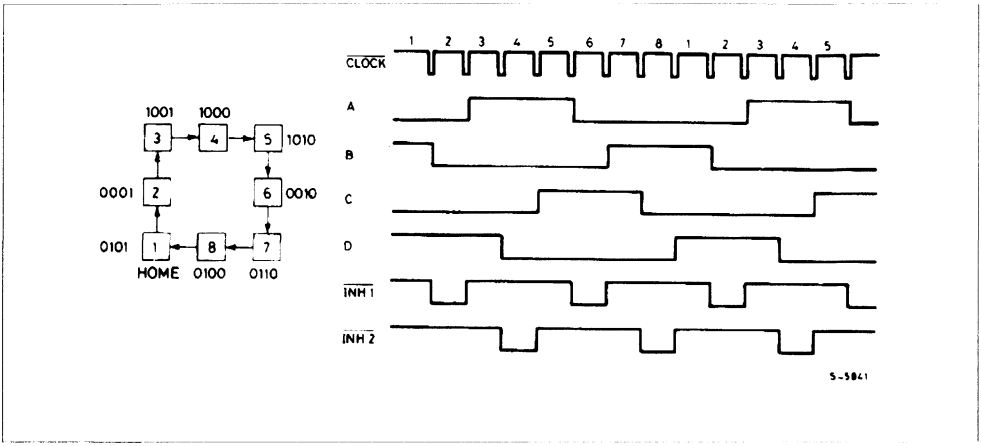
MOTOR DRIVING PHASE SEQUENCES

The L297's translator generates phase sequences for normal drive, wave drive and half step modes. The state sequences and output waveforms for these three modes are shown below. In all cases the translator advances on the low to high transition of CLOCK.

Clockwise rotation is indicated ; for anticlockwise rotation the sequences are simply reversed RESET restores the translator to state 1, where ABCD = 0101.

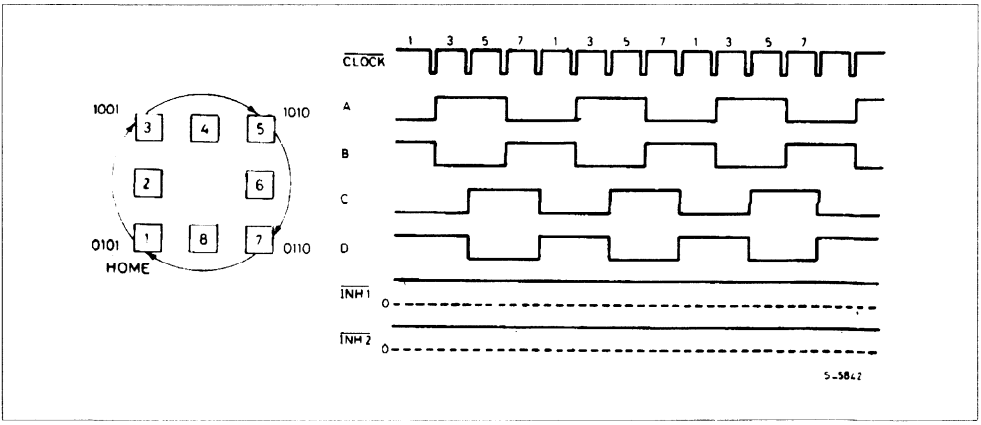
HALF STEP MODE

Half step mode is selected by a high level on the HALF/FULL input.



NORMAL DRIVE MODE

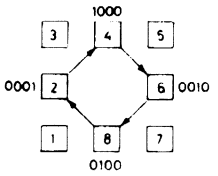
Normal drive mode (also called "two-phase-on" drive) is selected by a low level on the HALF/FULL input when the translator is at an odd numbered state (1, 3, 5 or 7). In this mode the INH1 and INH2 outputs remain high throughout.

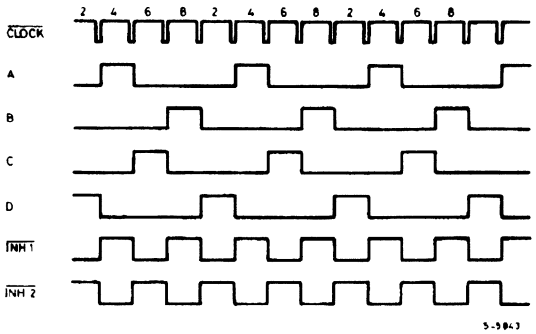


MOTOR DRIVING PHASE SEQUENCES (continued)

WAVE DRIVE MODE

Wave drive mode (also called "one-phase-on" drive) is selected by a low level on the HALF/FULL input when the translator is at an even numbered state (2, 4, 6 or 8).





ELECTRICAL CHARACTERISTICS (Refer to the block diagram T_{amb} = 25 C, V_S = 5V unless otherwise specified)

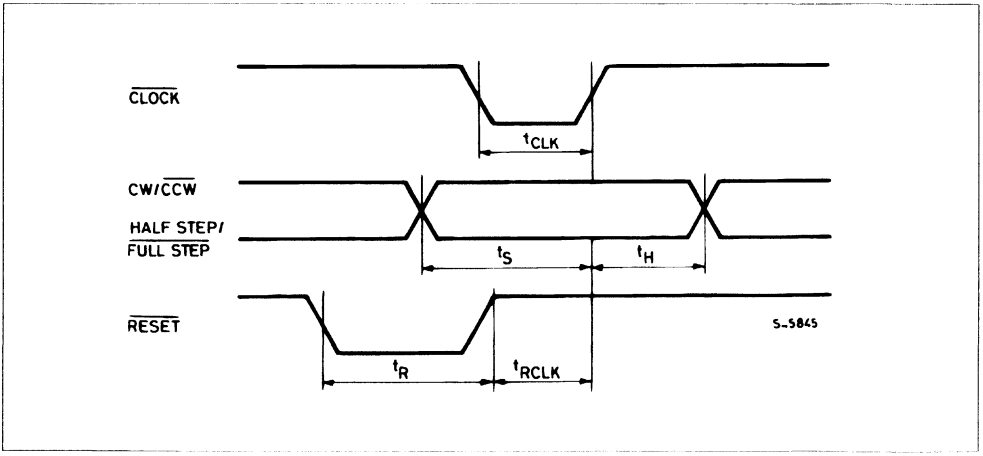
	Parameter	Test conditions		Min.	Typ.	Max.	Unit
V_S	Supply voltage (pin 12)			4.75		7	V
I_S	Quiescent supply current (pin 12)	Outputs floating			50	80	mA
V_i	Input voltage (pin 11, 17, 18, 19, 20)		Low			0.8	V
			High	2		V_S	V
I_i	Input current (pin 11, 17, 18, 19, 20)		V_i = L			−100	µA
			V_i = H			10	µA
V_{en}	Enable input voltage (pin 10)		Low			1.5	V
			High	2		V_S	V
I_{en}	Enable input current (pin 10)		V_{en} = L			−100	µA
			V_{en} = H			10	µA
V_o	Phase output voltage (pins 4, 6, 7, 9)	I_o = 10mA	V_{OL}			0.4	V
		I_o = 5mA	V_{OH}	3.9			V
V_{inh}	Inhibit output voltage (pins 5, 8)	I_o = 10mA	$V_{inh\ L}$			0.4	V
		I_o = 5mA	$V_{inh\ H}$	3.9			V
V_{SYNC}	Sync Output Voltage	I_o = 5mA	$V_{SYNC\ H}$	3.3			V
		I_o = 5mA	$V_{SYNC\ V}$			0.8	

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_{leak}	Leakage current (pin 3, 11*)	V_{CE} = 7 V			1	µA
V_{sat}	Saturation voltage (pins 3, 11*)	I = 5 mA			0.4	V
V_{off}	Comparators offset voltage (pins 13, 14, 15)	V_{ref} = 1 V			5	mV
I_b	Comparator bias current (pins 13, 14, 15)		– 100		10	µA
V_{ref}	Input reference voltage (pin 15)		0		3	V
t_{CLK}	Clock time		0.5			µs
t_S	Set up time		1			µs
t_H	Hold time		4			µs
t_R	Reset time		1			µs
t_{RCLK}	Reset to clock delay		1			µs

* L297A only

Figure 1.



APPLICATION INFORMATION

TWO PHASE BIPOLAR STEPPER MOTOR CONTROL CIRCUIT

This circuit drives bipolar stepper motors with winding currents up to 2A. The diodes are fast 2A types.

Figure 2.

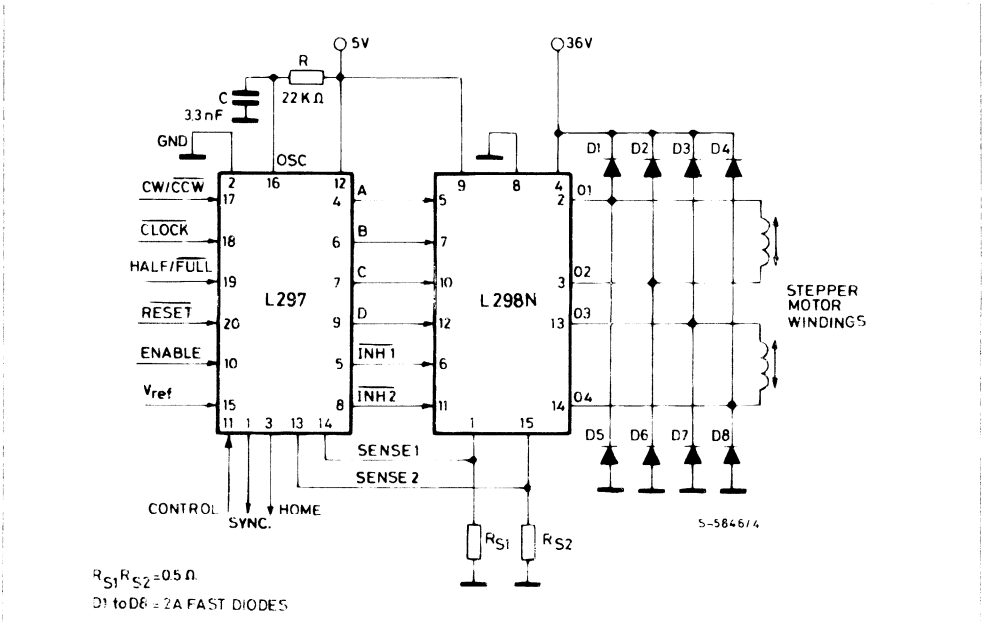


Figure 3 : Synchronising L297s

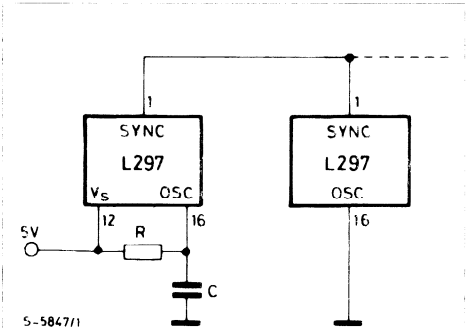
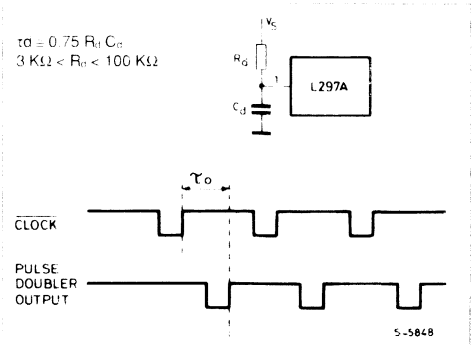


Figure 4 : Pulse doubler (L297A)



SGS-THOMSON
MICROELECTRONICS

L298N

DUAL FULL-BRIDGE DRIVER

PRELIMINARY DATA

- OPERATING SUPPLY VOLTAGE UP TO 46 V
- TOTAL DC CURRENT UP TO 4 A
- LOW SATURATION VOLTAGE
- OVERTEMPERATURE PROTECTION
- LOGICAL "0" INPUT VOLTAGE UP TO 1.5 V (HIGH NOISE IMMUNITY)

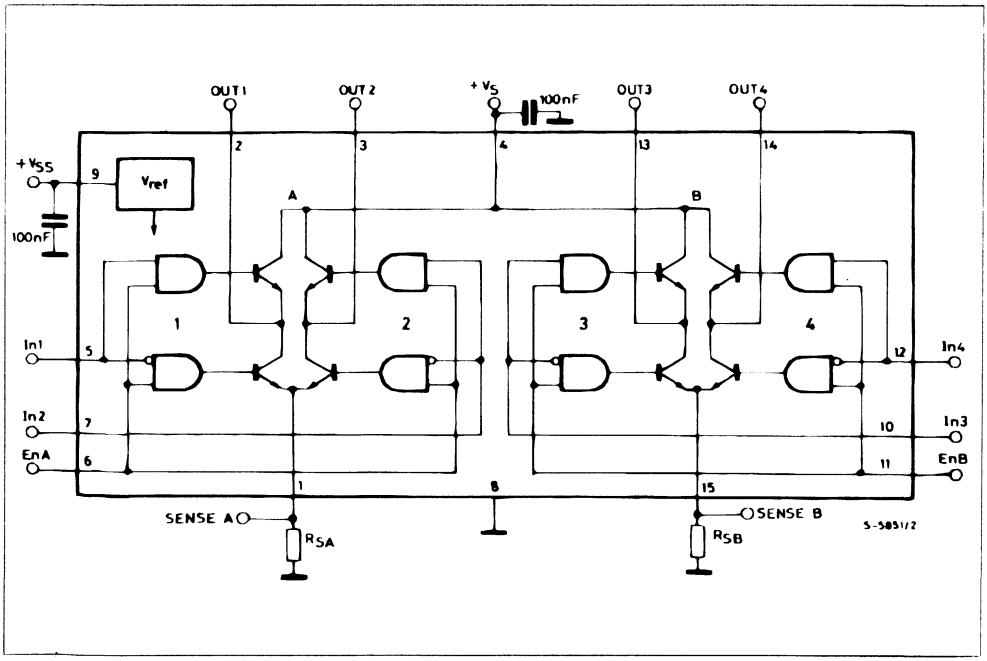
DESCRIPTION

The L298N is an integrated monolithic circuit in a 15-lead Multiwatt® package. It is a high voltage, high current dual full-bridge driver designed to accept standard TTL logic levels and drive inductive loads such as relays, solenoids, DC and stepping motors. Two enable inputs are provided to enable or disable the device independently of the input signals. The emitters of the lower transistors of each bridge are connected together and the corresponding external terminal can be used for the connection of an external sensing resistor. An additional supply input is provided so that the logic works at a lower voltage.

Multiwatt
(15-lead)

ORDER CODES : L298N
L298HN

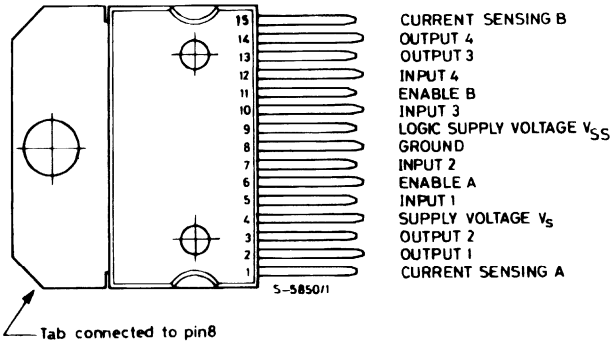
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
V_S	Power Supply	50	V
V_{SS}	Logic Supply Voltage	7	V
V_I, V_{en}	Input and Enable Voltage	– 0.3 to 7	V
I_O	Peak Output Current (each channel) - Non Repetitive (t = 100 µs) - Repetitive (80 % on – 20 % off ; t_{on} = 10 ms) - DC Operation	 3 2.5 2	 A A A
V_{sens}	Sensing Voltage	– 1 to 2.3	V
P_{tot}	Total Power Dissipation (T_{case} = 75 °C)	25	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

PIN CONNECTION (top view)



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	35	°C/W

PIN FUNCTIONS (refer to the block diagram)

N	Name	Function
1 ; 15	Sense A ; Sense B	Between this pin and ground is connected the sense resistor to control the current of the load.
2 ; 3	Out 1 ; Out 2	Outputs of the Bridge A ; the current that flows through the load connected between these two pins is monitored at pin 1.
4	V_S	Supply Voltage for the Power Output Stages. A non-inductive 100 nF capacitor must be connected between this pin and ground.
5 ; 7	Input 1 ; Input 2	TTL Compatible Inputs of the Bridge A.
6 ; 11	Enable A ; Enable B	TTL Compatible Enable Input ; the L state disables the bridge A (enable A) and/or the bridge B (enable B).
8	GND	Ground.
9	V_{SS}	Supply Voltage for the Logic Bloks. A 100 nF capacitor must be connected between this pin and ground.
10 ; 12	Input 3 ; Input 4	TTL Compatible Inputs of the Bridge B.
13 ; 14	Out 3 ; Out 4	Outputs of the Bridge B. The current that flows through the load connected between these two pins is monitored at pin 15.

ELECTRICAL CHARACTERISTICS (V_S = 42 V ; V_{SS} = 5 V, T_j = 25 °C ; unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_S	Supply Voltage (pin 4)	Operative Condition		V_{IH} + 2.5		46	V
V_{SS}	Logic Supply Voltage (pin 9)			4.5	5	7	V
I_S	Quiescent Supply Current (pin 4)	V_{en} = H I_L = 0	V_i = L		13	22	mA
			V_i = H		50	70	
		V_{en} = L	V_i = x			4	
I_{SS}	Quiescent Current from V_{SS} (pin 9)	V_{en} = H I_L = 0	V_i = L		24	36	mA
			V_i = H		7	12	
		V_{en} = L	V_i = x			6	
V_{iL}	Input Low Voltage (pins 5,7,10,12)			– 0.3		1.5	V
V_{iH}	Input High Voltage (pins 5,7,10,12)			2.3		V_{SS}	
I_{iL}	Low Voltage Input Current (pins 5,7,10,12)	V_i = L				– 10	µA
I_{iH}	High Voltage Input Current (pins 5,7,10,12)	V_i = H ≤ V_{SS} – 0.6 V			30	100	
V_{en} = L	Enable Low Voltage (pins 6,11)			– 0.3		1.5	V
V_{en} = H	Enable High Voltage (pins 6,11)			2.3		V_{SS}	
I_{en} = L	Low Voltage Enable Current (pins 6,11)	V_{en} = L				– 10	µA
I_{en} = H	High Voltage Enable Current (pins 6,11)	V_{en} = H ≤ V_{SS} – 0.6 V			30	100	
$V_{CE\ sat\ (H)}$	Source Saturation Voltage	I_L = 1 A			1.35	1.7	V
		I_L = 2 A			2	2.7	

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{CE\ sat\ (L)}$	Sink Saturation Voltage	I_L = 1 A (5)		1.2	1.6	V
		I_L = 2 A (5)		1.7	2.3	
$V_{CE\ sat}$	Total Drop	I_L = 1 A (5)			3.2	V
		I_L = 2 A (5)			4.9	
V_{sens}	Sensing Voltage (pins 1, 15)		− 1 (1)		2	V
T_1 (V_i)	Source Current Turn-off Delay	0.5 V_i to 0.9 I_L (2) ; (4)		1.5		µs
T_2 (V_i)	Source Current Fall Time	0.9 I_L to 0.1 I_L (2) ; (4)		0.2		µs
T_3 (V_i)	Source Current Turn-on Delay	0.5 V_i to 0.1 I_L (2) ; (4)		2		µs
T_4 (V_i)	Source Current Rise Time	0.1 I_L to 0.9 I_L (2) ; (4)		0.7		µs
T_5 (V_i)	Sink Current Turn-off Delay	0.5 V_i to 0.9 I_L (3) ; (4)		0.7		µs
T_6 (V_i)	Sink Current Fall Time	0.9 I_L to 0.1 I_L (3) ; (4)		0.25		µs
T_7 (V_i)	Sink Current Turn-on Delay	0.5 V_i to 0.9 I_L (3) ; (4)		1.6		µs
T_8 (V_i)	Sink Current Rise Time	0.1 I_L to 0.9 I_L (3) ; (4)		0.2		µs
f_c (V_i)	Commutation Frequency	I_L = 2 A		25	40	KHz
T_1 (V_{en})	Source Current Turn-off Delay	0.5 V_{en} to 0.9 I_L (2) ; (4)		3		µs
T_2 (V_{en})	Source Current Fall Time	0.9 I_L to 0.1 I_L (2) ; (4)		1		µs
T_3 (V_{en})	Source Current Turn-on Delay	0.5 V_{en} to 0.1 I_L (2) (4)		0.3		µs
T_4 (V_{en})	Source Current Rise Time	0.1 I_L to 0.9 I_L (2) ; (4)		0.4		µs
T_5 (V_{en})	Sink Current Turn-off Delay	0.5 V_{en} to 0.9 I_L (3) ; (4)		2.2		µs
T_6 (V_{en})	Sink Current Fall Time	0.9 I_L to 0.1 I_L (3) ; (4)		0.35		µs
T_7 (V_{en})	Sink Current Turn-on Delay	0.5 V_{en} to 0.1 I_L (3) ; (4)		0.25		µs
T_8 (V_{en})	Sink Current Rise Time	0.1 I_L to 0.9 I_L (3) ; (4)		0.1		µs
f_c (V_{en})	Commutation Frequency	I_L = 2 A		1		KHz

1) Sensing voltage can be −1 V for t ≤ 50 µsec; in steady state V_{sens} min ≥ − 0.5 V.
2) See fig. 2.
3) See fig. 4.
4) The load must be a pure resistor.
5) PIN 1 and PIN 15 connected to GND.

Figure 1 : Typical Saturation Voltage vs. Output Current.

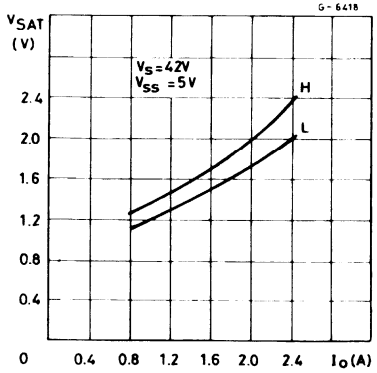
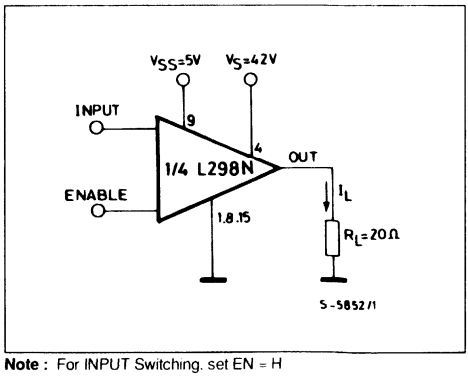


Figure 2 : Switching Times Test Circuits.



Note : For INPUT Switching, set EN = H
For ENABLE Switching, set IN = H

Figure 3 : Source Current Delay Times vs. Input or Enable Switching.

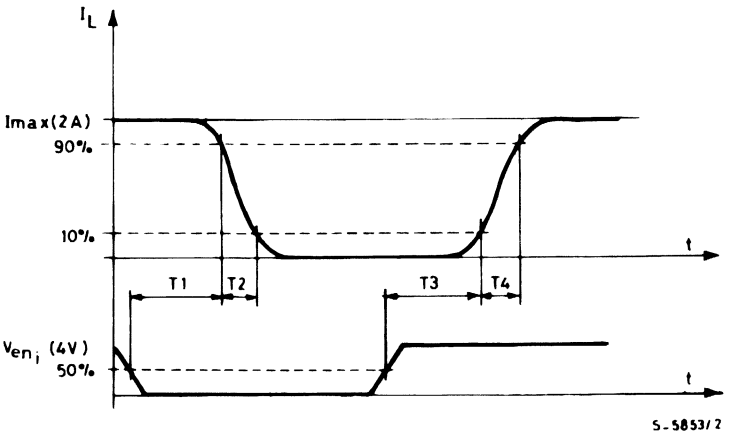
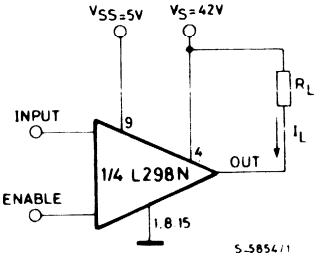


Figure 4 : Switching Times Test Circuits.



Note : For INPUT Switching, set EN = H
For ENABLE Switching, set IN = L

Figure 5 : Sink Current Delay Times vs. Input 0 V Enable Switching.

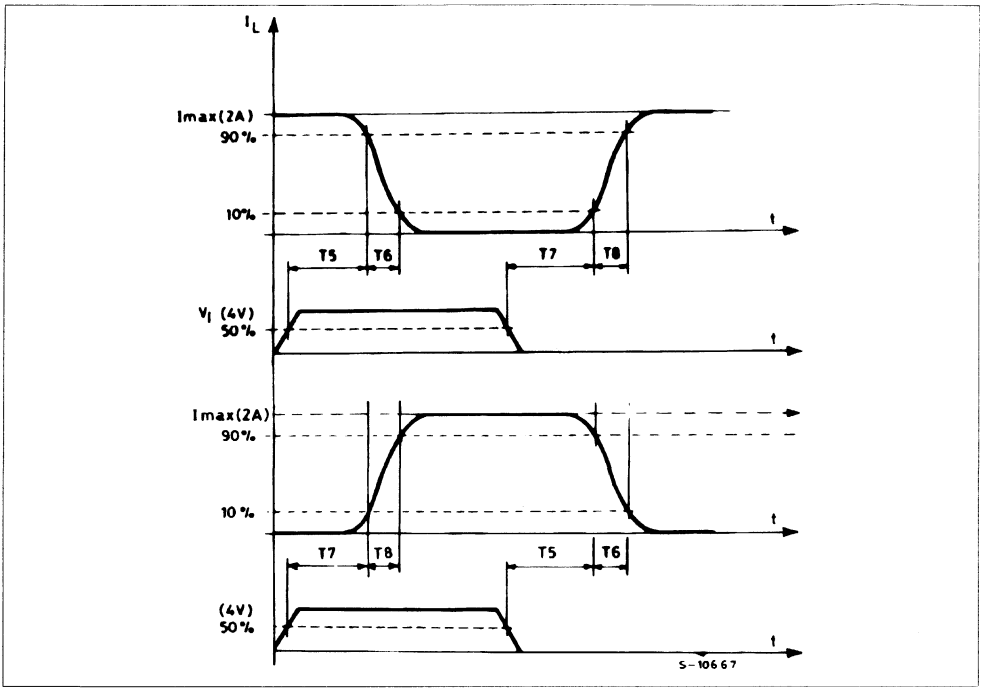
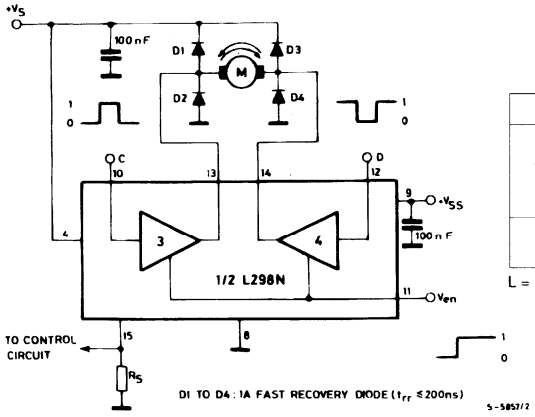


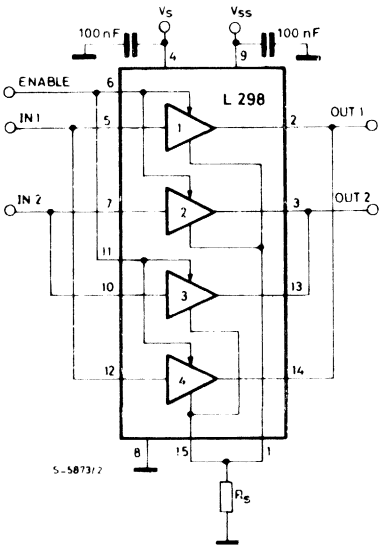
Figure 6 : Bidirectional DC Motor Control.



Inputs		Function
V_{en} = H	C = H ; D = L	Turn Right
	C = L ; D = H	Turn Left
	C = D	Fast Motor Stop
V_{en} = L	C = X ; D = C	Free Running Motor Stop

L = Low H = High X = Don't care

Figure 7 : For higher currents, outputs can be paralleled. Take care to parallel channel 1 with channel 4 and channel 2 with channel 3.



APPLICATION INFORMATION (Refer to the block diagram)

1.1. POWER OUTPUT STAGE

The L298N integrates two power output stages (A ; B). The power output stage is a bridge configuration and its outputs can drive an inductive load in common or differenzial mode, depending on the state of the inputs. The current that flows through the load comes out from the bridge at the sense output : an external resistor (R_{SA} ; R_{SB}.) allows to detect the intensity of this current.

1.2. INPUT STAGE

Each bridge is driven by means of four gates the input of which are In1 ; In2 ; EnA and In3 ; In4 ; EnB. The In inputs set the bridge state when The En input is high ; a low state of the En input inhibits the bridge. All the inputs are TTL compatible.

2. SUGGESTIONS

A non inductive capacitor, usually of 100 nF, must be foreseen between both Vs and Vss, to ground, as near as possible to pin 8 (GND). When the large capacitor of the power supply is too far from the IC, a second smaller one must be foreseen near the L298N.

The sense resistor, not of a wire wound type, must be grounded near the negative pole of Vs that must be near the GND pin of the I.C.

Each input must be connected to the source of the driving signals by means of a very short path.

Turn-On and Turn-Off : Before to Turn-ON the Supply Voltage and before to Turn it OFF, the Enable input must be driven to the Low state.

3. APPLICATIONS

Fig 6 shows a bidirectional DC motor control Schematic Diagram for which only one bridge is needed. The external bridge of diodes D1 to D4 is made by four fast recovery elements (trr $\leq$ 200 nsec) that must be chosen of a VF as low as possible at the worst case of the load current.

The sense output voltage can be used to control the current amplitude by chopping the inputs, or to provide overcurrent protection by switching low the enable input.

The brake function (Fast motor stop) requires that the Absolute Maximum Rating of 2 Amps must never be overcome.

When the repetitive peak current needed from the load is higher than 2 Amps, a paralleled configuration can be chosen (See Fig.7).

An external bridge of diodes are required when inductive loads are driven and when the inputs of the

IC are chopped ; Shottky diodes would be preferred.

This solution can drive until 3 Amps In DC operation and until 3.5 Amps of a repetitive peak current.

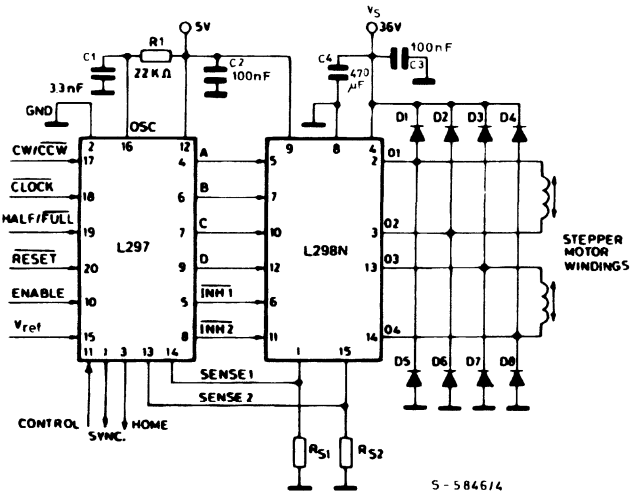
On Fig 8 it is shown the driving of a two phase bipolar stepper motor ; the needed signals to drive the inputs of the L298N are generated, in this example, from the IC L297.

Fig 9 shows an example of P.C.B. designed for the application of Fig 8.

Fig 10 shows a second two phase bipolar stepper motor control circuit where the current is controlled by the I.C. L6506.

Figure 8 : Two Phase Bipolar Stepper Motor Circuit.

This circuit drives bipolar stepper motors with winding currents up to 2 A. The diodes are fast 2 A types.



$R_{S1} = R_{S2} = 0.5\ \Omega$

D1 to D8 = 2 A Fast diodes { $V_F \leq 1.2$ V @ I = 2 A ; trr ≤ 200 ns

Figure 9: Suggested Printer Circuit Board Layout for the Circuit of fig. 8 (1 : 1 scale)

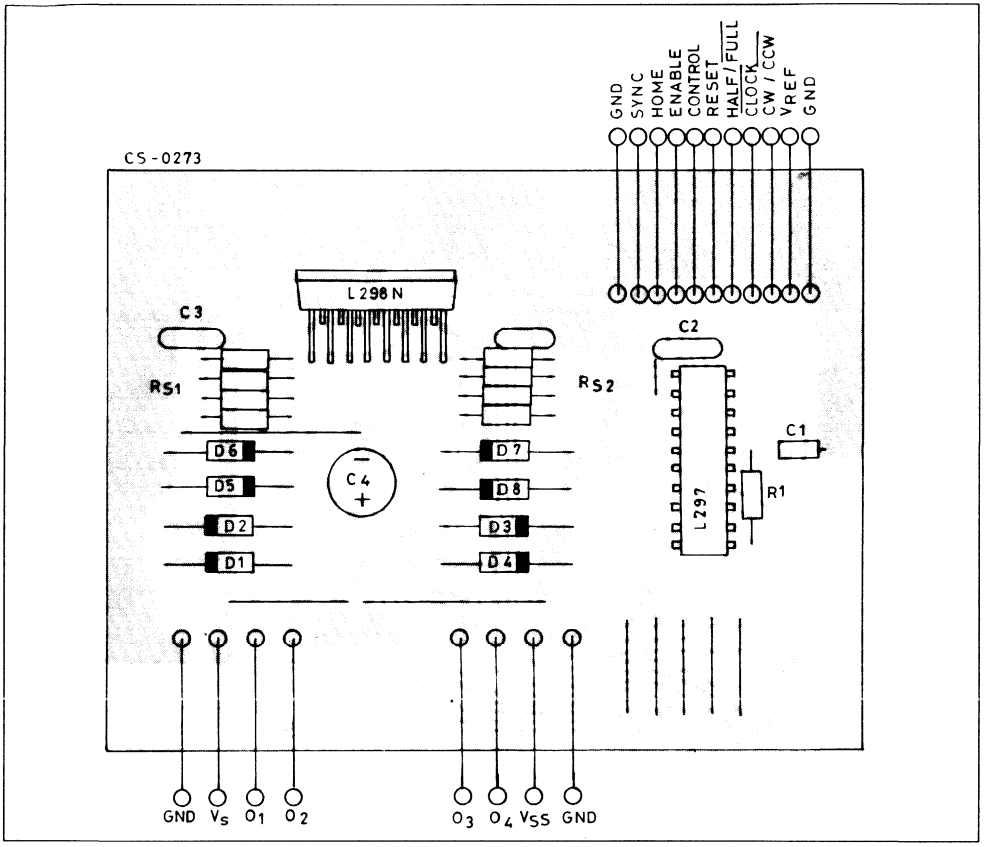
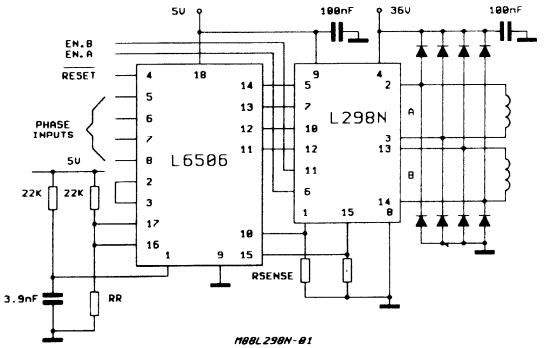


Figure 10: Two Phase Bipolar Stepper Motor Control Circuit by Using the Current Controller L6506.



R_R and R_{sense} depend from the load current

SGS-THOMSON MICROELECTRONICS

L601-L603
L602-L604

DARLINGTON ARRAYS

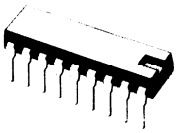
- EIGHT DARLINGTONS PER PACKAGE
- OUTPUT CURRENT 400 mA PER DRIVER (500 mA PEAK)
- OUTPUT VOLTAGE 90 V ($V_{CE\ (sus)}$ = 70 V)
- INTEGRAL SUPPRESSION DIODES FOR INDUCTIVE LOADS
- OUTPUTS CAN BE PARALLELED FOR HIGHER CURRENT
- TTL / CMOS / PMOS / DTL COMPATIBLE INPUTS
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY LAYOUT

The four versions interface to all common logic families :

L601	General purpose
L602	14 - 25 V PMOS
L603	5 V TTL, CMOS
L604	6 - 15 V CMOS, PMOS

These versatile devices are useful for driving a wide range of loads, including solenoids, relays DC motors, LED displays, filament lamps, thermal printheads and high power buffers.

The L601, L602, L603 and L604 are supplied in 18 pin plastic DIP packages with a copper leadframe to reduce thermal resistance.



DIP-18
(Plastic)

ORDER CODES : L601C L603C
L602C L604C

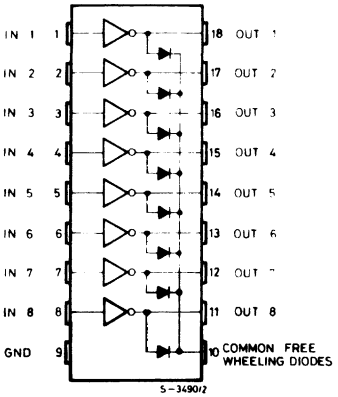
DESCRIPTION

The L601, L602, L603 and L604 are high voltage, high current darlington arrays each containing eight open collector darlington pairs with common emitters. Each channel is rated at 400 mA and can with stand peak currents of 500 mA. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout.

ABSOLUTE MAXIMUM RATINGS

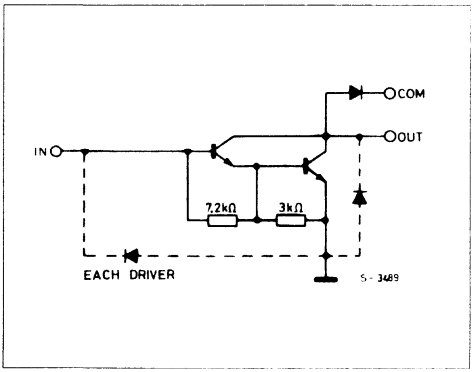
Symbol	Parameter	Value	Unit
V_{CEX}	Collector Emitter Voltage (input open)	90	V
I_C	Collector Current	0.4	A
I_C	Collector Peak Current	0.5	A
V_i	Input Voltage (for L602, L603 and L604)	30	V
I_i	Input Current (for L601 only)	25	mA
P_{tot}	Total Power Dissipation a T_{amb} = 25°C	1.8	W
T_{op}	Operating Junction Temperature	– 25 to 150	°C

PIN CONNECTIONS (top view)

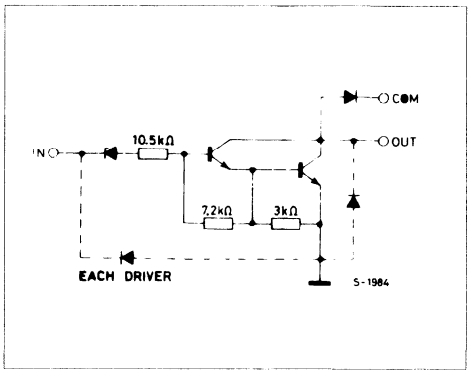


SCHEMATIC DIAGRAMS

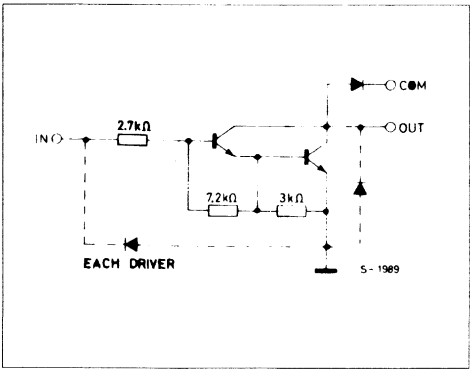
L601



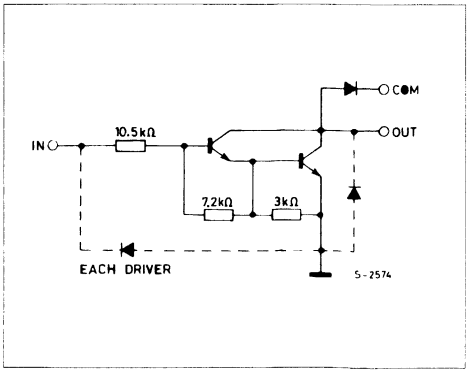
L602



L603



L604



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	70	C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 C, unless otherwise specified)

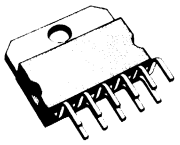
Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
I_{CEX}	Output Leakage Current	V_{CE} = 90 V				10	µA
$V_{CE(sat)}$	Collector Emitter Saturation Voltage	I_C = 300 mA	I_B = 500 µA			2	V
		I_C = 200 mA	I_B = 350 µA			1.7	V
		I_C = 100 mA	I_B = 250 µA			1.2	V
h_{FE}	DC Forward Current Gain (L601 only)	V_{CE} = 3 V	I_C = 300 mA	1000			–
V_i	Minimum Input Voltage (ON condition)	V_{CE} = 3 V	I_C = 300 mA				
		for L602				11.5	V
		for L603				2.5	V
		for L604				5	V
V_i	Maximum Input Voltage (OFF condition)	V_{CE} = 90 V	I_C = 25 µA				
		for L601		0.55			V
		for L602		7			V
		for L603		0.75			V
		for L604		1			V
I_R	Clamp Diode Reverse Current	V_R = 90 V				50	µA
V_F	Clamp Diode Forward Voltage	I_F = 300 mA			2	2.4	V
t_{on}	Turn-on Delay	0.5 V_i to 0.5 V_o			0.4		µs
t_{off}	Turn off Delay	0.5 V_i to 0.5 V_o			0.4		µs

SGS-THOMSON MICROELECTRONICS

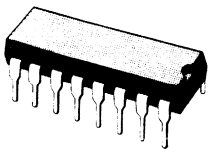
L702

2A QUAD DARLINGTON SWITCH

- SUSTAINING VOLTAGE : 70 V
- 2 A OUTPUT
- HIGH CURRENT GAIN
- IDEAL FOR DRIVING SOLENOIDS, DC MOTORS, STEPPER MOTORS, RELAYS, DISPLAYS, ETC.



Multiwatt-11



Powerdip 8 + 8

ORDER CODES : L702B - Powerdip
L702N - Multiwatt

DESCRIPTION

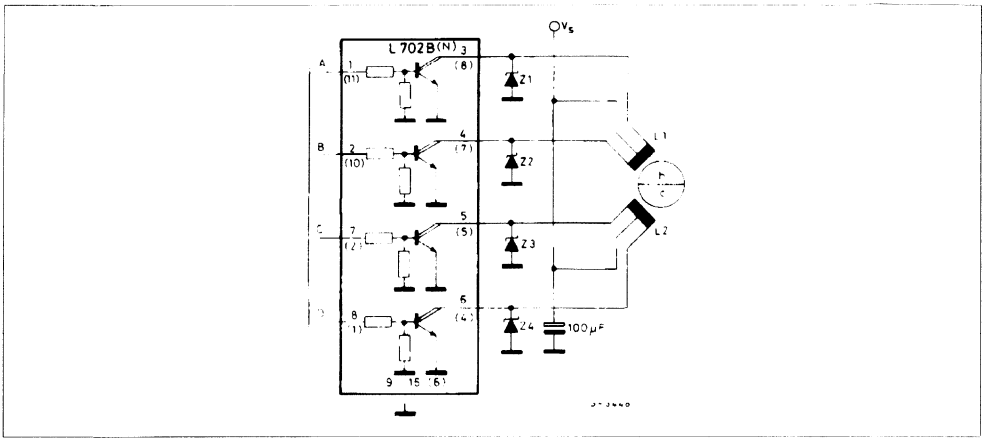
The L702 is a monolithic integrated circuit for high current and high voltage switching applications. It comprises four darlington transistors with common emitter and open collector suitable for current sinking applications mounted on the new POWERDIP and Multiwatt® packages.

This circuit reduces components, sizes and costs ; it can provide direct interface between low level logic and a variety of high current applications.

ABSOLUTE MAXIMUM RATINGS

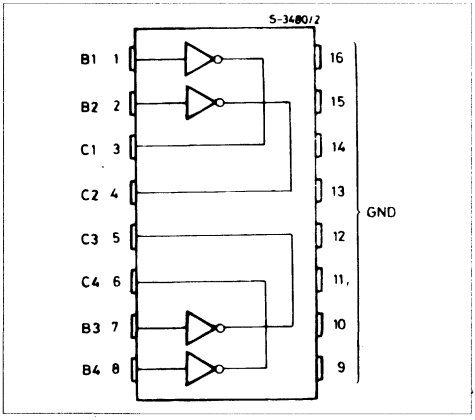
Symbol	Parameter		Value	Unit
V_{CEx}	Collector-emitter Voltage (input open)		90	V
V_i	Input Voltage		30	V
I_C	Collector Current		3	A
P_{tot}	Total Power Dissipation at T_{pin} 9 to 16 ≤ 90 °C	Powerdip	4	W
	Total Power Dissipation at T_{amb} ≤ 70 °C	Powerdip	1.1	W
	Total Power Dissipation at T_{case} ≤ 90 °C	Multiwatt	20	W
T_{stg}	Storage Temperature		– 55 to 150	°C
T_j	Operating Junction Temperature		– 25 to 150	°C

STEPPING MOTOR BUFFER

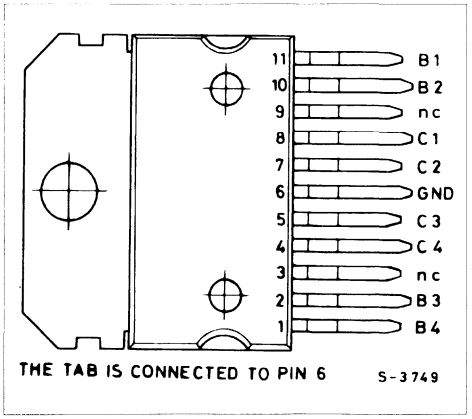


CONNECTION DIAGRAMS (top view)

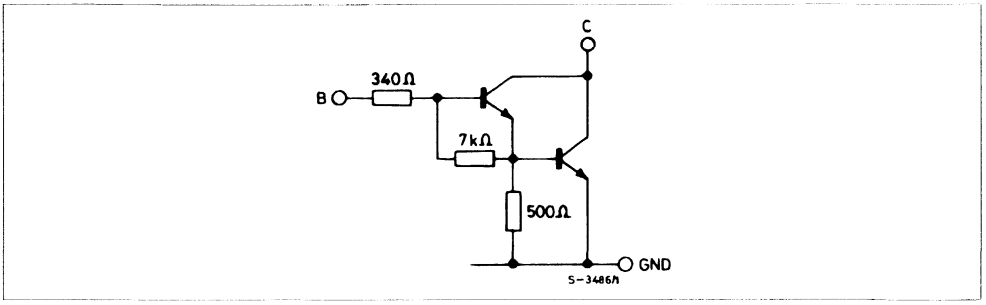
Powerdip



Multiwatt



SCHEMATIC DIAGRAM (each Darlington)



THERMAL DATA

$R_{th\ j\ amb}$	Thermal Resistance Junction Ambient	} Powerdip	Max	70	C/W
$R_{th\ j\ pins\ 9\ 16}$	Thermal Resistance Junction Pins 9 to 16	} Powerdip	Max	14	C/W
$R_{th\ j\ case}$	Thermal Resistance Junction-case	Multiwatt	Max	3	C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

Symbol	Parameter		Test conditions		Min.	Typ.	Max.	Unit
I_{CEX}	Output Leakage Current		V_{CE} = 90 V			10	50	μA
$V_{CE(sust)}$	Collector Emitter ( ) Sustaining Voltage		I_C = 100 mA		70			V
$V_{CE(sat)}$	Collector Emitter Saturation Voltage		I_C = 1.25 A I_i = 2 mA			1.3	1.9	V
h_{FE}	DC Forward Current Gain		I_C = 1 A V_{CE} = 3 V		1 000	4 000		
I_i	Input Current		V_i = 3.75 V V_i = 2.4 V Open Collector			7 3	11 6	mA mA
V_i	Input Voltage	Off Condition	V_{CE} = 70 V	$I_C \leq$ 0.1 mA			0.4	V
		On Condition	V_{CE} = 3 V	$I_C \geq$ 1 A	2.4			V
T_{on}	Turn On Time		V_s = 12 V			0.3		μs
T_{off}	Turn Off Time		R_L = 10 Ω			1		μs

Figure 1 : Switching Time.

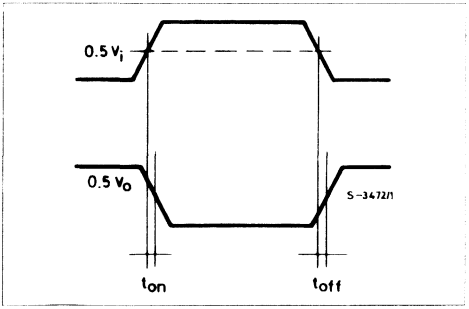


Figure 2 : t_{on} and t_{off} Test Circuit.

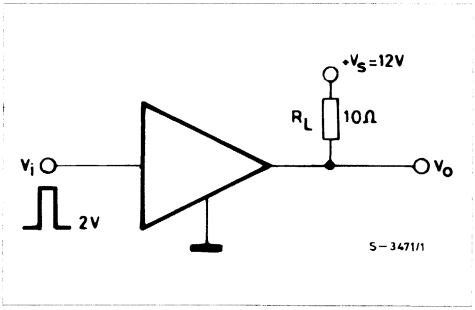


Figure 3 : Peak Collector Current vs. Duty Cycle and Number of Outputs (L702B only).

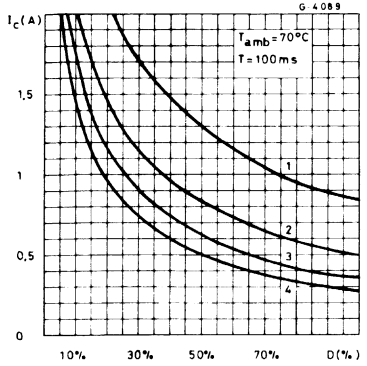


Figure 4 : Collector Emitter Saturation Voltage vs. Collector Current.

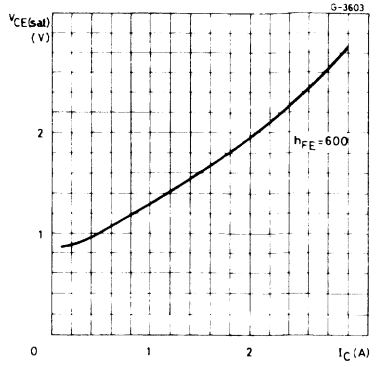


Figure 5 : Collector Current vs. Input Voltage.

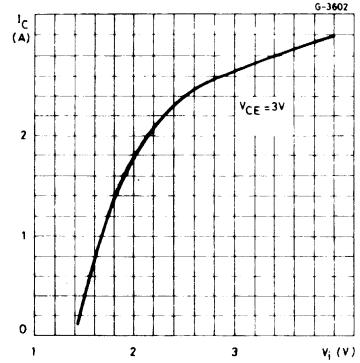


Figure 6 : Input Current vs. Input Voltage.

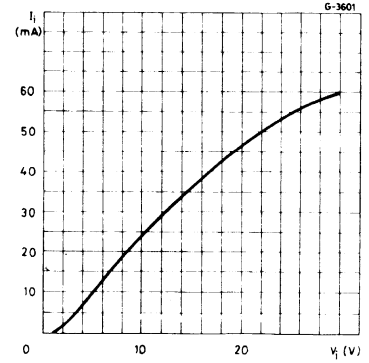


Figure 7 : Safe Operating Areas (L702B).

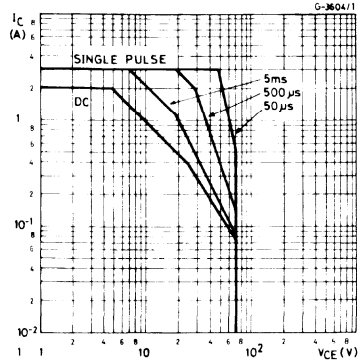
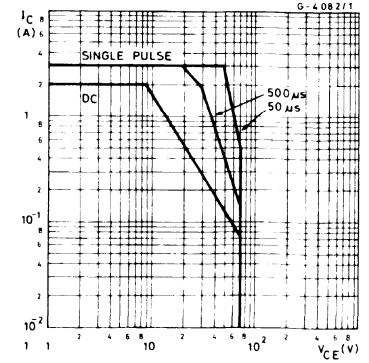


Figure 8 : Safe Operating Areas (L702N).



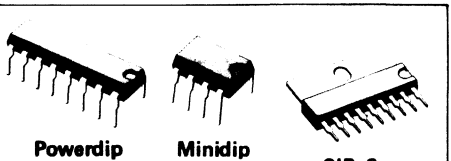
LOW DROP DUAL POWER OPERATIONAL AMPLIFIERS

- OUTPUT CURRENT TO 1A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGE
- LOW INPUT OFFSET VOLTAGE
- GROUND COMPATIBLE INPUTS
- LOW SATURATION VOLTAGE
- THERMAL SHUTDOWN
- CLAMP DIODE
- ESD PROTECTION
- DUMP PROTECTION

The L2720, L2722 and L2724 are monolithic integrated circuits in powerdip, minidip and SIP-9 packages, intended for use as power operational amplifiers in a wide range of applications including servo amplifiers and power supplies.

They are particularly indicated for driving, inductive loads, as motor and finds applications in compact-disc VCR automotive, etc.

The high gain and high output power capability provide superior performance whatever an operational amplifier/power booster combination is required.



Powerdip (8 + 8) | **Minidip Plastic** | **SIP-9**

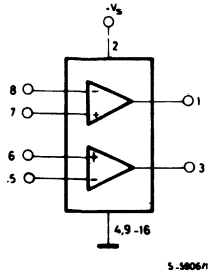
ORDERING NUMBERS:

L2720 L2722 L2724

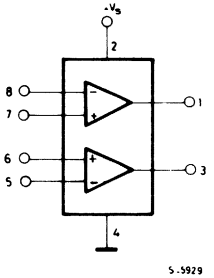
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply voltage	28	V
V_s	Peak supply voltage (50ms)	50	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	$\pm V_s$	
I_o	DC Output current	1	A
I_p	Peak output current (non repetitive)	1.5	A
P_{tot}	Power dissipation at T_{amb} = 80°C **(L2720)**, T_{amb} = 50°C **(L2722)**	1	W
	T_{case} = 75°C **(L2720)**	5	W
	T_{case} = 50°C **(L2724)**	10	W
T_{op}	Operating Temperature	−40 to 85	°C
T_{stg}, T_j	Storage and junction temperature	−40 to 150	°C

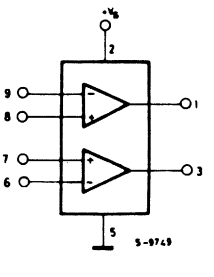
BLOCK DIAGRAMS



L2720

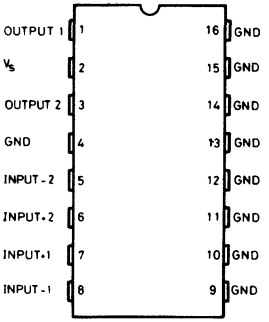


L2722

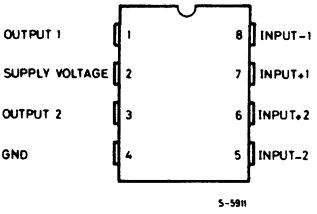


L2724

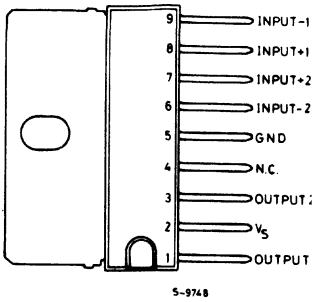
CONNECTION DIAGRAMS
(Top view)



L2720

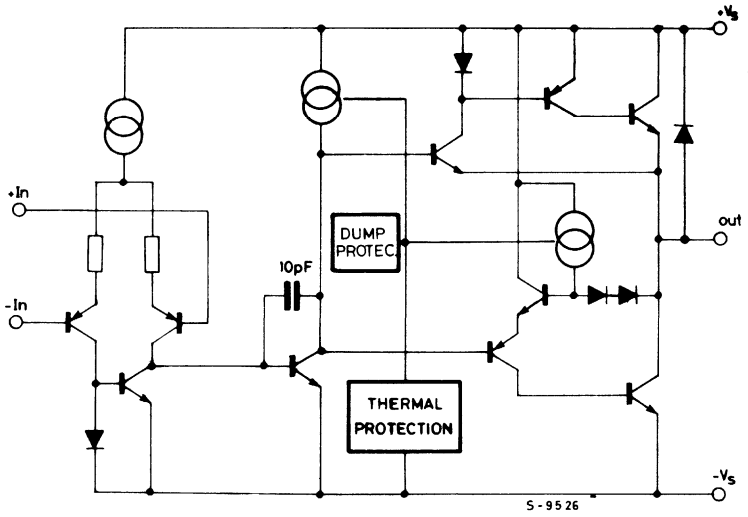


L2722



L2724

SCHEMATIC DIAGRAM (one section)



THERMAL DATA

			SIP-9	Powerdip	Minidip
$R_{th\ j\text{-}case}$	Thermal resistance junction-pins	max	10°C/W	15°C/W	*70°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-albient	max	70°C/W	70°C/W	100°C/W

* Thermal resistance junction-pin 4.

ELECTRICAL CHARACTERISTICS (V_s = 24V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_s	Single supply voltage			4		28	V
V_s	Split supply voltage			± 2		± 14	V
I_s	Quiescent drain current	$V_o = \frac{V_s}{2}$	V_s = 24V		10	15	mA
			V_s = 8V		9	15	mA
I_b	Input bias current				0.2	1	µA
V_{os}	Input offset voltage					10	mV
I_{os}	Input offset current					100	nA
SR	Slew rate				2		V/µs
B	Gain-bandwidth product				1.2		MHz
R_i	Input resistance			500			KΩ
G_v	O.L. voltage gain	f = 100Hz		70	80		dB
		f = 1KHz			60		dB
e_N	Input noise voltage	B = 22Hz to 22KHz			10		µV
I_N	Input noise current				200		pA
CMR	Common Mode rejection	f = 1KHz		66	84		dB
SVR	Supply voltage rejection	f = 100Hz R_G = 10KΩ V_R = 0.5V	V_s = 24V V_s = ±12V V_s = ± 6V	60	70 75 80		dB dB dB
$V_{DROP\ (HIGH)}$		V_s = ±2.5V to ± 12V	I_p = 100mA		0.7		V
			I_p = 500mA		1.0	1.5	V
$V_{DROP\ (LOW)}$			I_p = 100mA		0.3		V
			I_p = 500mA		0.5	1.0	V
C_s	Channel separation	f = 1KHz R_L = 10Ω G_v = 30dB	V_s = 24V		60		dB
			V_s = 6V		60		dB
T_{sd}	Thermal shutdown junction temperature				145		°C

Fig. 1 - Quiescent current vs. supply voltage

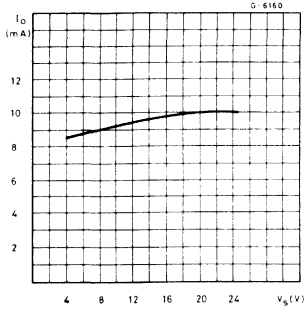


Fig. 2 - Open loop gain vs. frequency

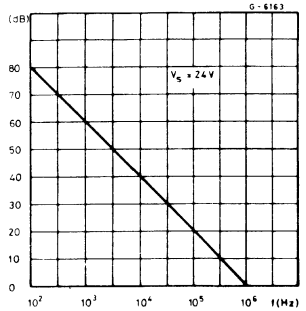


Fig. 3 - Common mode rejection vs. frequency

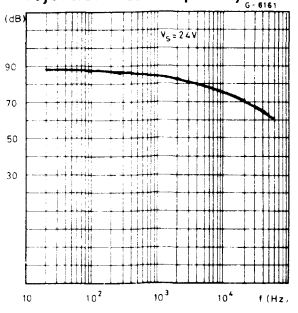


Fig. 4 - Output swing vs. load current (V_s = ± 5V)

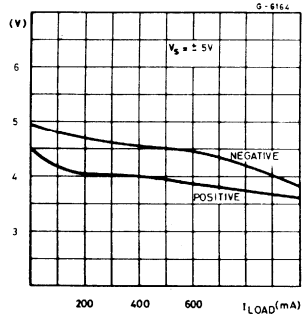


Fig. 5 - Output swing vs. load current (V_s = ± 12V)

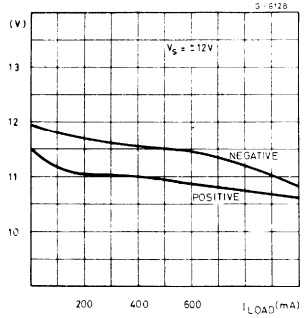


Fig. 6 - Supply voltage rejection vs. frequency

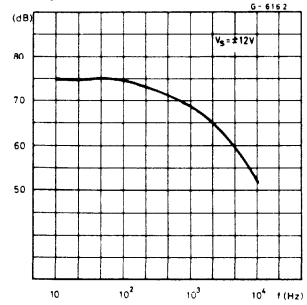
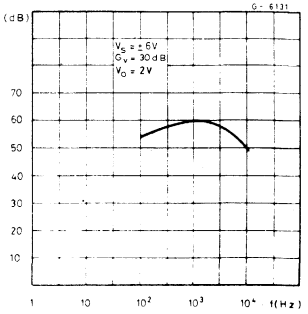


Fig. 7 - Channel separation vs. frequency

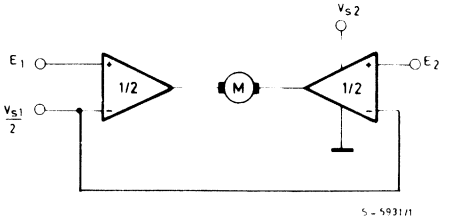


APPLICATION SUGGESTION

In order to avoid possible instability occurring into final stage the usual suggestions for the linear power stages are useful, as for instance:

- layout accuracy;
- A 100nF capacitor connected between supply pins and ground;
- boucherot cell (0.1 to 0.2 μF + 1Ω series) between outputs and ground or across the load. With single supply operation, a resistor (1KΩ) between the output and supply pin can be necessary for stability.

Fig. 8 - Bidirectional DC motor control with μP compatible inputs



V_{S1} = logic supply voltage

Must be $V_{S2} > V_{S1}$

E1, E2 = logic inputs

Fig. 9 - Servocontrol for compact-disc

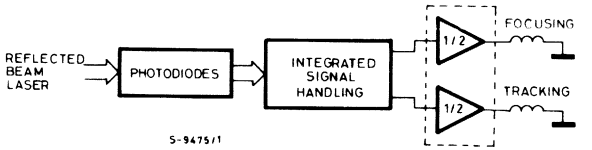


Fig. 10 - Capstan motor control in video recorders

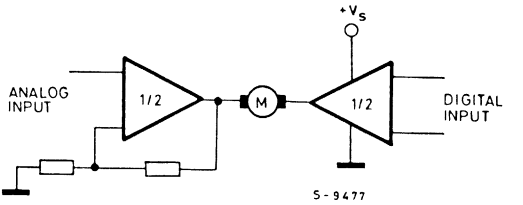
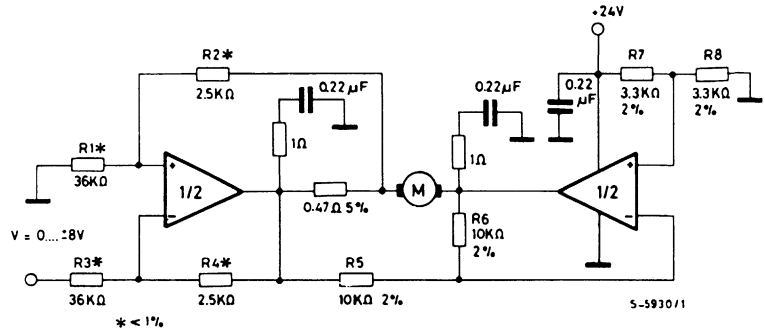


Fig. 11 - Motor current control circuit



Note: The input voltage level is compatible with L291 (5-BIT D/A converter)

Fig. 12 - Bidirectional speed control of DC motors.

For circuit stability ensure that $R_X > \frac{2R3 \circ R1}{R_M}$ where R_M = internal resistance of motor. The voltage available at the terminals of the motor is $V_M = 2\,(V_I - \frac{V_s}{2}) + |R_o|.\ I_M$ where $|R_o| = \frac{2R3 \circ R1}{R_X}$ and I_M is the motor current.

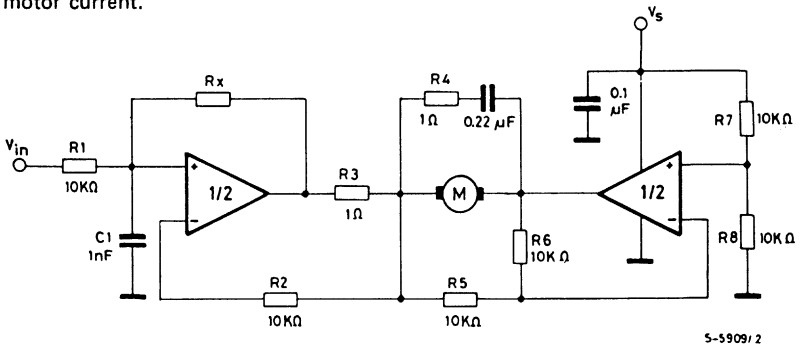
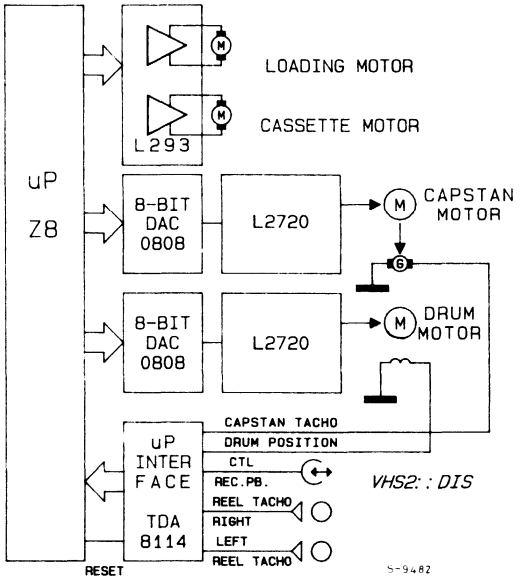


Fig. 13 - VHS-VCR Motor control circuit



SGS-THOMSON MICROELECTRONICS

L2726

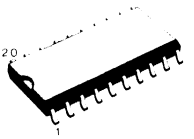
LOW DROP DUAL POWER OPERATIONAL AMPLIFIER

- OUTPUT CURRENT TO 1A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGE
- LOW INPUT OFFSET VOLTAGE
- GROUND COMPATIBLE INPUTS
- LOW SATURATION VOLTAGE
- THERMAL SHUTDOWN
- CLAMP DIODE
- ESD PROTECTION
- DUMP PROTECTION

The L2726 is a monolithic integrated circuit in SO-20 package intended for use as power operational amplifiers in a wide range of applications including servo amplifiers and power supplies.

It is particularly indicated for driving inductive loads, as motor and finds applications in compact-disc VCR automotive, etc.

The high gain and high output power capability provide superior performance whatever an operational amplifier/power booster combination is required.



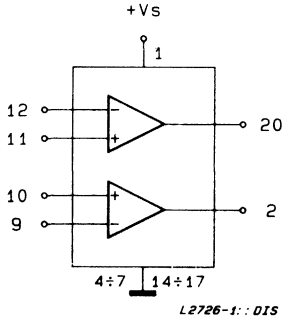
SO-20
(12 + 4 + 4)

ORDER NUMBER: L2726

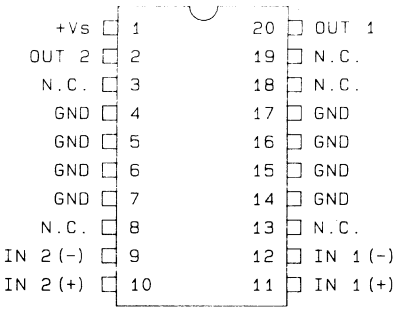
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply voltage	28	V
V_s	Peak supply voltage (50ms)	50	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	$\pm V_s$	
I_o	DC Output current	1	A
I_p	Peak output current (non repetitive)	1.5	A
P_{tot}	Power dissipation at T_{amb} = 85°C T_{case} = 75°C	1 5	W W
T_{op}	Operating Temperature	−40 to 85	°C
T_{stg}, T_j	Storage and junction temperature	−40 to 150	°C

BLOCK DIAGRAM

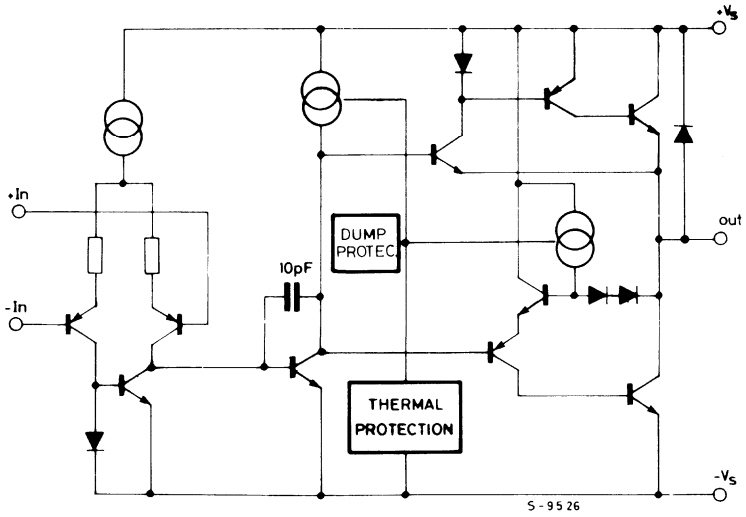


CONNECTION DIAGRAM
(Top view)



L2726-2: : DIS

SCHEMATIC DIAGRAM (one section)



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	15.0	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient (*)	max	65	°C/W

(*) With 4 sq. cm copper area heatsink

ELECTRICAL CHARACTERISTICS (V_s = 24V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_s	Single supply voltage			4		28	V
V_s	Split supply voltage			± 2		± 14	V
I_s	Quiescent drain current	$V_O = \frac{V_s}{2}$	V_s = 24V		10	15	mA
			V_s = 8V		9	15	mA
I_b	Input bias current				0.2	1	µA
V_{os}	Input offset voltage					10	mV
I_{os}	Input offset current					100	nA
SR	Slew rate				2		V/µs
B	Gain-bandwidth product				1.2		MHz
R_i	Input resistance			500			KΩ
G_v	O.L. voltage gain	f = 100Hz		70	80		dB
		f = 1KHz			60		dB
e_N	Input noise voltage	B = 22Hz to 22KHz			10		µV
I_N	Input noise current	B = 22Hz to 22KHz			200		pA
CMR	Common Mode rejection	f = 1KHz		66	84		dB
SVR	Supply voltage rejection	f = 100Hz R_G = 10KΩ V_R = 0.5V	V_s = 24V V_s = ±12V V_s = ± 6V	60	70 75 80		dB dB dB
$V_{DROP\ (HIGH)}$		V_s = ±2.5V to ±12V	I_p = 100mA		0.7		V
			I_p = 500mA		1.0	1.5	V
$V_{DROP\ (LOW)}$			I_p = 100mA		0.3		V
			I_p = 500mA		0.5	1.0	V
C_s	Channel separation	f = 1KHz R_L = 10Ω G_v = 30dB	V_s = 24V		60		dB
			V_s = 6V		60		dB
T_{sd}	Thermal shutdown junction temperature				145		°C

Fig. 1 - Quiescent current vs. supply voltage

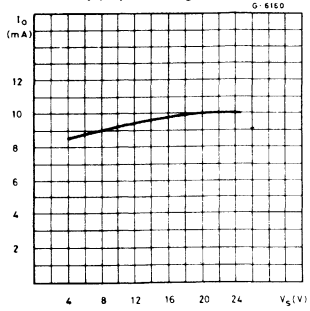


Fig. 2 - Open loop gain vs. frequency

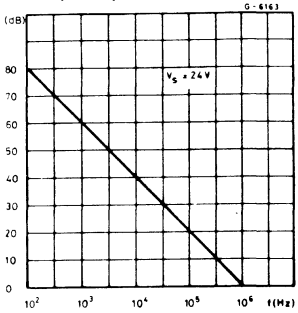


Fig. 3 - Common mode rejection vs. frequency

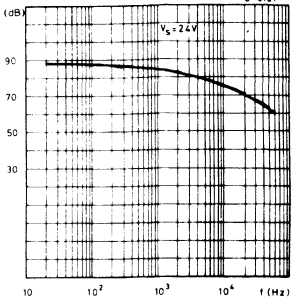


Fig. 4 - Output swing vs. load current (V_S = ± 5V)

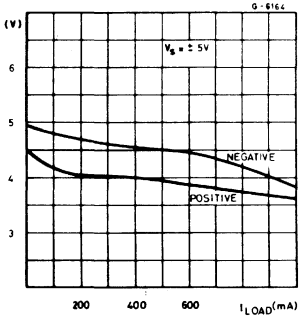


Fig. 5 - Output swing vs load current (V_S = ± 12V)

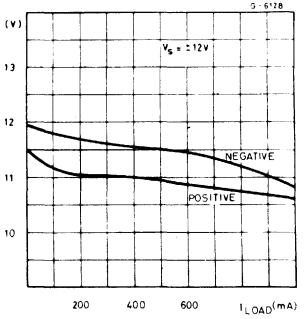


Fig. 6 - Supply voltage rejection vs. frequency

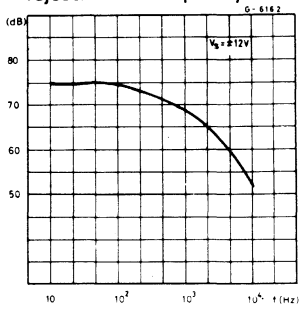
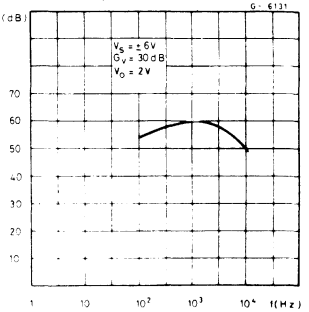


Fig. 7 - Channel separation vs. frequency



SGS-THOMSON MICROELECTRONICS

L2750

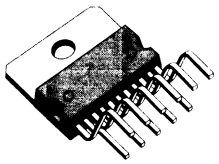
DUAL LOW DROP HIGH POWER OPERATIONAL AMPLIFIER

ADVANCE DATA

- HIGH OUTPUT CURRENT
- VERY LOW SATURATION VOLTAGE
- LOW VOLTAGE OPERATION
- LOW INPUT OFFSET VOLTAGE
- GND COMPATIBLE INPUTS
- ST-BY FUNCTION (LOW CONSUMPTION)
- HIGH APPLICATION FLEXIBILITY

PROTECTIONS:

- VERY INDUCTIVE LOADS
- OVERRATING CHIP TEMPERATURE
- LOAD DUMP VOLTAGE
- FORTUITOUS OPEN GROUND
- ESD



Multiwatt-11

ORDERING NUMBER: L2750

DESCRIPTION

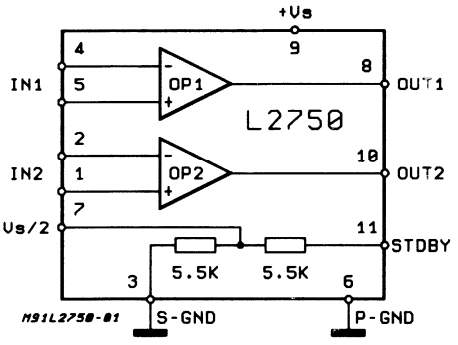
The L2750 is a new technology class AB dual power operational amplifier assembled in Multiwatt 11 package.

Thanks to the fully complementary PNP/NPN output configuration the L2750 can deliver a rail-to-rail output voltage swing even at the highest current.

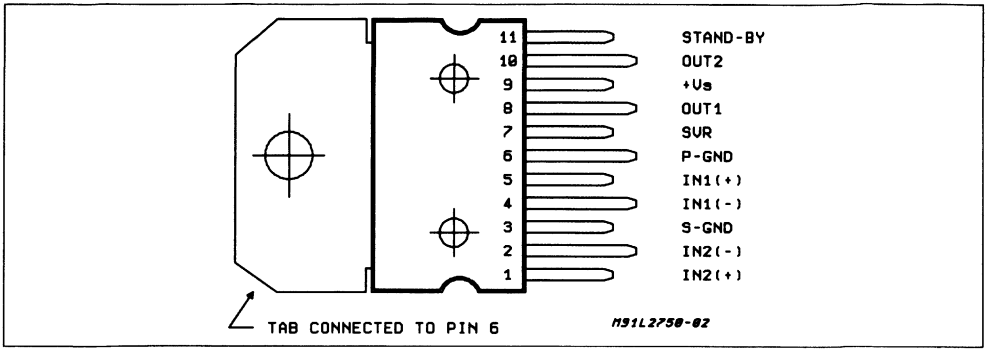
Additional feature is the very low current Stand-By function.

The high application flexibility of the L2750 makes the device suitable for either motor driving/control and audio applications purposes.

BLOCK DIAGRAM



PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{S\ op}$	Operating Supply Voltage	18	V
$V_{S\ max}$	Supply Voltage	28	V
V_{PEAK}	Peak Supply Voltage (t = 50ms)	40	V
V_i	Input Voltage	$V_{S\ op}$	V
V_i	Differential Input Voltage	$V_{S\ op}$	V
I_O	Output Peak Current (non rep. t = 100µs)	5	A
I_O	Output Peak Current (rep. f > 10Hz)	4	A
P_{tot}	Power Dissipation T_{CASE} = 85°C	36	W
T_{stg}, T_j	Storage and Junction Temperature	-40 to 150	°C

THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	1.8	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the operational amplifier with G_V = 24dB; V_S = 14.4V; T_{amb} = 25°C, unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		4		18	V
I_d	Total Quiescent Drain Current			30	50	mA
V_{OS}	Input Offset Voltage				5	mV
I_{SB}	ST-BY Current Consumption				50	µA
I_S	Input Bias Current				0.5	µA
I_{OS}	Input Offset Current				50	nA
V_{DROP}	Output Voltage Drop (High)	I_O = 0.5A I_O = 3A		0.25 1.1	0.5 2.5	V V
	Output Voltage Drop (Low)	I_O = 0.5A I_O = 3A		0.25 1	0.5 2	V V
SR	Slew Rate			4		V/µs
B	Gain Bandwidth Prod			10		MHz
G_V	Open Loop Voltage Gain	f = 1KHz		85		dB
R_{IN}	Input Resistance			150		MΩ
E_{IN}	Input Noise Voltage	R_s = 0 to 10KΩ f = 22Hz to 22KHz		3		µV
CMRR	Common Mode Rejection Ratio		75	90		dB

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SVR	Supply Voltage Rejection	R_S = 0 f = 100Hz	75	90		dB
C_T	Crosstalk	f = 1KHz to 10KHz		80		dB

APPLICATION SUGGESTION

The high flexibility makes the L2750 suitable for a wide range of applications.

Motor Controller

The device can be utilized as a motor controller. Fig.1 represents a bidirectional DC motor control suitable for logic driving. In these kinds of application it is possible to take advantage of the high current capability of the L2750 for driving several types of low impedance motors in a broad range of applications. Moreover the low drop allows high start up currents even at lowest supply voltage.

Audio Applications

Another typical utilization of the L2750 concerns the audio field, as follows:

1) DRIVER FOR BOOSTER : The remarkably low distortion and noise makes the device proper to be used as high quality driver for main amplifiers (i.e. car radio boosters). An example is shown by Fig. 5, where the gain is set to 24 dB (see also the relevant characteristics).

2) CAR RADIO BOOSTER WITH DIFFERENTIAL INPUT : Fig. 10 shows an example of car radio booster, with a gain of 30 dB, that is specially recommended for active loudspeakers. Among its main feature is the differential input and subsequent high noise suppression. The typical output power delivered into a 4Ω load is 24W (V_S = 14.4V; d =10%), as shown by the characteristics enclosed.

Figure 1

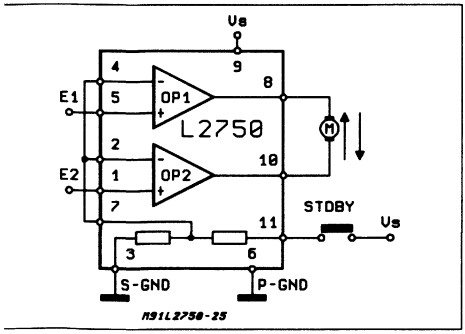


Figure 2: Low Drop Voltage vs. Output Current

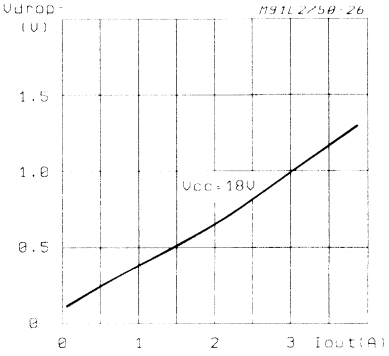


Figure 3: High Drop Voltage vs. Output Current

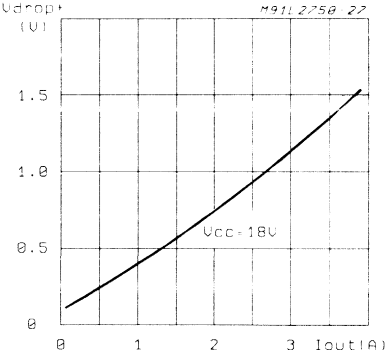


Figure 4: Open Loop Gain vs. Phase Response

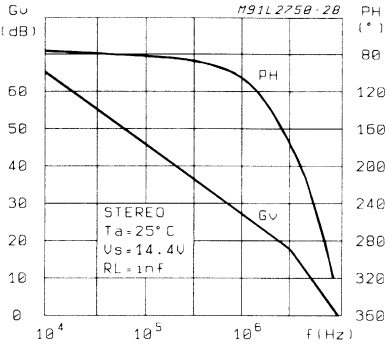


Figure 5: Stereo Audio Amplifier Application Circuit

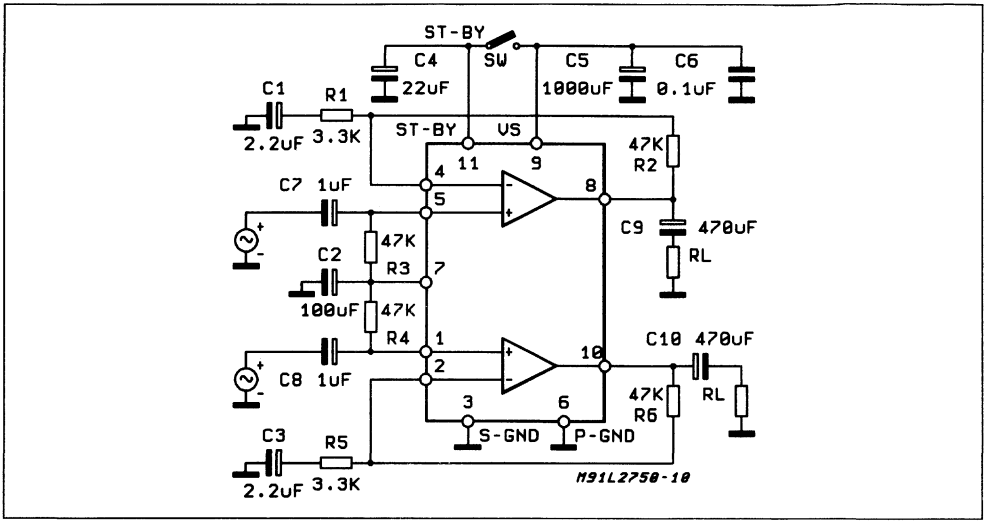
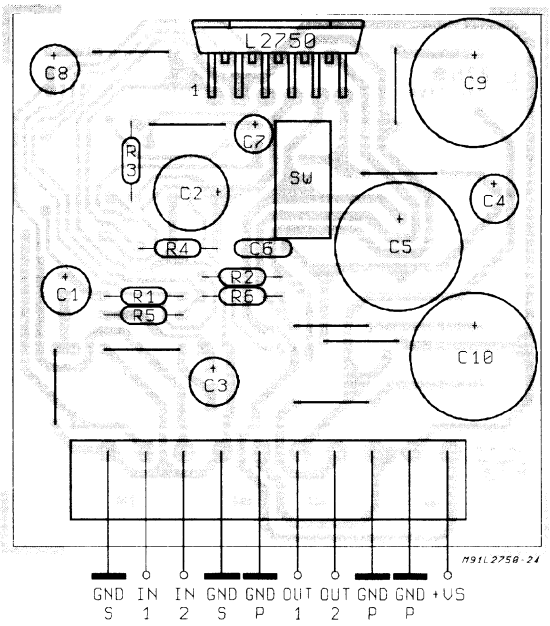


Figure 6: P.C. Board and Components Layout of the Circuit of Figure 5 (1:1 scale)



AUDIO STEREO APPLICATION CIRCUIT OF FIGURE 5

Figure 7: Quiescent Drain Current vs. Supply Voltage

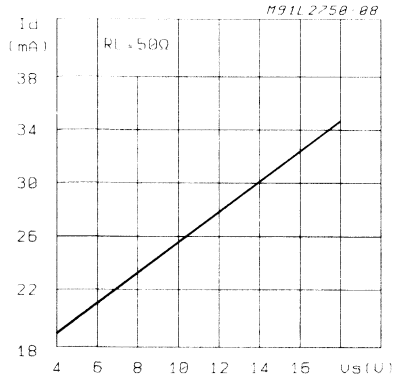


Figure 8: Distortion vs. Output Voltage

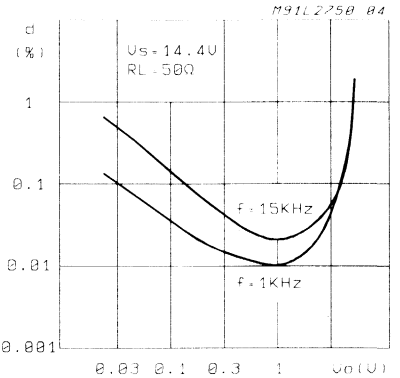


Figure 9: Distortion vs. Frequency

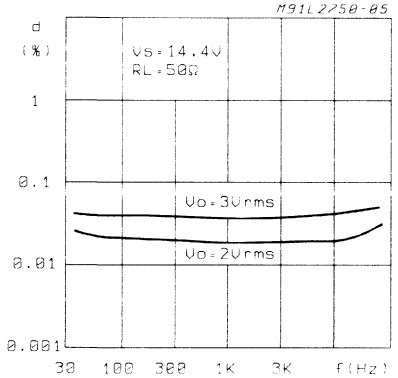


Figure 10: Cross-Talk vs Frequency

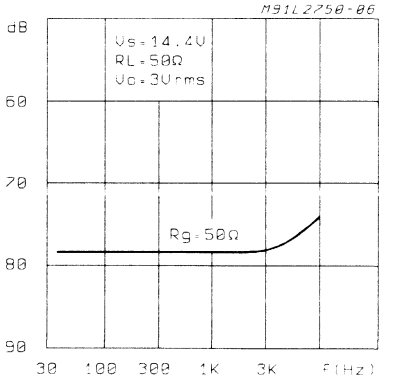


Figure 11: Supply Voltage Rejection vs. Frequency

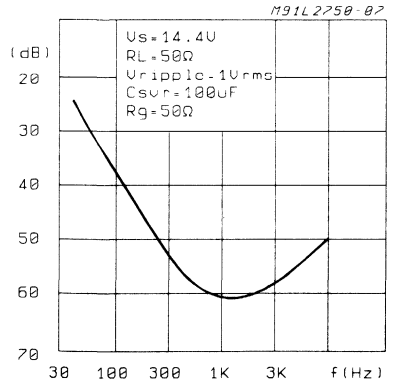


Figure 12: E_N Input vs. R_g

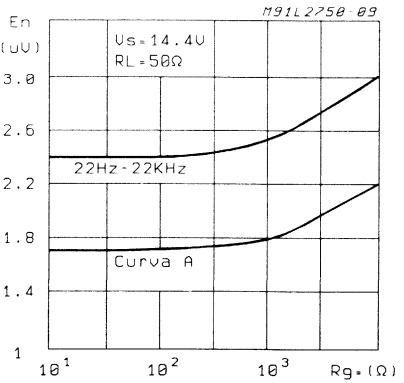


Figure 13: Bridge Power Amplifier with Balanced Input Application Circuit

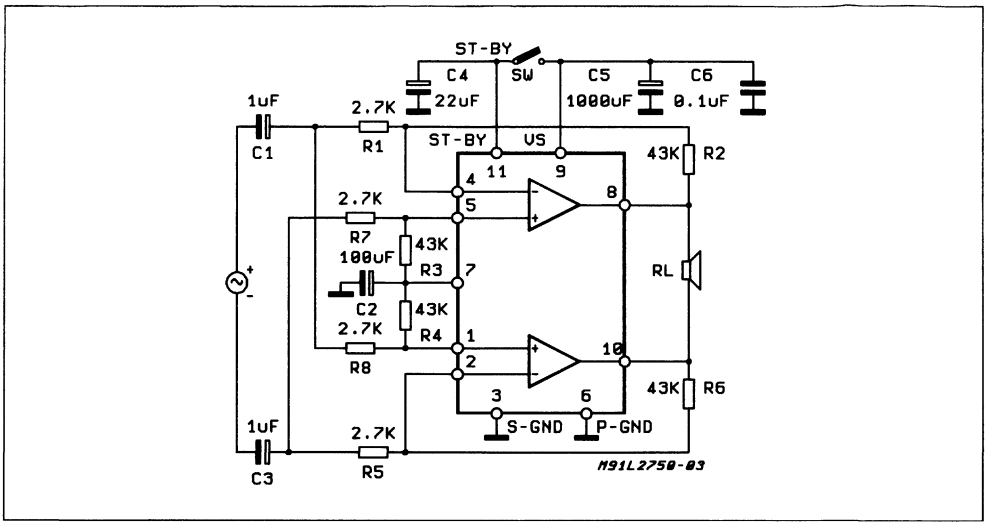
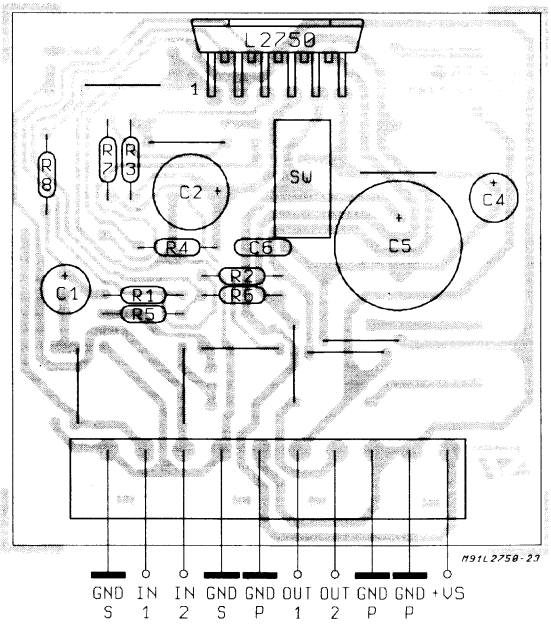


Figure 14: P.C. Board and Component Layout of the Circuit of Figure 13 (1:1 scale)



BRIDGE AUDIO APPLICATION CIRCUIT OF FIGURE 13

Figure 15: Quiescent Drain Current vs. Supply Voltage

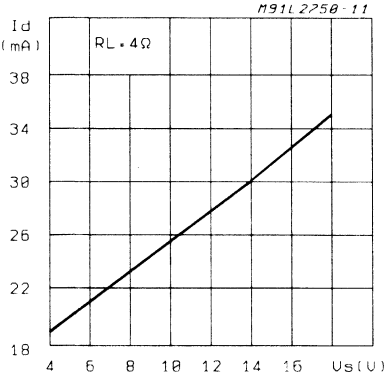


Figure 16: Noise vs. R_S

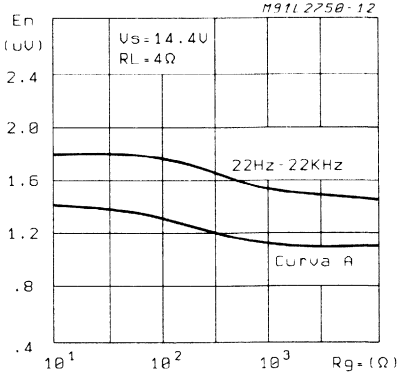


Figure 17: Output Power vs. Supply Voltage

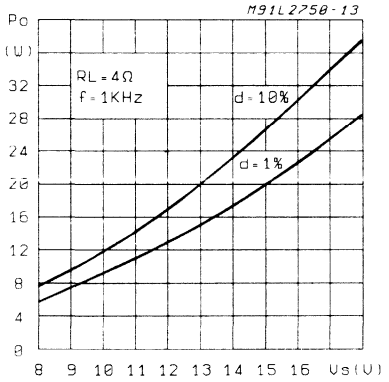


Figure 18: Output Power vs Supply Voltage

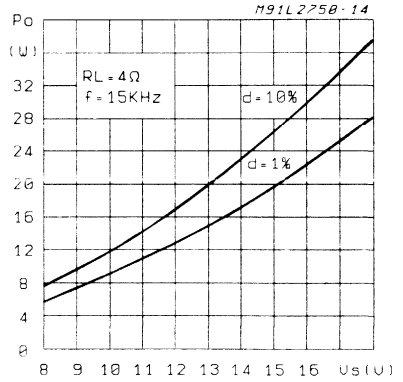


Figure 19: Distortion vs. Output Power

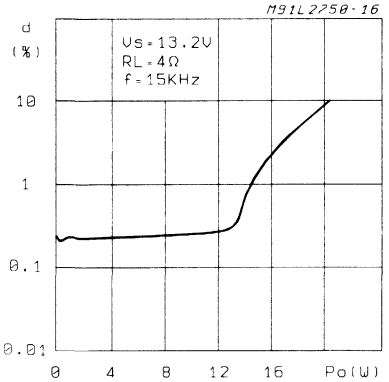


Figure 20: Distortion vs. Output Power

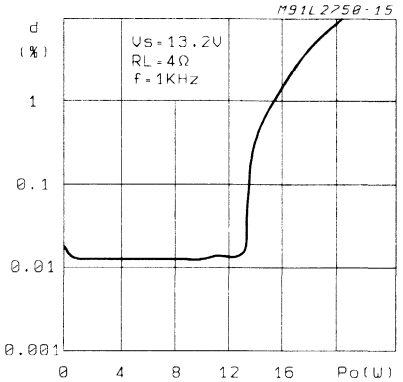


Figure 21: Distortion vs. Output Power

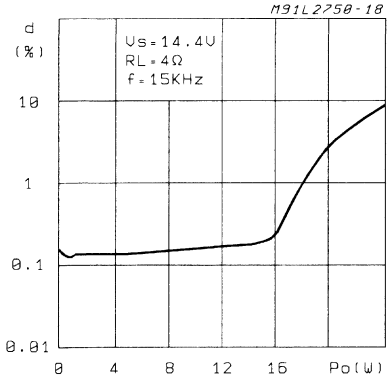


Figure 22: Distortion vs. Output Power

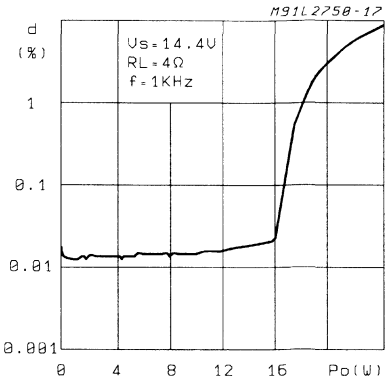


Figure 23: Distortion vs. Frequency

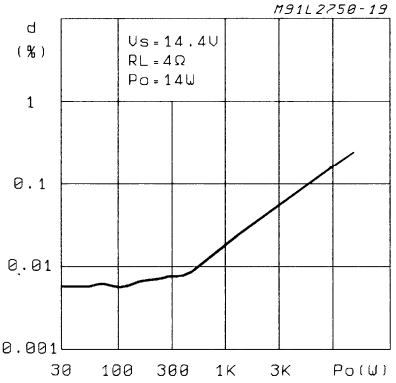


Figure 24: Supply Voltage Rejection vs. Frequency

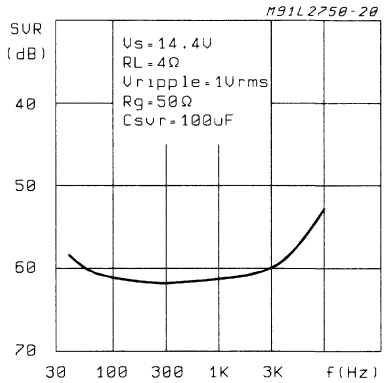


Figure 25: Total Power Dissipation and Efficiency vs. Output Power

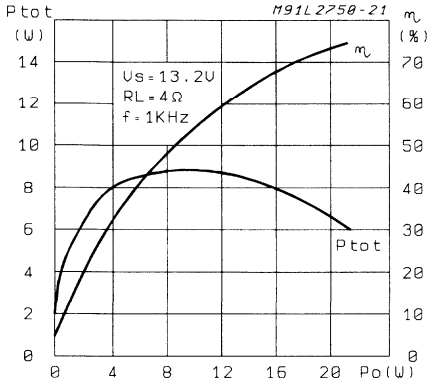
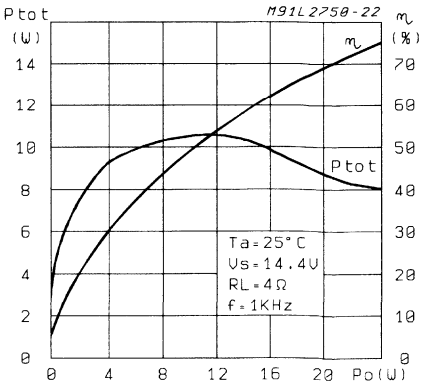


Figure 26: Total Power Dissipation and Efficiency vs. Output Power



SGS-THOMSON MICROELECTRONICS

L4901A

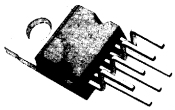
DUAL 5V REGULATOR WITH RESET

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST/1)

- OUTPUT CURRENTS: I_{o1} = 400mA
  I_{o2} = 400mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- LOW QUIESCENT CURRENT (INPUT 1)
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT HIGH
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4901A is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset and data save functions during switch on/off can be realized.



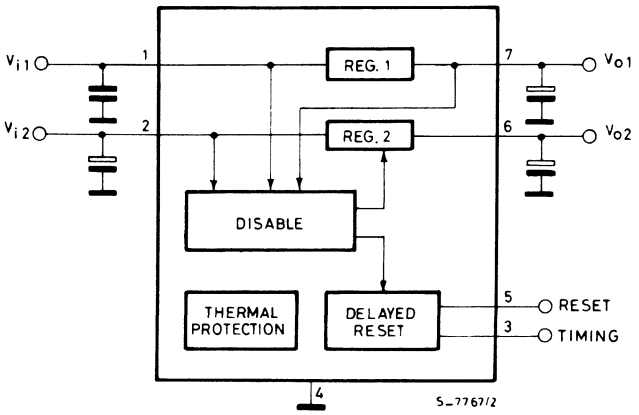
Heptawatt

ORDERING NUMBER: L4901A

ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	24	V
	Transient input overvoltage (t = 40 ms)	60	V
I_O	Output current	internally limited	
T_j	Storage and junction temperature	-40 to 150	°C

BLOCK DIAGRAM



SGS-THOMSON MICROELECTRONICS

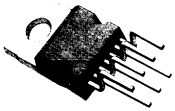
L4902A

DUAL 5V REGULATOR WITH RESET AND DISABLE

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST/1)

- DOUBLE BATTERY OPERATING
- OUTPUT CURRENTS: I_{01} = 300mA
  I_{02} = 300mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- OUTPUT 2 DISABLE LOGICAL INPUT
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- RESET OUTPUT NORMALLY HIGH
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4902A is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.
Reset and data save functions and remote switch on/off control can be realized.



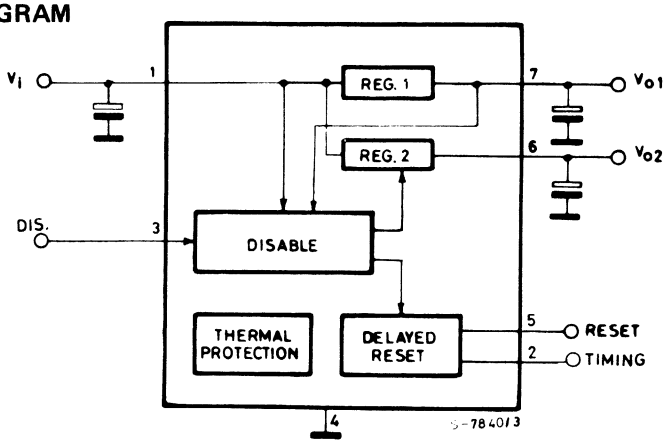
Heptawatt

ORDERING NUMBER: L4902A

ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	28	V
	Transient input overvoltage (t = 40 ms)	60	V
I_o	Output current	internally limited	
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

BLOCK DIAGRAM



DUAL 5V REGULATOR WITH RESET AND DISABLE FUNCTIONS

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST/1)

- OUTPUT CURRENTS: I_{o1} = 50mA, I_{o2} = 100mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ±2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- OUTPUT 2 DISABLE LOGICAL INPUT
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT NORMALLY LOW
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4903 is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset, data save functions and remote switch on/off control can be realized.

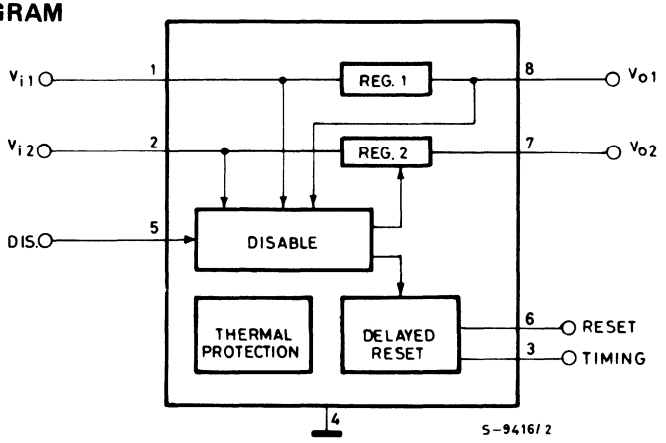
Minidip Plastic

ORDERING NUMBER: L4903

ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	24	V
V_t	Transient input overvoltage (t = 40 ms)	60	V
P_{tot}	Power dissipation at T_{amb} = 50°C	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

BLOCK DIAGRAM



DUAL 5V REGULATOR WITH RESET

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST/1)

- OUTPUT CURRENTS: I_{01} = 50mA, I_{02} = 100mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- LOW QUIESCENT CURRENT (INPUT 1)
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT NORMALLY HIGH
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4904A is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset and data save functions during switch on/off can be realized.

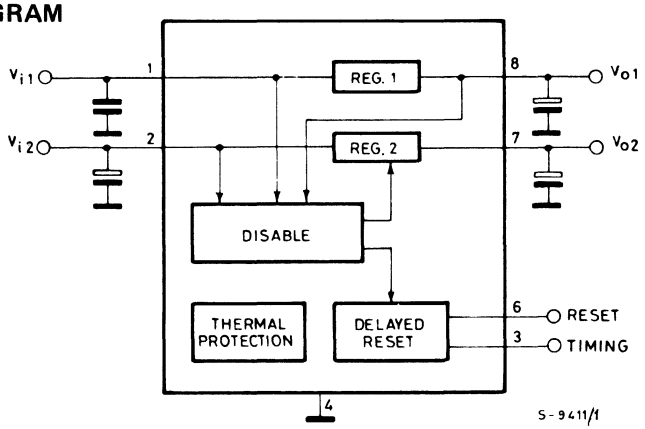
Minidip Plastic

ORDERING NUMBER: L4904A

ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	24	V
	Transient input overvoltage (t = 40 ms)	60	V
I_o	Output current	internally limited	
P_{tot}	Power dissipation at T_{amb} = 50°C	1	W
T_j	Storage and junction temperature	-40 to 150	°C

BLOCK DIAGRAM



SGS-THOMSON MICROELECTRONICS

L4905

DUAL 5V REGULATOR WITH RESET

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST/1)

- DOUBLE BATTERY OPERATING
- OUTPUT CURRENTS: I_{O1} = 200mA
  I_{O2} = 300mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 1%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- LOW QUIESCIENT CURRENT (INPUT 1)
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT HIGH
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4905 is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset and data save functions during switch on/off can be realized.

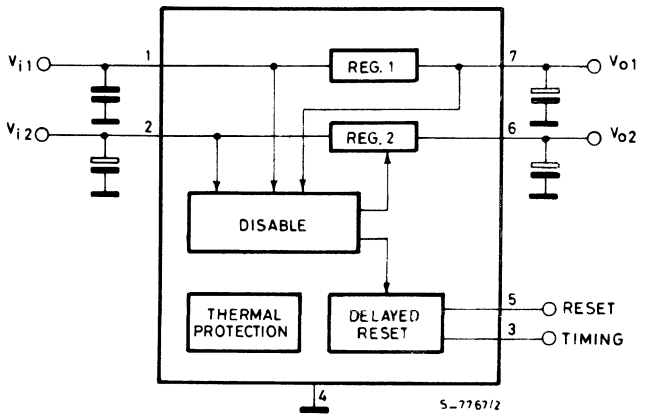
Heptawatt

ORDERING NUMBER: L4905

ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	28	V
	Transient input overvoltage (t = 40 ms)	60	V
I_o	Output current	internally limited	
T_j	Storage and junction temperature	-40 to 150	°C

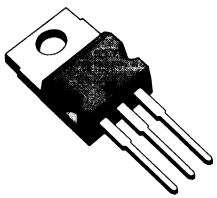
BLOCK DIAGRAM



VERY LOW DROP 1.5 A REGULATORS

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST/1)

- PRECISE 5 V, 8.5 V, 10 V, 12 V OUTPUTS
- LOW DROPOUT VOLTAGE (500 mV typ at 1.5A)
- VERY LOW QUIESCENT CURRENT
- THERMAL SHUTDOWN
- SHORT CIRCUIT PROTECTION
- REVERSE POLARITY PROTECTION

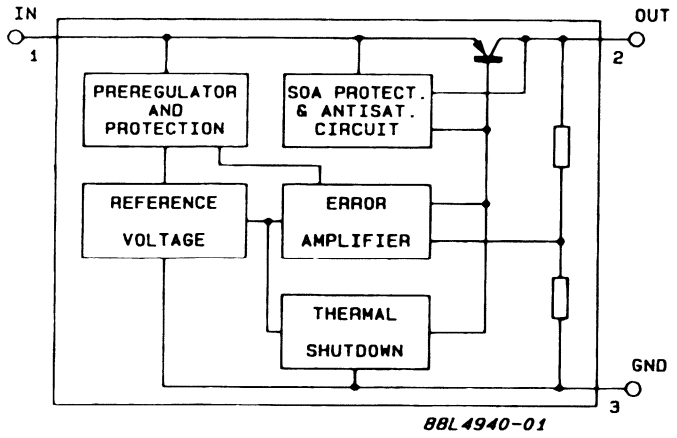


TO-220

DESCRIPTION

The L4940 series of three terminal positive regulators is available in TO-220 package and with several fixed output voltages, making it useful in a wide range of industrial and consumer applications. Thanks to its very low input/output voltage drop, these devices are particularly suitable for battery powered equipments, reducing consumption and prolonging battery life. Each type employs internal current limiting, antisaturation circuit, thermal shutdown and safe area protection.

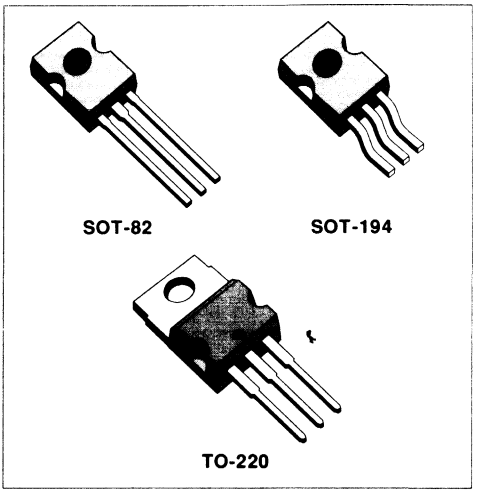
BLOCK DIAGRAM



VERY LOW DROP 1A REGULATOR

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST/1)

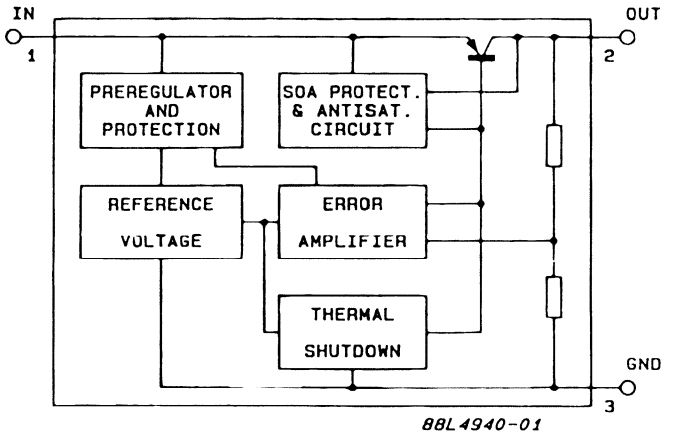
- LOW DROPOUT VOLTAGE (450 mV typ at 1A)
- VERY LOW QUIESCENT CURRENT
- THERMAL SHUTDOWN
- SHORT CIRCUIT PROTECTION
- REVERSE POLARITY PROTECTION



DESCRIPTION

The L4941 is a three terminal 5 V positive regulator available in TO-220, SOT-82 and SOT-194 packages, making it useful in a wide range of the industrial and consumer applications. Thanks to its very low input/output voltage drop, this device is particularly suitable for battery powered equipment, reducing consumption and prolonging battery life. It employs internal current limiting, antisaturation circuit, thermal shut-down and safe area protection.

BLOCK DIAGRAM



2.5A POWER SWITCHING REGULATOR

PRELIMINARY DATA

- 2.5A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- PRECISE (± 2%) ON-CHIP REFERENCE
- HIGH SWITCHING FREQUENCY
- VERY HIGH EFFICIENCY (UP TO 90%)
- VERY FEW EXTERNAL COMPONENTS
- SOFT START
- INTERNAL LIMITING CURRENT
- THERMAL SHUTDOWN

The L4960 is a monolithic power switching regulator delivering 2.5A at a voltage variable from 5V to 40V in step down configuration.

Features of the device include current limiting, soft start, thermal protection and 0 to 100% duty cycle for continuous operation mode.

The L4960 is mounted in a Heptawatt plastic power package and requires very few external componênts.

Efficient operation at switching frequencies up to 150KHz allows a reduction in the size and cost of external filter components.

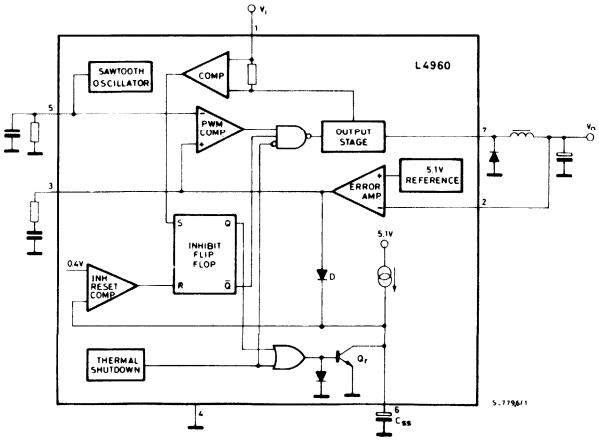
Heptawatt

ORDERING NUMBER: L4960 (Vertical)
L4960H (Horizontal)

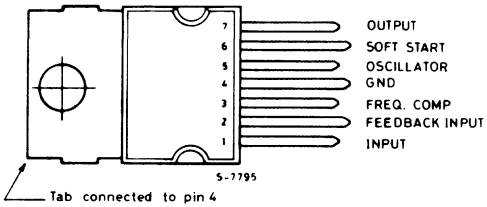
ABSOLUTE MAXIMUM RATINGS

V_1	Input voltage	50	V
$V_1 - V_7$	Input to output voltage difference	50	V
V_7	Negative output DC voltage	-1	V
	Negative output peak voltage at t = 0.1μs; f = 100KHz	-5	V
V_3, V_6	Voltage at pin 3 and 6	5.5	V
V_2	Voltage at pin 2	7	V
I_3	Pin 3 sink current	1	mA
I_5	Pin 5 source current	20	mA
P_{tot}	Power dissipation at $T_{case} \leqslant 90°C$	15	W
T_j, T_{stg}	Junction and storage temperature	-40 to 150	°C

BLOCK DIAGRAM



CONNECTION DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	50	°C/W

PIN FUNCTIONS

N°	NAME	FUNCTION
1	SUPPLY VOLTAGE	Unregulated voltage input. An internal regulator powers the internal logic.
2	FEEDBACK INPUT	The feedback terminal of the regulation loop. The output is connected directly to this terminal for 5.1V operation; it is connected via a divider for higher voltages.
3	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
4	GROUND	Common ground terminal.
5	OSCILLATOR	A parallel RC network connected to this terminal determines the switching frequency.
6	SOFT START	Soft start time constant. A capacitor is connected between this terminal and ground to define the soft start time constant. This capacitor also determines the average short circuit output current.
7	OUTPUT	Regulator output.

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $T_j = 25°C$, $V_i = 35V$, unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
DYNAMIC CHARACTERISTICS							
V_o	Output voltage range	V_i = 46V	I_o = 1A	V_{ref}		40	V
V_i	Input voltage range	$V_o = V_{ref}$ to 36V	I_o = 2.5A	9		46	V
ΔV_o	Line regulation	V_i = 10V to 40V $V_o = V_{ref}$	I_o = 1A		15	50	mV
ΔV_o	Load regulation	$V_o = V_{ref}$	I_o = 0.5A to 2A		10	30	mV
V_{ref}	Internal reference voltage (pin 2)	V_i = 9V to 46V	I_o = 1A	5	5.1	5.2	V
$\frac{\Delta V_{ref}}{\Delta T}$	Average temperature coefficient of refer. voltage	T_j = 0°C to 125°C I_o = 1A			0.4		mV/°C
V_d	Dropout voltage	I_o = 2A			1.4	3	V
I_{om}	Maximum operating load current	V_i = 9V to 46V $V_o = V_{ref}$ to 36V		2.5			A
I_{7L}	Current limiting threshold (pin 7)	V_i = 9V to 46V $V_o = V_{ref}$ to 36V		3		4.5	A
I_{SH}	Input average current	V_i = 46V; output short-circuit			30	60	mA
η	Efficiency	f = 100KHz	$V_o = V_{ref}$		75		%
		I_o = 2A	V_o = 12V		85		%
SVR	Supply voltage ripple rejection	$\Delta V_i = 2V_{rms}$ f_{ripple} = 100Hz $V_o = V_{ref}$	I_o = 1A	50	56		dB
f	Switching frequency			85	100	115	KHz
$\frac{\Delta f}{\Delta V_i}$	Voltage stability of switching frequency	V_i = 9V to 46V			0.5		%
$\frac{\Delta f}{\Delta T_j}$	Temperature stability of switching frequency	T_j = 0°C to 125°C			1		%
f_{max}	Maximum operating switching frequency	$V_o = V_{ref}$	I_o = 2A	120	150		KHz
T_{sd}	Thermal shutdown junction temperature				150		°C

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
DC CHARACTERISTICS							
I_{1Q}	Quiescent drain current	100% duty cycle pins 5 and 7 open	V_I = 46V		30	40	mA
		0% duty cycle			15	20	mA
$-I_{7L}$	Output leakage current	0% duty cycle				1	mA
SOFT START							
I_{6SO}	Source current			100	130	150	μA
I_{6SI}	Sink current			50	70	120	μA
ERROR AMPLIFIER							
V_{3H}	High level output voltage	V_2 = 4.7V	I_3 = 100μA	3.5			V
V_{3L}	Low level output voltage	V_2 = 5.3V	I_3 = 100μA			0.5	V
I_{3SI}	Sink output current	V_2 = 5.3V		100	150		μA
$-I_{3SO}$	Source output current	V_2 = 4.7V		100	150		μA
I_2	Input bias current	V_2 = 5.2V			2	10	μA
G_v	DC open loop gain	V_3 = 1V to 3V		46	55		dB
OSCILLATOR							
$-I_5$	Oscillator source current			5			mA

CIRCUIT OPERATION (refer to the block diagram)

The L4960 is a monolithic stepdown switching regulator providing output voltages from 5.1V to 40V and delivering 2.5A.

The regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1V on-chip reference (zener zap trimmed to ± 2%).

This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage.

The gain and frequency stability of the loop can be adjusted by an external RC network connected to pin 3. Closing the loop directly gives an output voltage of 5.1V. Higher voltages are obtained by inserting a voltage divider.

Output overcurrents at switch on are prevented by the soft start function. The error amplifier output is initially clamped by the external capacitor C_{ss} and allowed to rise, linearly, as this capacitor is charged by a constant current source. Output overload protection is provided in the form of a current limiter. The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold this comparator sets a flip flop which disables the output stage and discharges the soft start capacitor. A second comparator resets the flip flop when the voltage across the soft start capacitor has fallen to 0.4V.

The output stage is thus re-enabled and the output voltage rises under control of the soft start network. If the overload condition is still present the limiter will trigger again when the threshold current is reached. The average short circuit current is limited to a safe value by the dead time introduced by the soft start network. The thermal overload circuit disables circuit operation when the junction temperature reaches about 150°C and has hysteresis to prevent unstable conditions.

Fig. 1 - Soft start waveforms

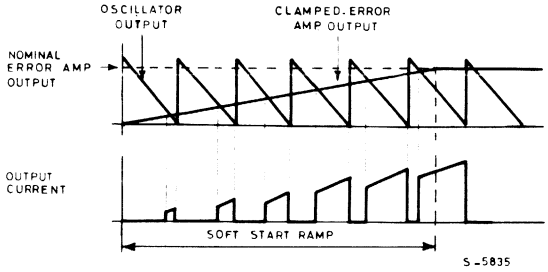


Fig. 2 - Current limiter waveforms

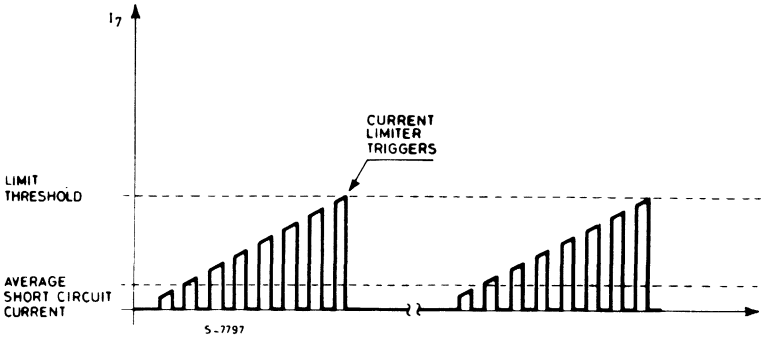
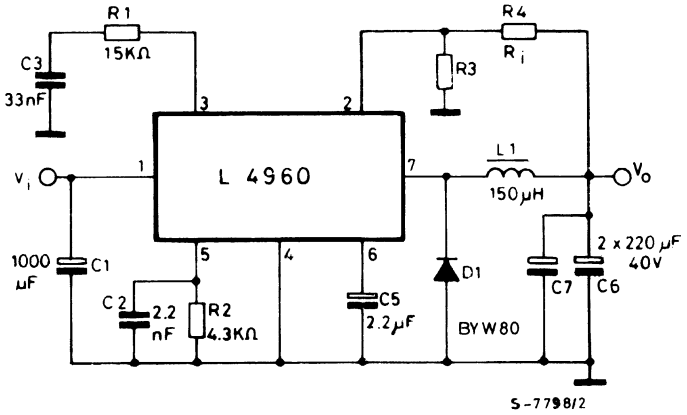


Fig. 3 - Test and application circuit



C6, C7: EKR (ROE)
L1 = 150µH at 5A (COGEMA 946042)
CORE TYPE: MAGNETICS 58206-A2 MPP
N° TURNS 45, WIRE GAUGE: 0.8mm (20 AWG)

Fig. 4 - Quiescent drain current vs. supply voltage (0% duty cycle)

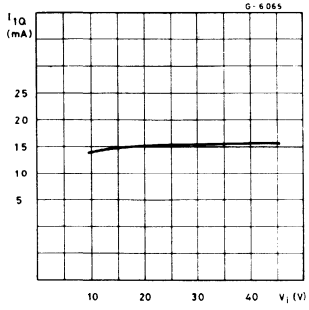


Fig. 5 - Quiescent drain current vs. supply voltage (100% duty cycle)

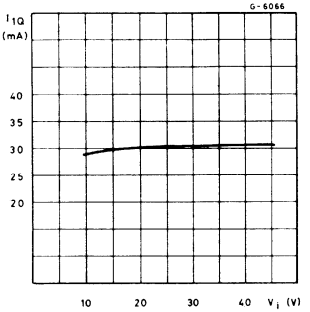


Fig. 6 - Quiescent drain current vs. junction temperature (0% duty cycle)

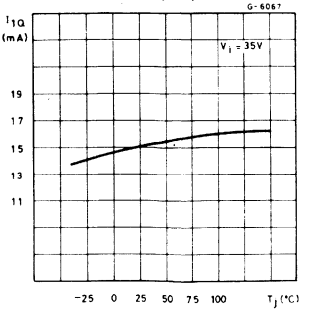


Fig. 7 - Quiescent drain current vs. junction temperature (100% duty cycle)

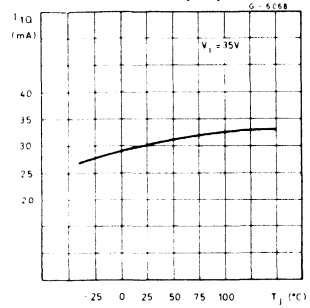


Fig. 8 - Reference voltage (pin 2) vs. V_I

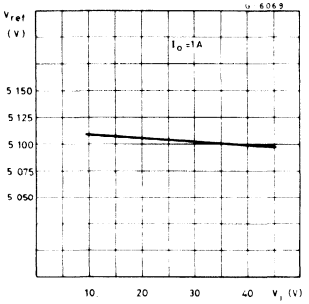


Fig. 9 - Reference voltage vs. junction temperature (pin 2)

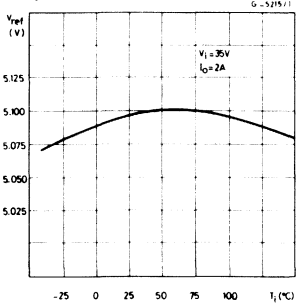


Fig. 10 - Open loop frequency and phase responde of error amplifier

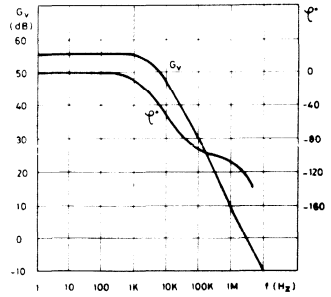


Fig. 11 - Switching frequency vs. input voltage

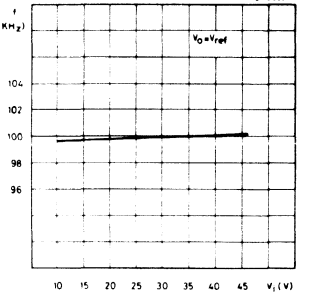


Fig. 12 - Switching frequency vs. junction temperature

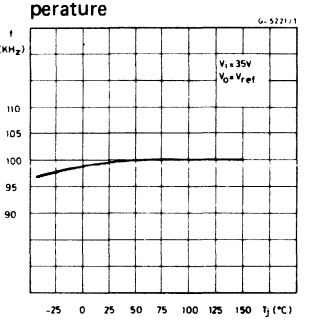


Fig. 13 - Switching frequency vs. R2 (see test circuit)

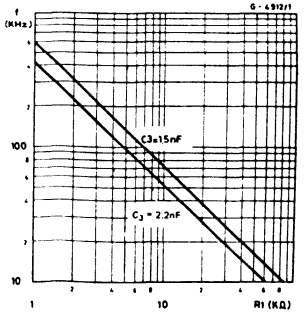


Fig. 14 - Line transient response

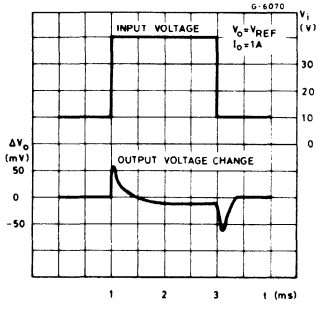


Fig. 15 - Load transient response

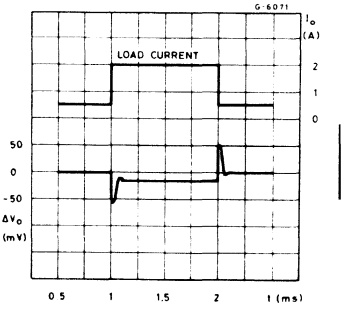


Fig. 16 - Supply voltage ripple rejection vs. frequency

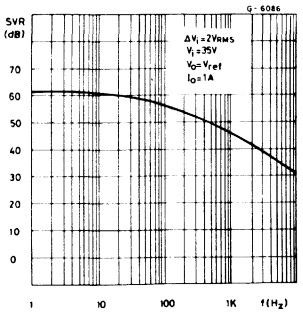


Fig. 17 - Dropout voltage between pin 1 and pin 7 vs. current at pin 7

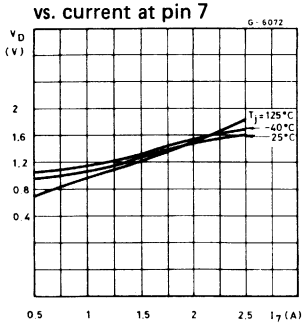


Fig. 18 - Dropout voltage between pin 1 and 7 vs. junction temperature

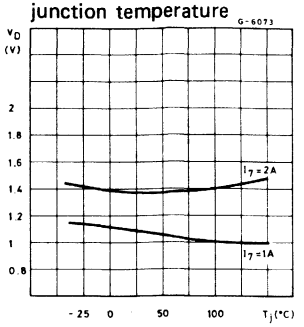


Fig. 19 - Power dissipation derating curve

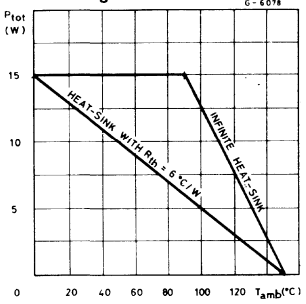


Fig. 20 - Efficiency vs. output current

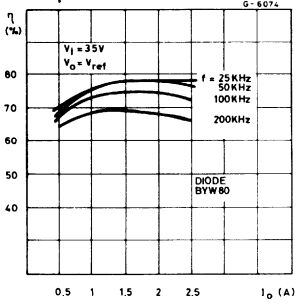


Fig. 21 - Efficiency vs. output current

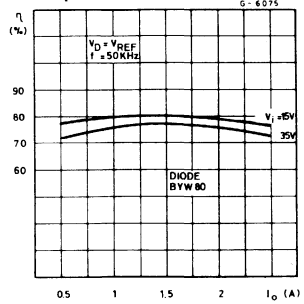


Fig. 22 - Efficiency vs. output current

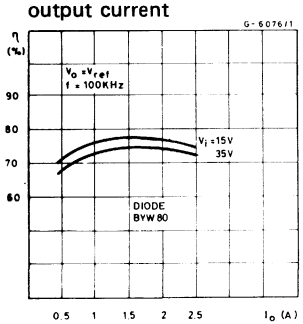
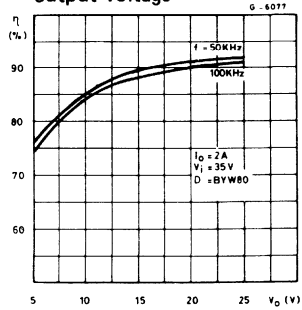
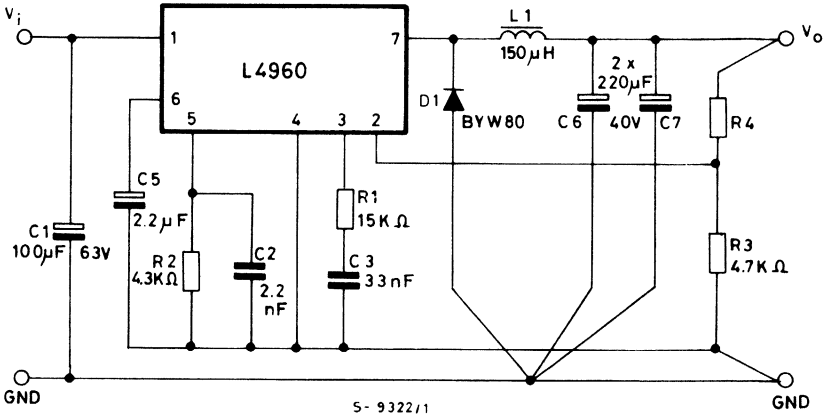


Fig. 23 - Efficiency vs. output voltage



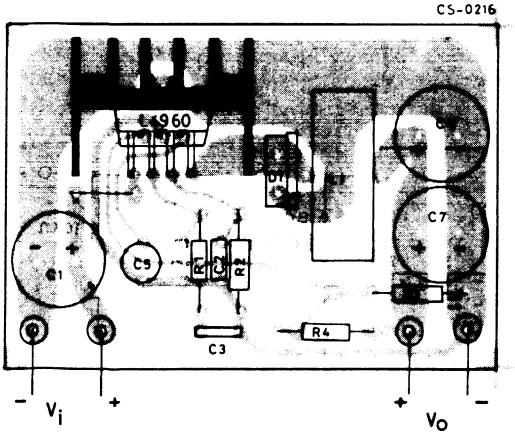
APPLICATION INFORMATION

Fig. 24 - Typical application circuit



C_1, C_6, C_7: EKR (ROE)
D_1: BYW80 OR 5A SCHOTTKY DIODE
SUGGESTED INDUCTOR: L_1 = 150µH at 5A
CORE TYPE: MAGNETICS 58206 - A2 - MPP
N° TURNS: 45, WIRE GAUGE: 0.8mm (20 AWG), COGEMA 946042
U15/GUP15: N° TURNS: 60, WIRE GAUGE: 0.8mm (20 AWG), AIR GAP: 1mm, COGEMA 969051.

Fig. 25 - P.C. board and component layout of the Fig. 24 (1 : 1 scale)



Resistor values for standard output voltages		
V_o	R3	R4
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

APPLICATION INFORMATION (continued)

Fig. 26 - A minimal 5.1V fixed regulator; Very few component are required

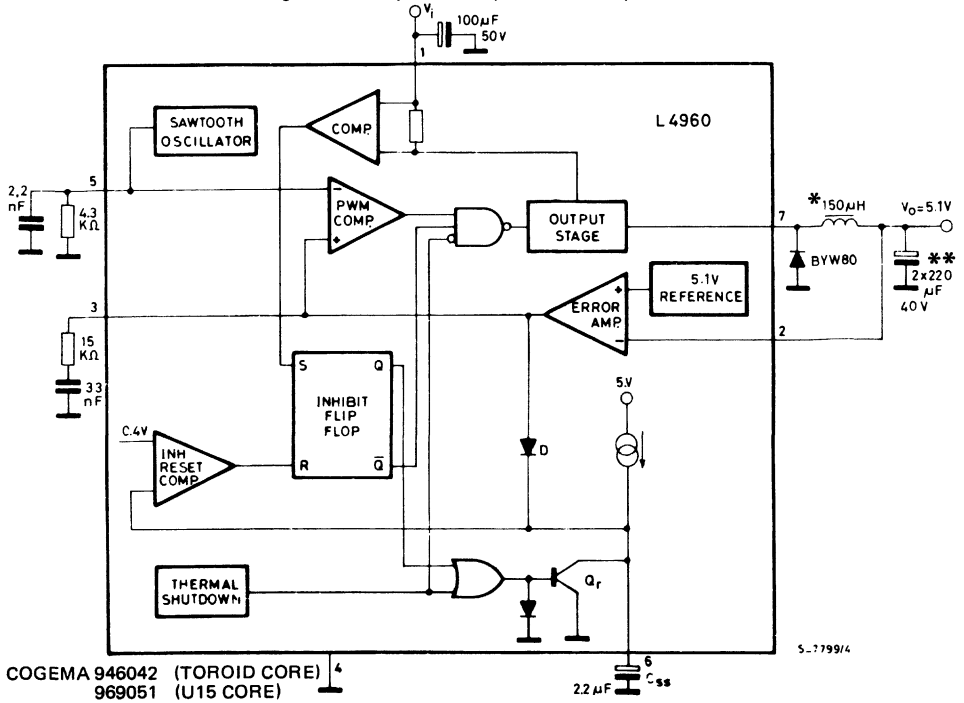
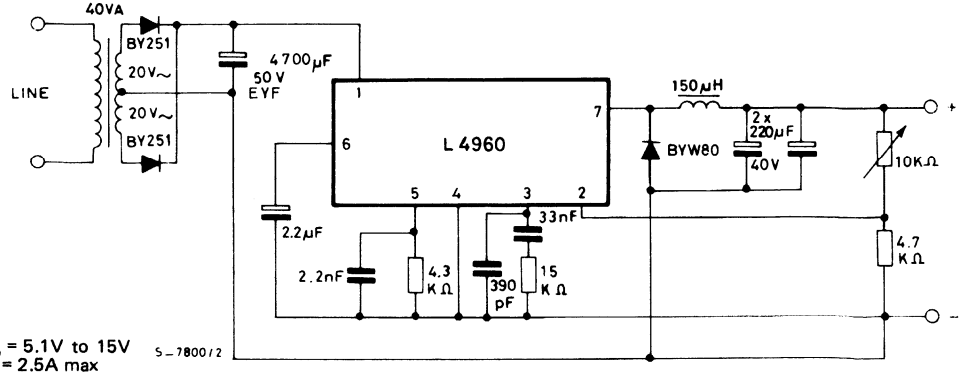


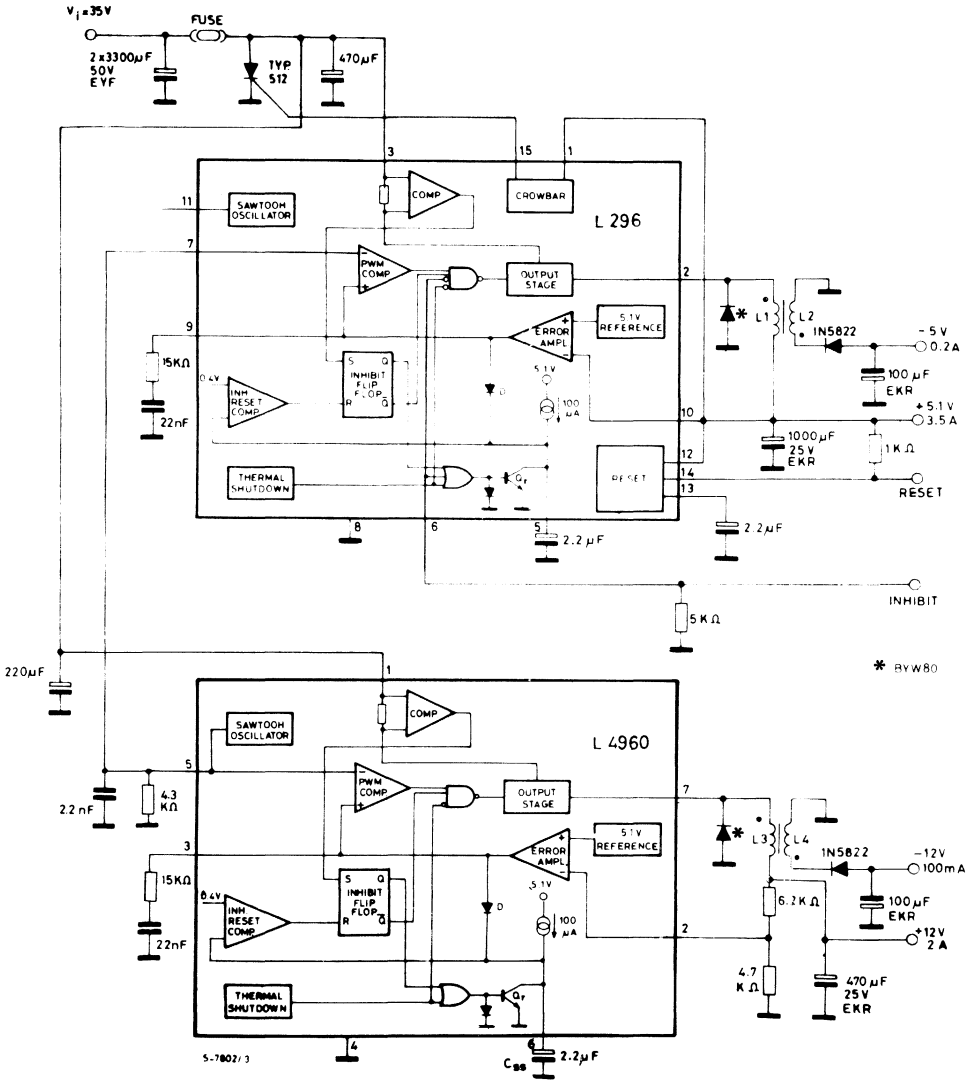
Fig. 27 - Programmable power supply



V_o = 5.1V to 15V
I_o = 2.5A max
Load regulation (1A to 2A) = 10mV (V_o = 5.1V)
Line regulation (220V ± 15% and to I_O = 1A) = 15mV (V_o = 5.1V)

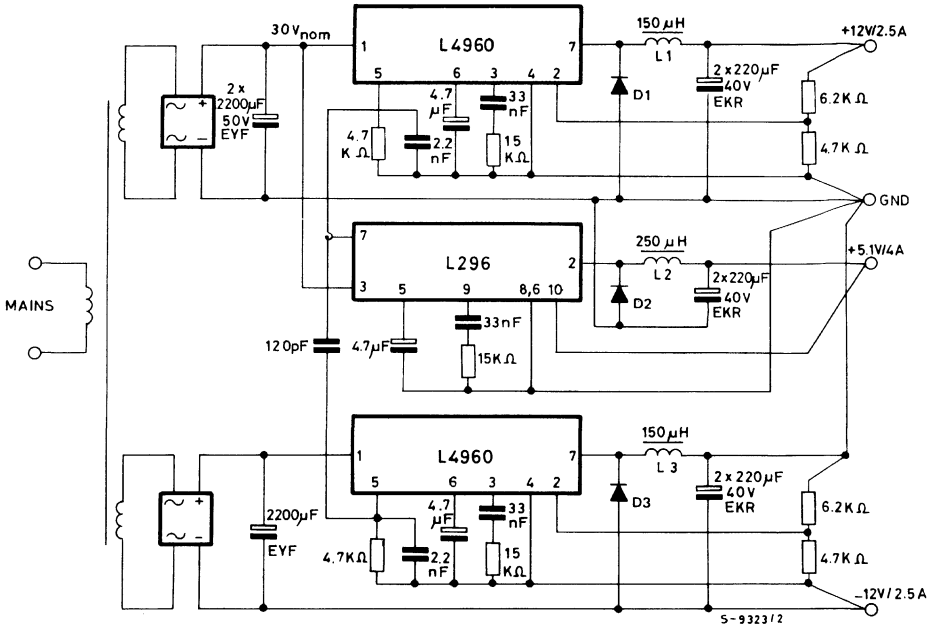
APPLICATION INFORMATION (continued)

Fig. 28 - Microcomputer supply with + 5.1V, -5V, +12V and -12V outputs



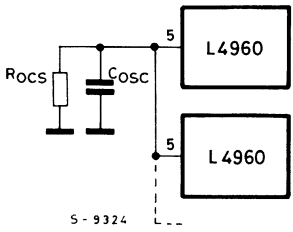
APPLICATION INFORMATION (continued)

Fig. 29 - DC-DC converter 5.1V/4A, ± 12V/2.5A; a suggestion how to synchronize a negative output



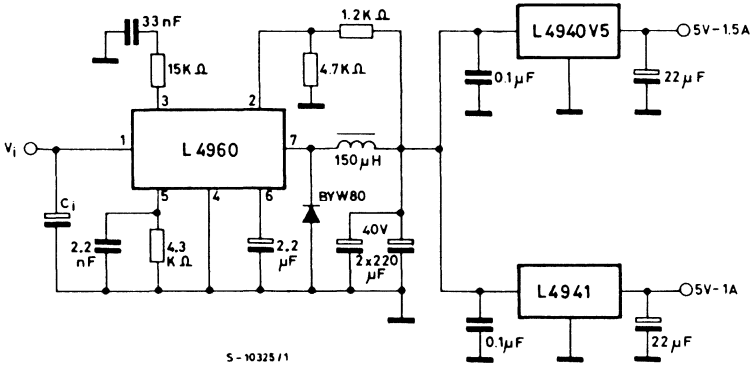
L1, L3 = COGEMA 946042 (969051)
L2 = COGEMA 946044 (946045)
D_1, D_2, D3 = BYW80

Fig. 30 - In multiple supplies several L4960s can be synchronized as shown



APPLICATION INFORMATION (continued)

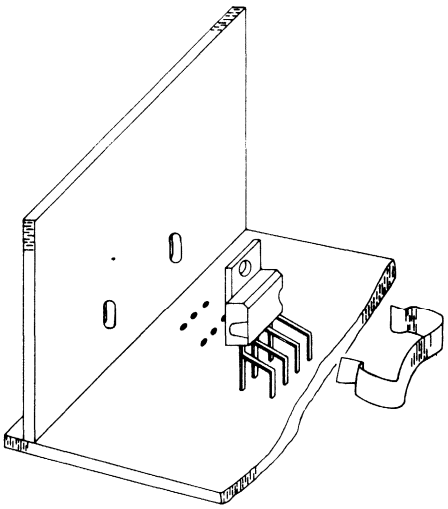
Fig. 31 - Regulator for distributed supplies



MOUNTING INSTRUCTION

The power dissipated in the circuit must be removed by adding an external heatsink.
Thanks to the Heptawatt package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact, no electrical isolation is needed between the two surfaces.

Fig. 32 - Mounting example



1.5A POWER SWITHING REGULATOR

PRELIMINARY DATA

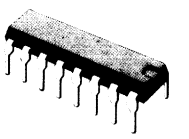
- 1.5A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- PRECISE (± 2 %) ON-CHIP REFERENCE
- HIGH SWITCHING FREQUENCY
- VERY HIGH EFFICIENCY (UP TO 90%)
- VERY FEW EXTERNAL COMPONENTS
- SOFT-START
- INTERNAL LIMITING CURRENT
- THERMAL SHUTDOWN

The L4962 is a monolithic power switching regulator delivering 1.5A at a voltage veriable from 5V to 40V in step down configuration.

Features of device include current limiting, soft start, thermal protection and 0 to 100% duty cycle for continuous operating mode.

The L4962 is mounted in a 16-lead Powerdip plastic package and Heptawatt package and requires very few external components.

Efficient operation at switching frequencies up to 150KHz allows a reduction in the size and cost of external filter components.



Powerdip
(12 + 2 + 2)

Heptawatt

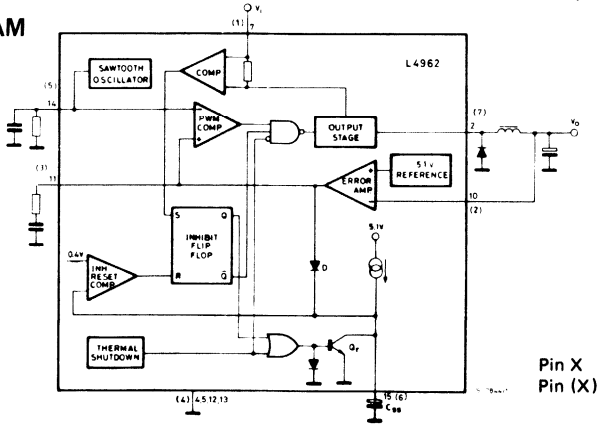
ORDERING NUMBER:

L4962 (12 + 2 + 2 Powerdip)
L4962E (Heptawatt)
L4962EH (Horizontal Heptawatt)

ABSOLUTE MAXIMUM RATINGS

V_7	Input voltage	50	V
$V_7 - V_2$	Input to output voltage difference	50	V
V_2	Negative output DC voltage	-1	V
	Output peak voltage at t = 0.1μs, f = 100KHz	-5	V
V_{11}, V_{15}	Voltage at pin 11, 15	5.5	V
V_{10}	Voltage at pin 10	7	V
I_{11}	Pin 11 sink current	1	mA
I_{14}	Pin 14 source current	20	mA
P_{tot}	Power dissipation at $T_{pins} \leq 90°C$ (Powerdip)	4.3	W
	$T_{case} \leq 90°C$ (Heptawatt)	15	W
T_j, T_{stg}	Junction and storage temperature	-40 to 150	°C

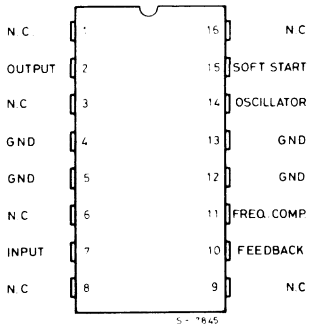
BLOCK DIAGRAM

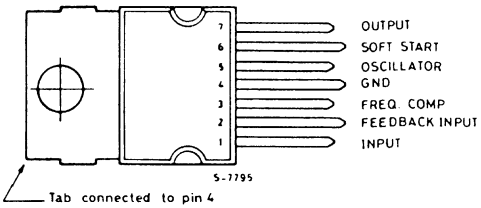


Pin X = Powerdip
Pin (X) = Heptawatt

CONNECTION DIAGRAMS

(Top view)





THERMAL DATA

			Heptawatt	Powerdip
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4°C/W	–
$R_{th\ j\text{-}pins}$	Thermal resistance junction-pins	max	–	14°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	50°C/W	80°C/W*

* Obtained with the GND pins soldered to printed circuit with minimized copper area.

PIN FUNCTIONS

HEPTAWATT	POWERDIP	NAME	FUNCTION
1	7	SUPPLY VOLTAGE	Unregulated voltage input. An internal regulator powers the internal logic.
2	10	FEEDBACK INPUT	The feedback terminal of the regulation loop. The output is connected directly to this terminal for 5.1V operation; it is connected via a divider for higher voltages.
3	11	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
4	4, 5, 12, 13	GROUND	Common ground terminal.
5	14	OSCILLATOR	A parallel RC network connected to this terminal determines the switching frequency. This pin must be connected to pin 7 input when the internal oscillator is used.
6	15	SOFT START	Soft start time constant. A capacitor is connected between this terminal and ground to define the soft start time constant. The capacitor also determines the average short circuit output current.
7	2	OUTPUT	Regulator output.
	1, 3, 6, 8, 9, 16		N.C.

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $T_j = 25°C$, $V_I = 35V$, unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
DYNAMIC CHARACTERISTICS						
V_o	Output voltage range	V_I = 46V I_o = 1A	V_{ref}		40	V
V_I	Input voltage range	$V_o = V_{ref}$ to 36V I_o = 1.5A	9		46	V
ΔV_o	Line regulation	V_I = 10V to 40V $V_o = V_{ref}$ I_o = 1A		15	50	mV
ΔV_o	Load regulation	$V_o = V_{ref}$ I_o = 0.5A to 1.5A		8	20	mV
V_{ref}	Internal reference voltage (pin 10)	V_I = 9V to 46V I_o = 1A	5	5.1	5.2	V
$\frac{\Delta V_{ref}}{\Delta T}$	Average temperature coefficient of refer. voltage	T_j = 0°C to 125°C I_o = 1A		0.4		mV/°C
V_d	Dropout voltage	I_o = 1.5A		1.5	2	V
I_{om}	Maximum operating load current	V_I = 9V to 46V $V_o = V_{ref}$ to 36V	1.5			A
I_{2L}	Current limiting threshold (pin 2)	V_I = 9V to 46V $V_o = V_{ref}$ to 36V	2		3.3	A
I_{SH}	Input average current	V_I = 46V; output short-circuit		15	30	mA
η	Efficiency	f = 100KHz $V_o = V_{ref}$		70		%
		I_o = 1A V_o = 12V		80		%
SVR	Supply voltage ripple rejection	$\Delta V_I = 2V_{rms}$ f_{ripple} = 100Hz $V_o = V_{ref}$ I_o = 1A	50	56		dB
f	Switching frequency		85	100	115	KHz
$\frac{\Delta f}{\Delta V_I}$	Voltage stability of switching frequency	V_I = 9V to 46V		0.5		%
$\frac{\Delta f}{\Delta T_j}$	Temperature stability of switching frequency	T_j = 0°C to 125°C		1		%
f_{max}	Maximum operating switching frequency	$V_o = V_{ref}$ I_o = 1A	120	150		KHz
T_{sd}	Thermal shutdown junction temperature			150		°C

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
DC CHARACTERISTICS							
I_{7Q}	Quiescent drain current	100% duty cycle pins 2 and 14 open	V_I = 46V		30	40	mA
		0% duty cycle			15	20	mA
$-I_{2L}$	Output leakage current	0% duty cycle				1	mA
SOFT START							
I_{15SO}	Source current			100	130	160	μA
I_{15SI}	Sink current			50	70	120	μA
ERROR AMPLIFIER							
V_{11H}	High level output voltage	V_{10} = 4.7V	I_{11} = 100μA	3.5			V
V_{11L}	Low level output voltage	V_{10} = 5.3V	I_{11} = 100μA			0.5	V
I_{11SI}	Sink output current	V_{10} = 5.3V		100	150		μA
$-I_{11SO}$	Source output current	V_{10} = 4.7V		100	150		μA
I_{10}	Input bias current	V_{10} = 5.2V			2	10	μA
G_v	DC open loop gain	V_{11} = 1V to 3V		46	55		dB
OSCILLATOR							
$-I_{14}$	Oscillator source current			5			mA

CIRCUIT OPERATION (refer to the block diagram)

The L4962 is a monolithic stepdown switching regulator providing output voltages from 5.1V to 40V and delivering 1.5A.

The regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1V on-chip reference (zener zap trimmed to ± 2%).

This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage.

The gain and frequency stability of the loop can be adjusted by an external RC network connected to pin 11. Closing the loop directly gives an output voltage of 5.1V. Higher voltages are obtained by inserting a voltage divider.

Output overcurrents at switch on are prevented by the soft start function. The error amplifier output is initially clamped by the external capacitor C_{ss} and allowed to rise, linearly, as this capacitor is charged by a constant current source. Output overload protection is provided in the form of a current limiter. The load current is sensed by a internal metal resistor connected to a comparator. When the load current exceeds a preset threshold this comparator sets a flip flop which disables the output stage and discharges the soft start capacitor. A second comparator resets the flip flop when the voltage across the soft start capacitor has fallen to 0.4V.

The output stage is thus re-enabled and the output voltage rises under control of the soft start network. If the overload condition is still present the limiter will trigger again when the threshold current is reached. The average short circuit current is limited to a safe value by the dead time introduced by the soft start network. The thermal overload circuit disables circuit operation when the junction temperature reaches about 150°C and has hysteresis to prevent unstable conditions.

Fig. 1 - Soft start waveforms

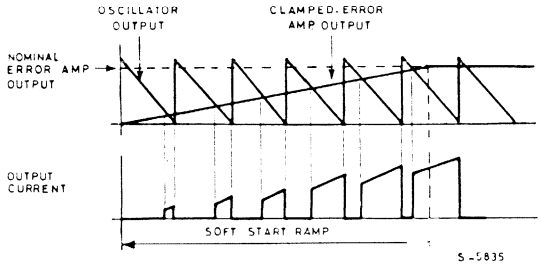


Fig. 2 - Current limiter waveforms

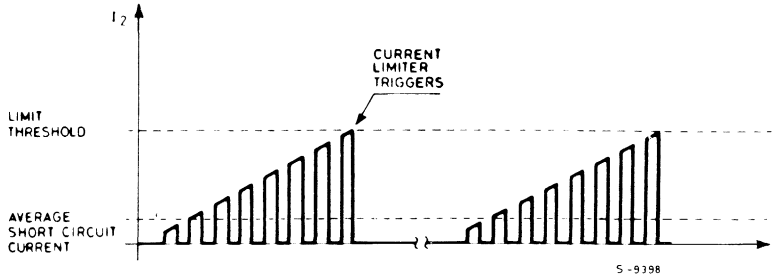
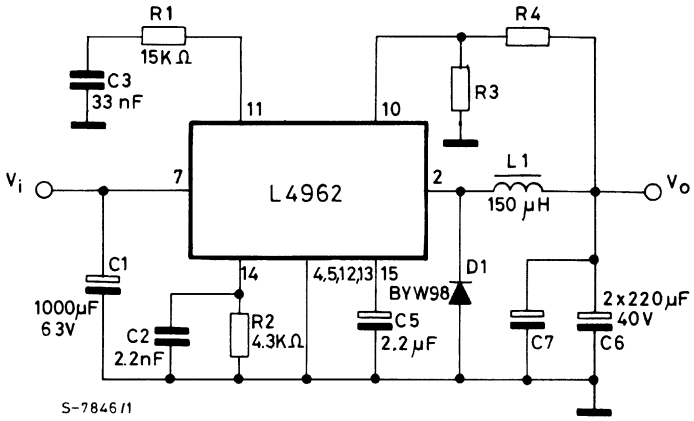


Fig. 3 - Test and application circuit (Powerdip)



1) D_1: BYW98 or 3A Schottky diode, 45V of VRRM;
2) L_1: CORE TYPE - MAGNETICS 58120 - A2 MPP
   N° TURNS 45, WIRE GAUGE: 0.8mm (20 AWG)
3) C_6, C_7: ROE, EKR 220μF 40V

Fig. 4 - Quiescent drain current vs. supply voltage (0% duty cycle)

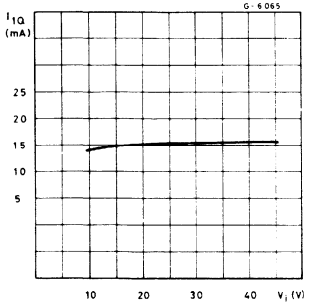


Fig. 5 - Quiescent drain current vs. supply voltage (100% duty cycle)

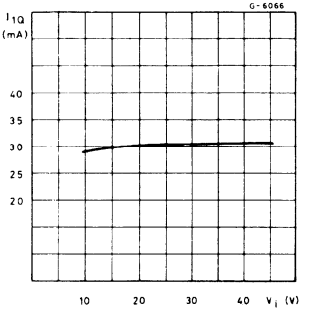


Fig. 6 - Quiescent drain current vs. junction temperature (0% duty cycle)

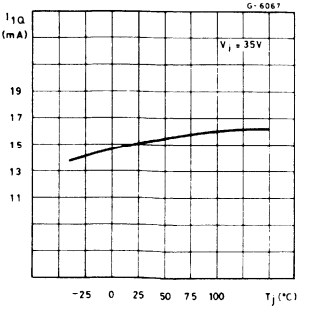


Fig. 7 - Quiescent drain current vs. junction temperature (100% duty cycle)

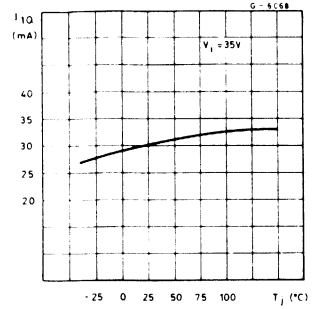


Fig. 8 - Reference voltage (pin 10) vs. V_I rdip) vs. V_I

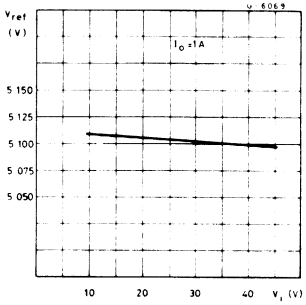


Fig. 9 - Reference voltage (pin 10) vs. junction temperature

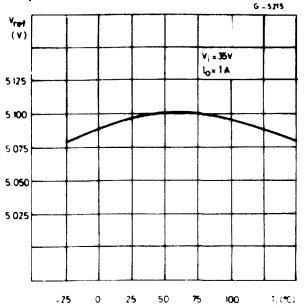


Fig. 10 - Open loop frequency and phase response of error amplifier

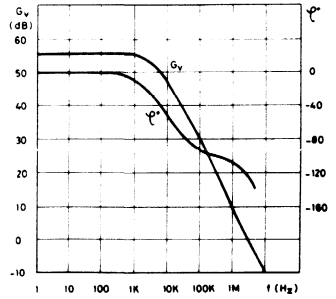


Fig. 11 - Switching frequency vs. input voltage

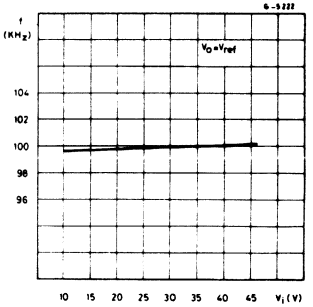


Fig. 12 - Switching frequency vs. junction temperature

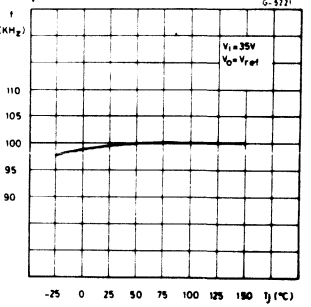


Fig. 13 - Switching frequency vs. R2 (see test circuit)

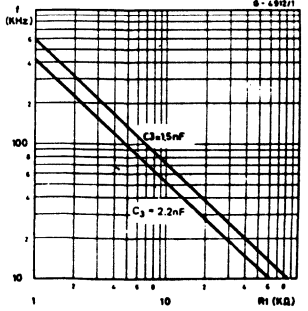


Fig. 14 - Line transient response

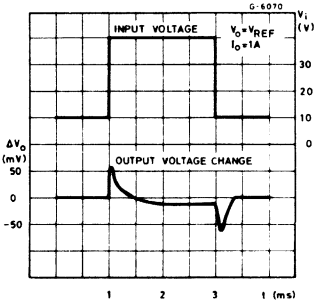


Fig. 15 - Load transient response

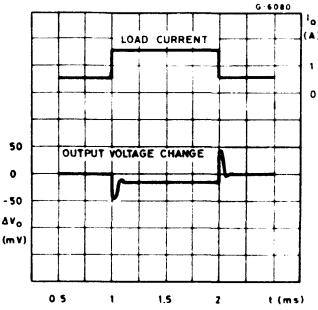


Fig. 16 - Supply voltage ripple rejection vs. frequency

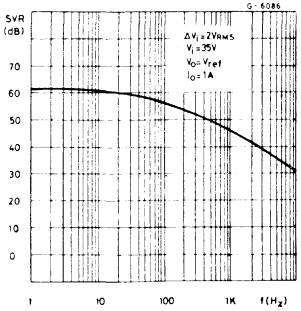


Fig. 17 - Dropout voltage between pin 7 and pin 2 vs. current at pin 2

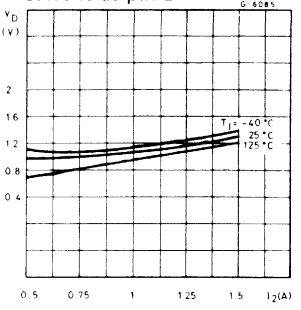


Fig. 18 - Dropout voltage between pin 7 and 2 vs. junction temperature

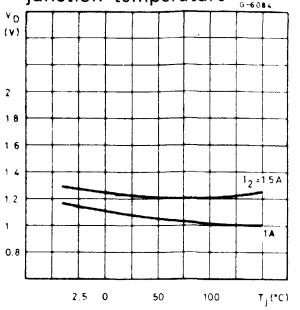


Fig. 19 - Efficiency vs. output current

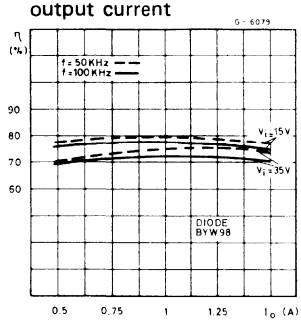


Fig. 20 - Efficiency vs. output current

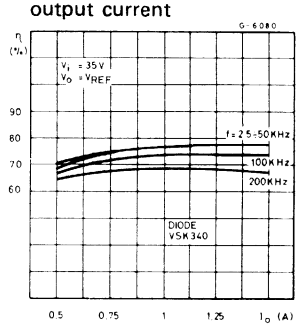


Fig. 21 - Efficiency vs. output current

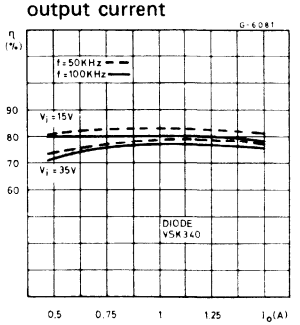


Fig. 22 - Efficiency vs. output voltage

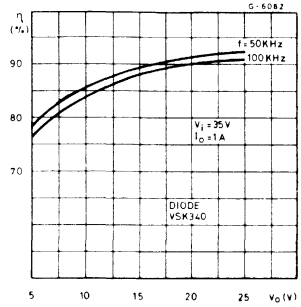


Fig. 23 - Efficiency vs. output voltage

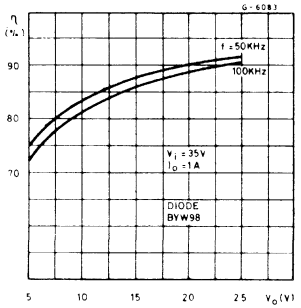
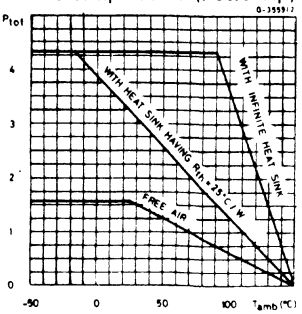
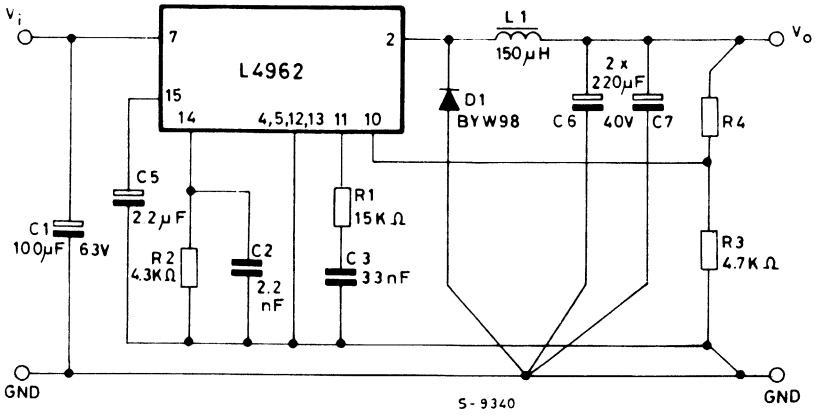


Fig. 24 - Maximum allowable power dissipation vs. ambient temperature (Powerdip)



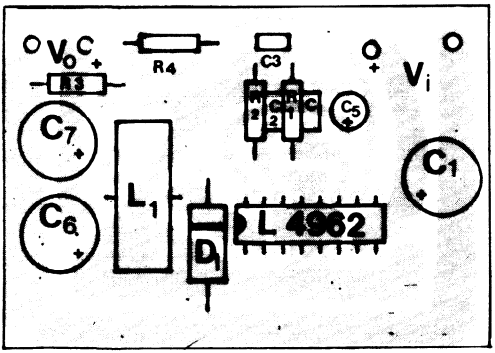
APPLICATION INFORMATION

Fig. 25 - Typical application circuit



C_1, C_6, C_7: EKR (ROE)
D_1: BYW98 OR VISK340 (SCHOTTKY)
SUGGESTED INDUCTORS (L_1): MAGNETICS 58120 - A2MPP - 45 TURNS - WIRE GAUGE 0.8mm (20AWG) - COGEMA 946043
OR U15, GUP15, 60 TURNS 1mm, AIR GAP 0.8mm (20AWG) - COGEMA 969051

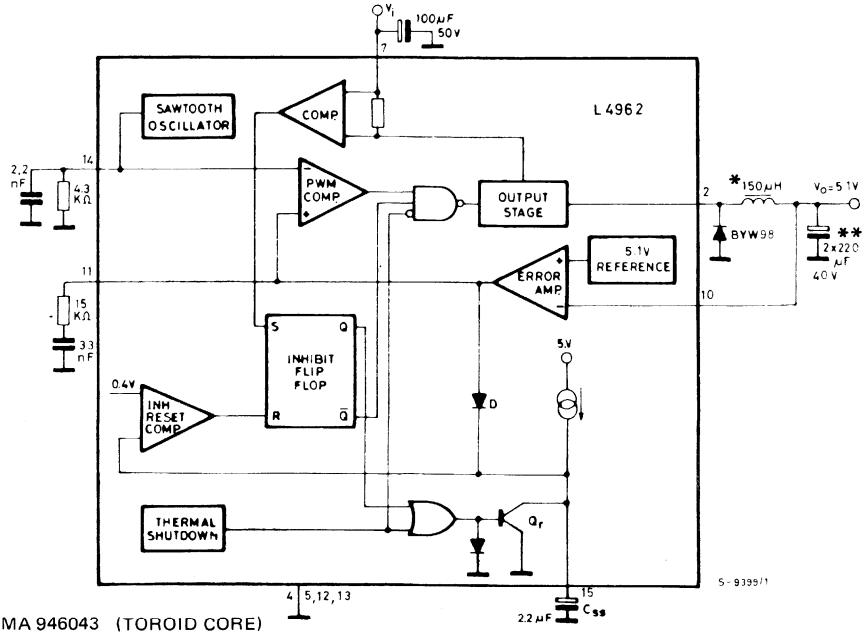
Fig. 26 - P.C. board and component layout of the circuit of Fig. 25 (1 : 1 scale)



Resistor values for standard output 7 voltages		
V_o	R3	R4
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

APPLICATION INFORMATION (continued)

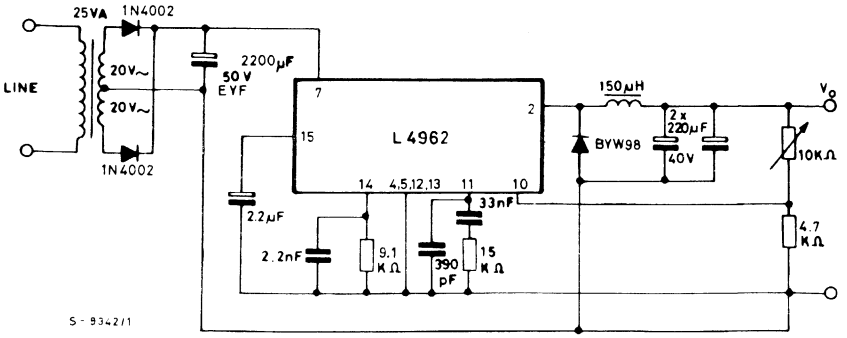
Fig. 27 - A minimal 5.1V fixed regulator; very few components are required



* COGEMA 946043 (TOROID CORE)
969051 (U15 CORE)

** EKR (ROE)

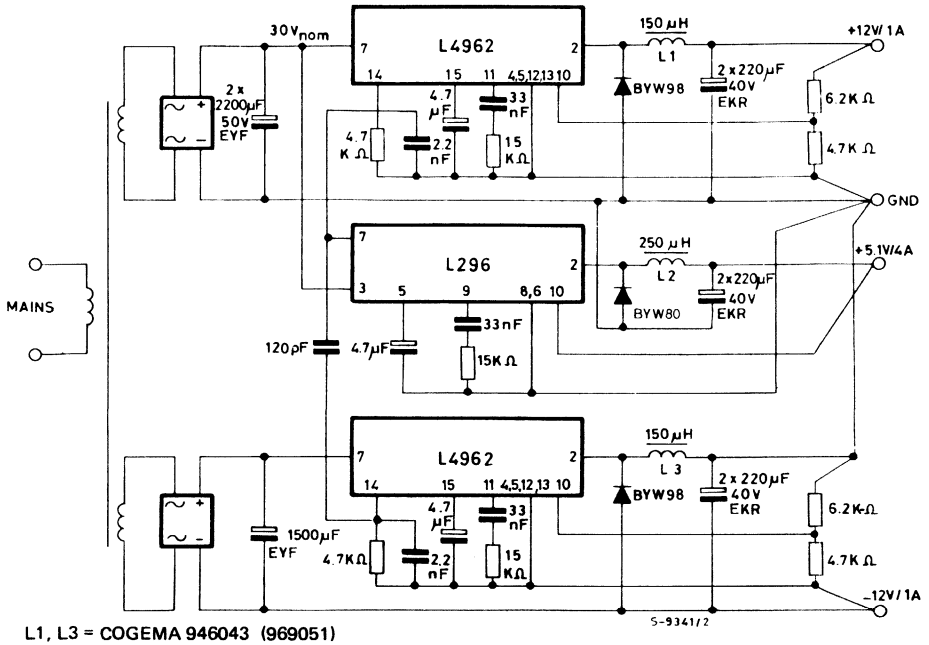
Fig. 28 - Programmable power supply



V_O = 5.1V to 15V
I_O = 1.5A max
Load regulation (0.5A to 1.5A) = 10mV (V_O = 5.1V)
Line regulation (220V ± 15% and to I_O = 1A) = 15mV (V_O = 5.1V)

APPLICATION INFORMATION (continued)

Fig. 29 - DC-DC converter 5.1V/4A, ± 12V/1A. A suggestion how to synchronize a negative output



L1, L3 = COGEMA 946043 (969051)
L2 = COGEMA 946044 (946045)

Fig. 30 - In multiple supplies several L4962s can be synchronized as shown

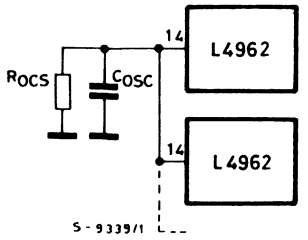
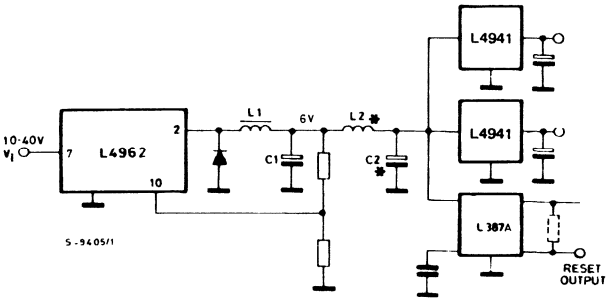


Fig. 31 - Preregulator for distributed supplies



* L2 and C2 are necessary to reduce the switching frequency spikes when linear regulators are remote from L4962

MOUNTING INSTRUCTION

The $R_{th\ j\text{-}amb}$ of the L4962 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 32).
The diagram of figure 33 shows the $R_{th\ j\text{-}amb}$ as a function of the side "ℓ" of two equal square copper areas having the thickness of 35μ (1.4 mils). During soldering the pins temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.
The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 32 - Example of P.C. board copper area which is used as heatsink

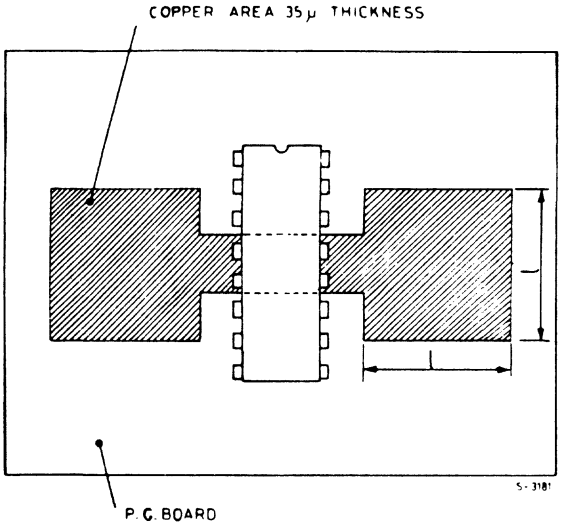
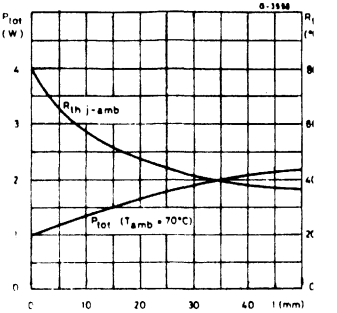


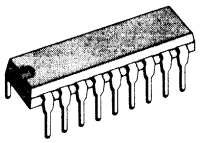
Fig. 33 - Maximum dissipable power and junction to ambient thermal resistance vs. side "ℓ"



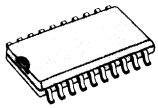
1.5A SWITCHING REGULATOR

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST/1)

- 1.5A OUTPUT LOAD CURRENT
- 5.1 TO 36V OUTPUT VOLTAGE RANGE
- DISCONTINUOUS VARIABLE FREQUENCY MODE
- PRECISE (+/–2%) ON CHIP REFERENCE
- VERY HIGH EFFICIENCY
- VERY FEW EXTERNAL COMPONENTS
- NO FREQ. COMPENSATION REQUIRED
- RESET AND POWER FAIL OUTPUT FOR MICROPROCESSOR
- INTERNAL CURRENT LIMITING
- THERMAL SHUTDOWN



Powerdip12+3+3



SO20

ORDERING NUMBERS:

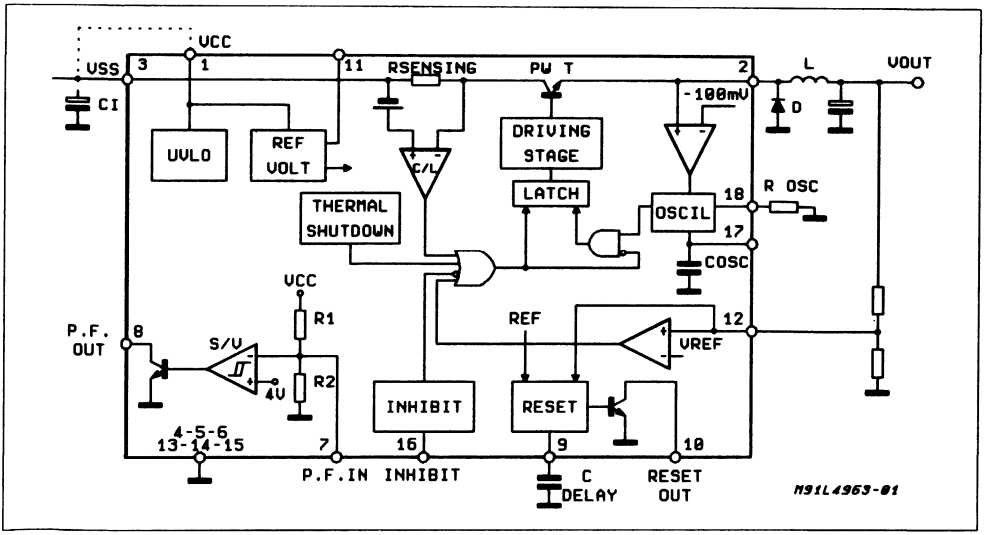
L4963W L4963D

DESCRIPTION

The L4963 is a monolithic power switching regulator delivering 1.5A at 5.1V. The output voltage is adjustable from 5.1V to 36V, working in discontinuous variable frequency mode. Features of the device include remote inhibit, internal current limiting and thermal protection, reset and power fail outputs for microprocessor.

The L4963 is mounted in a 12+3+3 lead Powerdip (L4963) and SO20 large (L4963D) plastic packages and requires very few external components.

BLOCK DIAGRAM



HIGH CURRENT SWITCHING REGULATOR

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST/1)

- 4 A OUTPUT CURRENT
- 5.1 V TO 28 V OUTPUT VOLTAGE RANGE
- 0 TO 100 % DUTY CYCLE RANGE
- PRECISE (± 3 %) ON-CHIP REFERENCE
- SWITCHING FREQUENCY UP TO 120 KHz
- VERY HIGH EFFICIENCY (UP TO 90 %)
- VERY FEW EXTERNAL COMPONENTS
- SOFT START
- RESET OUTPUT
- CURRENT LIMITING
- INPUT FOR REMOTE INHIBIT AND SYNCHRONUS PWM
- THERMAL SHUTDOWN

DESCRIPTION

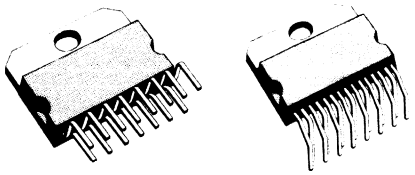
The L4964 is a stepdown power switching regulator delivering 4 A at a voltage variable from 5.1 V to 28 V.

Features of the device include overload protection, soft start, remote inhibit, thermal protection, a reset output for microprocessors and a PWM comparator input for synchronization in multichip configurations.

The L4964 is mounted in a 15-lead Multiwatt® plastic power package and requires very few external components.

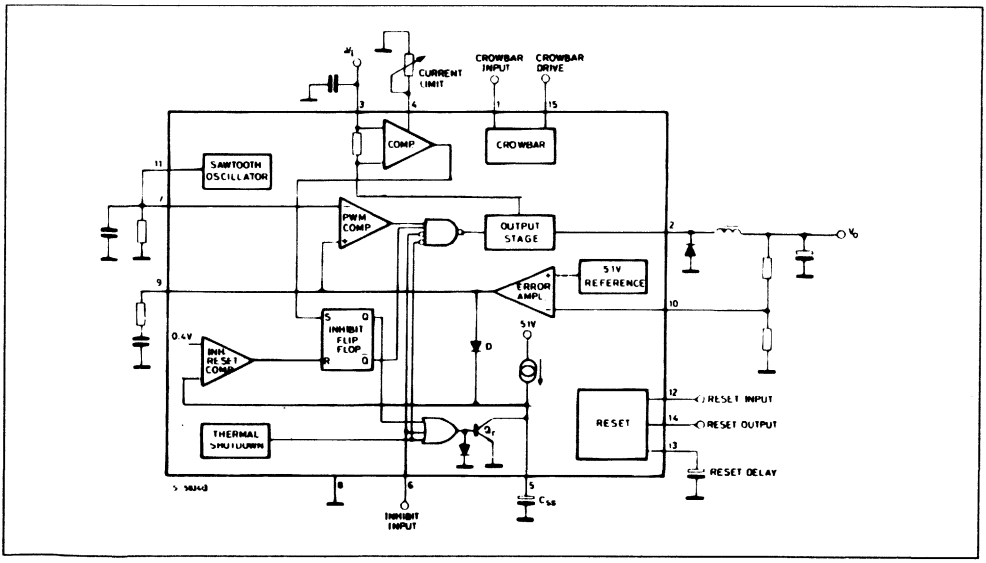
Efficient operation at switching frequencies up to 120 KHz allows a reduction in the size and cost of external filter components.

Multiwatt
(15-lead)



ORDER CODES : L4964
L4964HT

BLOCK DIAGRAM

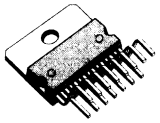


10A SWITCHING REGULATOR

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST/1)

- 10A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- 0 TO 90% DUTY CYCLE RANGE
- INTERNAL FEED-FORWARD LINE REGULATION
- INTERNAL CURRENT LIMITING
- PRECISE 5.1V ± 2% ON CHIP REFERENCE
- RESET AND POWER FAIL FUNCTIONS
- SOFT START
- INPUT/OUTPUT SYNC PIN
- UNDER VOLTAGE LOCK OUT WITH HYSTERETIC TURN-ON
- PWM LATCH FOR SINGLE PULSE PER PERIOD
- VERY HIGH EFFICIENCY
- SWITCHING FREQUENCY UP TO 500KHz
- THERMAL SHUTDOWN
- CONTINUOUS MODE OPERATION

MULTIPOWER BCD TECHNOLOGY



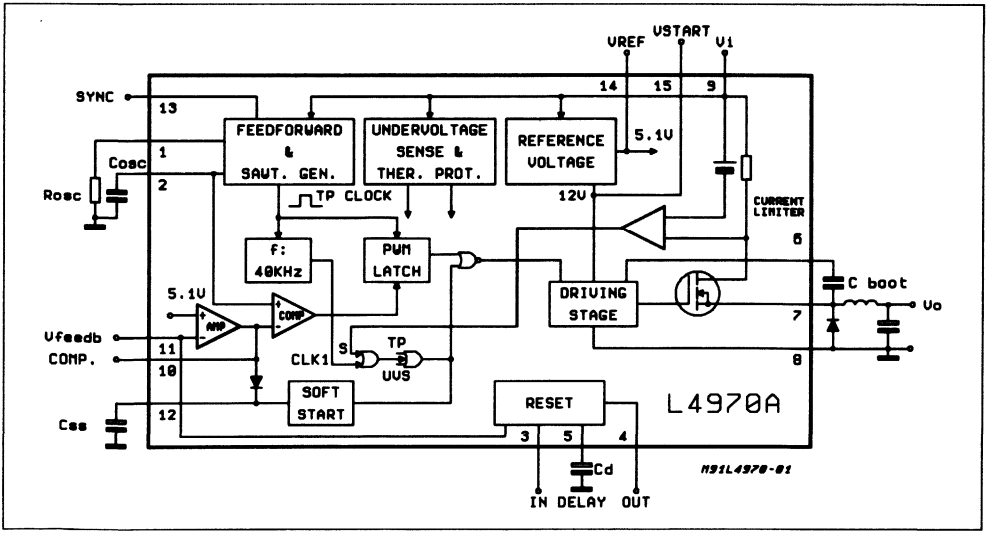
Multiwatt15V
ORDERING NUMBER: L4970A

DESCRIPTION

The L4970A is a stepdown monolithic power switching regulator delivering 10A at a voltage variable from 5.1 to 40V.

Realized with BCD mixed technology, the device uses a DMOS output transistor to obtain very high efficiency and very fast switching times. Features of the L4970A include reset and power fail for microprocessors, feed forward line regulation, soft start, limiting current and thermal protection. The device is mounted in a 15-lead multiwatt plastic power package and requires few external components. Efficient operation at switching frequencies up to 500KHz allows reduction in the size and cost of external filter components.

BLOCK DIAGRAM

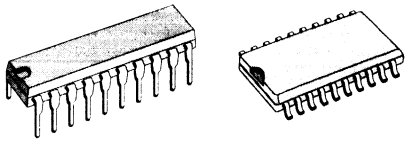


2A SWITCHING REGULATOR

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST/1)

- 2A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- 0 TO 90% DUTY CYCLE RANGE
- INTERNAL FEED-FORWARD LINE REG.
- INTERNAL CURRENT LIMITING
- PRECISE 5.1V ± 2% ON CHIP REFERENCE
- RESET AND POWER FAIL FUNCTIONS
- INPUT/OUTPUT SYNC PIN
- UNDER VOLTAGE LOCK OUT WITH HYSTERETIC TURN-ON
- PWM LATCH FOR SINGLE PULSE PER PERIOD
- VERY HIGH EFFICIENCY
- SWITCHING FREQUENCY UP TO 200KHz
- THERMAL SHUTDOWN
- CONTINUOUS MODE OPERATION

MULTIPOWER BCD TECHNOLOGY



POWERDIP (16 + 2 + 2)

SO20

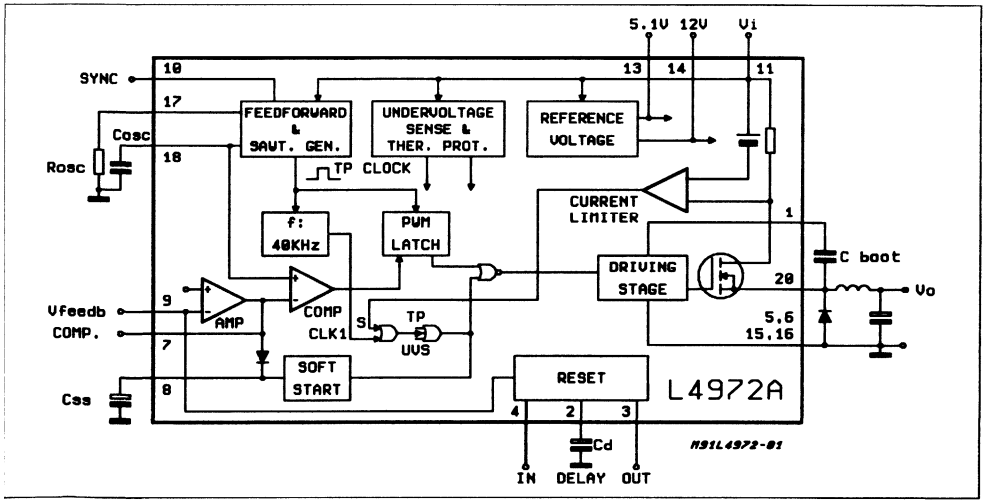
ORDERING NUMBERS : L4972A (Powerdip)
L4972AD (SO20)

DESCRIPTION

The L4972A is a stepdown monolithic power switching regulator delivering 2A at a voltage variable from 5.1 to 40V.

Realized with BCD mixed technology, the device uses a DMOS output transistor to obtain very high efficiency and very fast switching times. Features of the L4972A include reset and power fail for microprocessors, feed forward line regulation, soft start, limiting current and thermal protection. The device is mounted in a Powerdip 16 + 2 + 2 and SO20 large plastic packages and requires few external components. Efficient operation at switching frequencies up to 200KHz allows reduction in the size and cost of external filter component.

BLOCK DIAGRAM

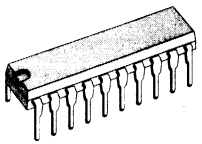


3.5A SWITCHING REGULATOR

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST/1)

- 3.5A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- 0 TO 90% DUTY CYCLE RANGE
- INTERNAL FEED-FORWARD LINE REG.
- INTERNAL CURRENT LIMITING
- PRECISE 5.1V ± 2% ON CHIP REFERENCE
- RESET AND POWER FAIL FUNCTIONS
- INPUT/OUTPUT SYNC PIN
- UNDER VOLTAGE LOCK OUT WITH HYSTERETIC TURN-ON
- PWM LATCH FOR SINGLE PULSE PER PERIOD
- VERY HIGH EFFICIENCY
- SWITCHING FREQUENCY UP TO 200KHz
- THERMAL SHUTDOWN
- CONTINUOUS MODE OPERATION

MULTIPOWER BCD TECHNOLOGY



POWERDIP (16 + 2 + 2)

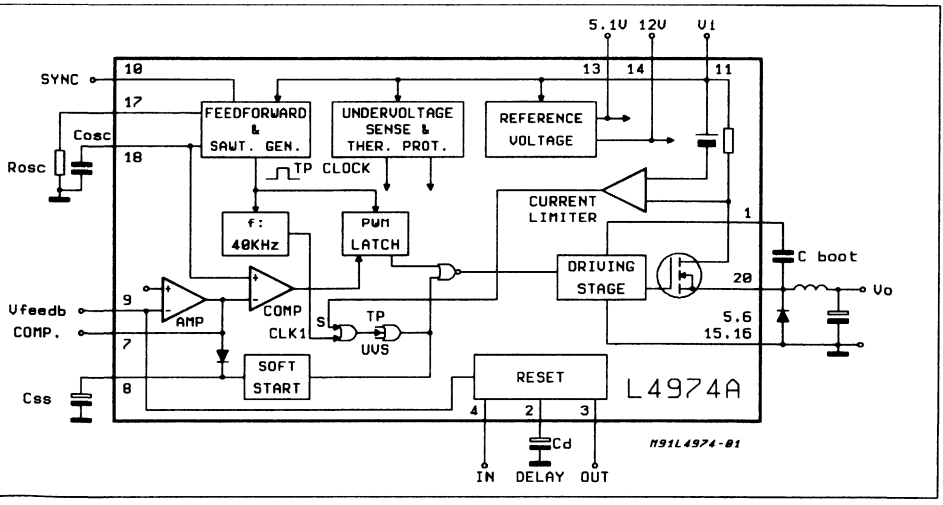
ORDERING NUMBER : L4974A

DESCRIPTION

The L4974A is a stepdown monolithic power switching regulator delivering 3.5A at a voltage variable from 5.1 to 40V.

Realized with BCD mixed technology, the device uses a DMOS output transistor to obtain very high efficiency and very fast switching times. Features of the L4974A include reset and power fail for microprocessors, feed forward line regulation, soft start, limiting current and thermal protection. The device is mounted in a Powerdip 16 + 2 + 2 plastic package and requires few external components. Efficient operation at switching frequencies up to 200KHz allows reduction in the size and cost of external filter component.

BLOCK DIAGRAM

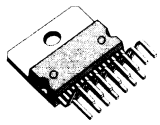


5A SWITCHING REGULATOR

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST/1)

- 5A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- 0 TO 90% DUTY CYCLE RANGE
- INTERNAL FEED-FORWARD LINE REGULATION
- INTERNAL CURRENT LIMITING
- PRECISE 5.1V ± 2% ON CHIP REFERENCE
- RESET AND POWER FAIL FUNCTIONS
- SOFT START
- INPUT/OUTPUT SYNC PIN
- UNDER VOLTAGE LOCK OUT WITH HYSTERETIC TURN-ON
- PWM LATCH FOR SINGLE PULSE PER PERIOD
- VERY HIGH EFFICIENCY
- SWITCHING FREQUENCY UP TO 500KHz
- THERMAL SHUTDOWN
- CONTINUOUS MODE OPERATION

MULTIPOWER BCD TECHNOLOGY



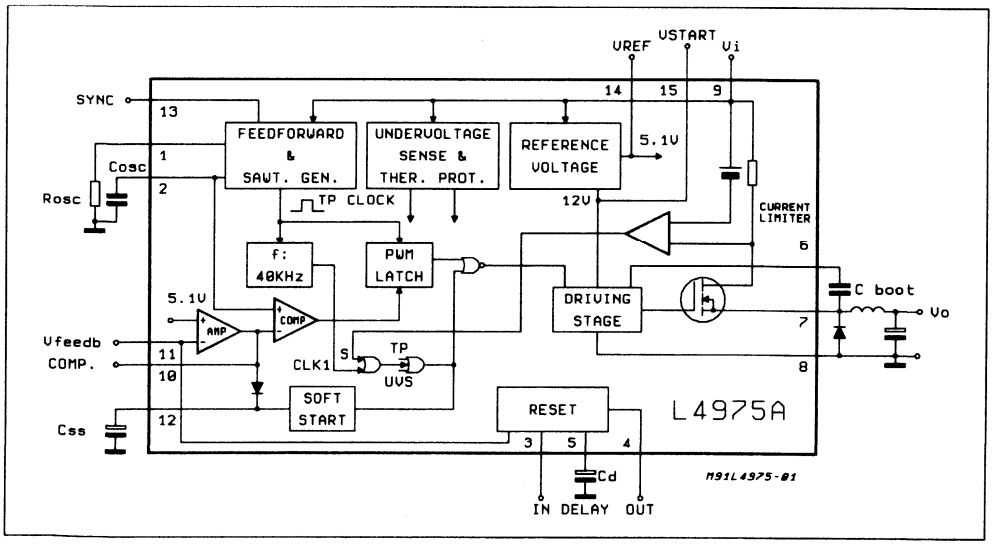
Multiwatt15V
ORDERING NUMBER: L4975A

DESCRIPTION

The L4975A is a stepdown monolithic power switching regulator delivering 5A at a voltage variable from 5.1 to 40V.

Realized with BCD mixed technology, the device uses a DMOS output transistor to obtain very high efficiency and very fast switching times. Features of the L4975A include reset and power fail for microprocessors, feed forward line regulation, soft start, limiting current and thermal protection. The device is mounted in a 15-lead multiwatt plastic power package and requires few external components. Efficient operation at switching frequencies up to 500KHz allows reduction in the size and cost of external filter components.

BLOCK DIAGRAM

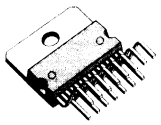


7A SWITCHING REGULATOR

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST/1)

- 7A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- 0 TO 90% DUTY CYCLE RANGE
- INTERNAL FEED-FORWARD LINE REGULATION
- INTERNAL CURRENT LIMITING
- PRECISE 5.1V ± 2% ON CHIP REFERENCE
- RESET AND POWER FAIL FUNCTIONS
- SOFT START
- INPUT/OUTPUT SYNC PIN
- UNDER VOLTAGE LOCK OUT WITH HYSTERETIC TURN-ON
- PWM LATCH FOR SINGLE PULSE PER PERIOD
- VERY HIGH EFFICIENCY
- SWITCHING FREQUENCY UP TO 500KHz
- THERMAL SHUTDOWN
- CONTINUOUS MODE OPERATION

MULTIPOWER BCD TECHNOLOGY



Multiwatt15V

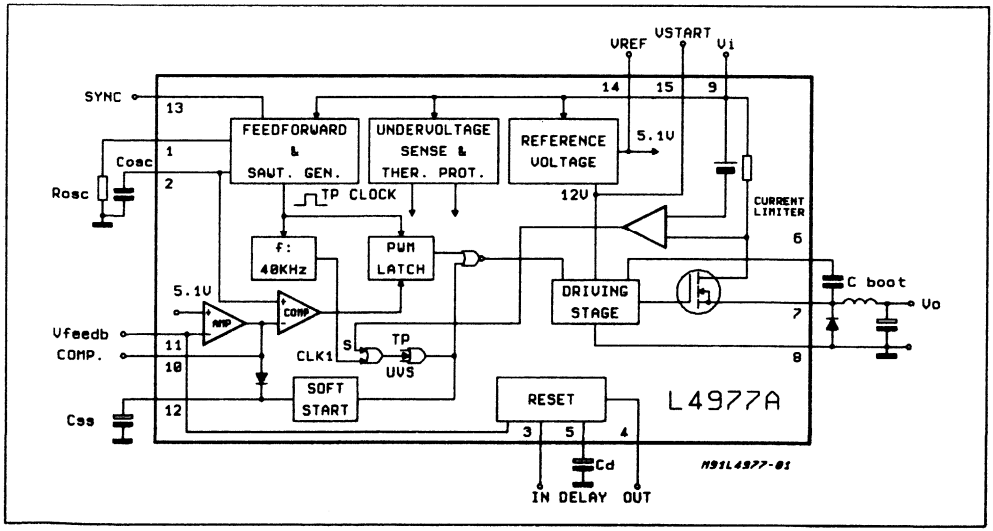
ORDERING NUMBER: L4977A

Realized with BCD mixed technology, the device uses a DMOS output transistor to obtain very high efficiency and very fast switching times. Features of the L4977A include reset and power fail for microprocessors, feed forward line regulation, soft start, limiting current and thermal protection. The device is mounted in a 15-lead multiwatt plastic power package and requires few external components. Efficient operation at switching frequencies up to 500KHz allows reduction in the size and cost of external filter components.

DESCRIPTION

The L4977A is a stepdown monolithic power switching regulator delivering 7A at a voltage variable from 5.1 to 40V.

BLOCK DIAGRAM



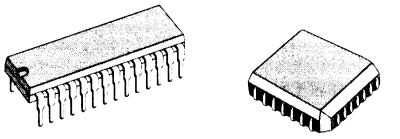
SGS-THOMSON MICROELECTRONICS

L5170

OCTAL LINE DRIVER

ADVANCE DATA

- OCTAL LINE DRIVER FOR:
  - EIA STD: RS232D; RS423A
  - CCIT: V.10; V.28
- NO EXTERNAL COMPONENTS
- VERY LONG TRANSMISSION LINE (5000ft)
- 50V EOS OUTPUT PROTECTION



DIP28 **PLCC28**

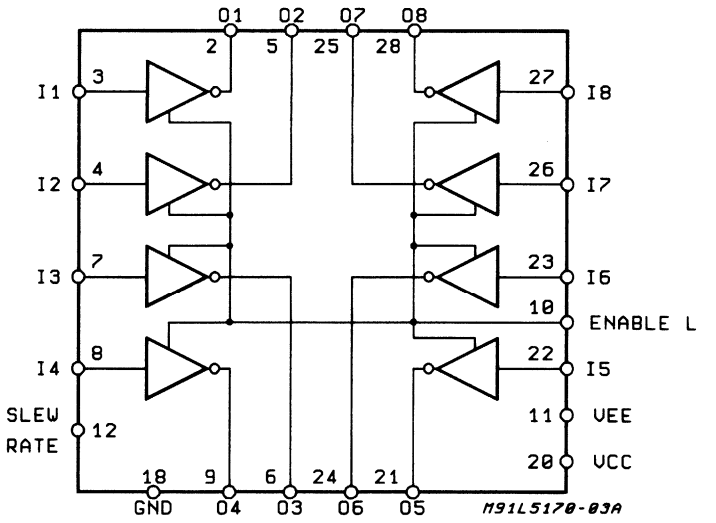
ORDERING NUMBERS:

L5170A L5170D

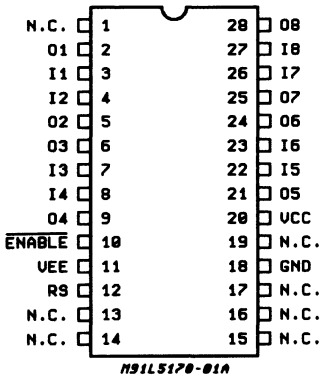
DESCRIPTION

L5170 is an octal line driver unit in DIP28 and PLCC28 packages intended for use in the EIA std RS232D, RS423A and CCITT V.10 and V.28 applications.
With no external components L5170 is able to drive a line up to 5000ft assuming the line capacitance is 35pF per ft and the capacitance of the filter, connectors/protection components add up to the total capacitance load. The drivers typically run in short circuit current mode whenever the cable attached is over 500ft.

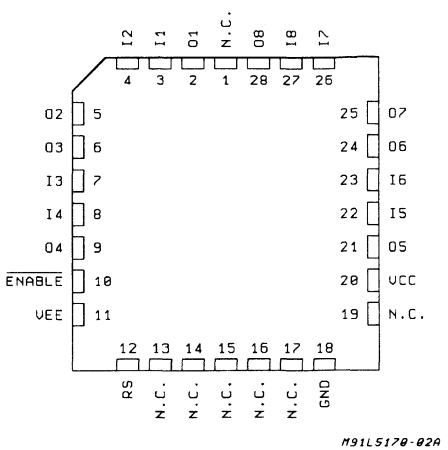
BLOCK DIAGRAM



PIN CONNECTIONS (Top views)



DIP28



PLCC28

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	+15	V
V_{EE}	Supply Voltage	– 15	V
V_i	Input Voltage (Enable Data)	– 1.5 to 7	V
V_O	Output Voltage	±6	V
I_O	Output Current (**)	±150	mA
SR	Minimum Slew Resistor (***)	1.5	1KΩ
P_{tot}	Power Dissipation at T_{amb} = 70°C **(PLCC28)** (*) **(DIP28)** (*)	1.2 1.3	W W
T_{op}	Operating Free Air Temperature Range	0 to +70	°C
T_{stg}	Storage Temperature Range	-65 to 150	°C

Notes:
(*) Mounted on board with minimized dissipating copper area.
(**) Minimum Current per driver. Do not exceed maximum power dissipation if more than one input is on.
(***) Minimum value of the resistor used to set the slew rate.

THERMAL DATA

Symbol	Description		PLCC28	DIP28	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient (*)	Max.	67	62	°C/W

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 9 to 11V; V_{EE} = − 9 to − 11V T_{amb} =0 to 70°C, unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{OH}	High Level Output Voltage	V_{in} = 0.8V R_L = inf R_L = 3KΩ R_L = 450Ω (see note 1)	 5 5 4.5		 6 6 6	 V V V
V_{OL}	Low Level Output Voltage	V_{in} = 2.4V R_L = inf R_L = 3KΩ R_L = 450Ω (see note 1)	 − 6 − 6 − 6		 − 5 − 5 − 4.5	 V V V
V_{OI}	Output Voltage Balance	$\|V_{CC}\| = \|V_{EE}\|$; R_L = 450Ω			0.4	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
V_{IK}	Input Clamp Voltage	I_{IN} = − 15mA	− 1.5			V
I_{IH}	High Level Input Current	V_{IN} = 2.4V			40	µA
I_{IL}	Low Level Input Current	V_{IN} = 0.4V	− 400			µA
I_{CC}	Positive Supply Current	V_{IN} = 2.4V; R_S = 2KΩ; R_L = 3KΩ C_L = 2.5nF; (See note 2)			30	mA
I_{CC1}	Positive Supply Current	V_{IN} = 0.4V; R_S = 2KΩ; R_L = 3KΩ C_L = 2.5nF; (See note 2)			40	mA
I_{EE}	Negative Supply Current	V_{IN} = 2.4V; R_S = 2KΩ; R_L = 3KΩ C_L = 2.5nF; (See note 2)	− 30			mA
I_{EE1}	Negative Supply Current	V_{IN} = 0.4V; R_S = 2KΩ; R_L = 3KΩ C_L = 2.5nF; (See note 2)	− 40			mA
I_{sh}	Output Short Circuit Current	V_O = 0V; V_{IN} = 2.4V; (see fig.1)	25		100	mA
I_{sl}	Output Short Circuit Current	V_O = 0V; V_{IN} = 2.4V; (see fig.1)	− 100		− 25	mA
I_{bal}	Output Current Balance	Ish/Isl = Ibal	0.625		1.6	mA/mA
I_x	Output Leakage Current	See fig.2,3 and note 3 V_O = 6V V_O = − 6V	 − 70		70	 µA µA
t_r	Rise time (see note 4 and 5; see figure 4A)	R_L = 450Ω; C_L = 50pF R_{slew} = 5.34KΩ ±1%	2		2.7	µs
t_{rc1}		R_L = 450Ω; C_L = 0.01µF R_{slew} = 10KΩ ±1%			10	µs
t_{rc2}		R_L = 450Ω; C_L = 0.1µF R_{slew} = 10KΩ ±1%			50	µs
t_{rc3}		R_L = 450Ω; C_L = 2.5nF R_{slew} = 2KΩ ±1%	0.65		1.2	µs
t_{rc4}		R_L = 450Ω; C_L = 2.5nF R_{slew} = 10KΩ ±1%	3.25		6	µs
t_f	Fall time (see note 4 and 5; see figure 4A)	R_L = 450Ω; C_L = 50pF R_{slew} = 5.34KΩ ±1%	2		2.7	µs
t_{fc1}		R_L = 450Ω; C_L = 0.01µF R_{slew} = 10KΩ ±1%			10	µs
t_{fc2}		R_L = 450Ω; C_L = 0.1µF R_{slew} = 10KΩ ±1%			50	µs
t_{fc3}		R_L = 450Ω; C_L = 2.5nF R_{slew} = 2KΩ ±1%	0.65		1.2	µs
t_{fc4}		R_L = 450Ω; C_L = 2.5nF R_{slew} = 10KΩ ±1%	3.25		6	µs

Note 1: The Output under load must not drop below 90% of the open circuit drive level.

Note 2: This represents the static condition only. Applications can see 130mA normal current draw for clock and data lines with up to 500mA transients when all lines are transitioning at the same time. Over 500ft of cable slew rate is governed by the drivers ability to sink current. The currents are rougly equivalent to the short circuit current.

AC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_{lz}	Output Enable to Output (see figure 4B)	R_L = 450Ω; C_L = 50pF R_{slew} = 10KΩ			5	µs
t_{nz}					5	µs
t_{zl}					150	µs
t_{zh}					150	µs
t_{plh}	Propagation (see figure 4C)	R_L = 450Ω; C_L = 50pF R_{slew} = 2KΩ	0.3		0.9	µs
t_{ph1}			0.3		0.9	µs

LINE TRANSIENT IMMUNITY (Considering the following cases: Powered ON, Powered OFF-Low impedance power supply and Powered OFF-High impedance supply).

ESD	Elettrostatic Discharge	Tested per MIL-STD-883 (see note 6)	2			KV
EOS	Electrical Overstress	Transient pulse both polarities for 100µs (see note 7)	50			V

Note 3: The output leakage is measured under the following conditions:
a) The Driver tristated
b) Power supply OFF, and the power pins shorted to Ground
c) Power supply OFF. Impedances between power pins open and power pins shorted to Ground.

Note 4: The output waveform should not show any signs of oscillations under any load variation between o.1VVss and 0.9Vss. The oscillation allowed when V_{SS} < 0.1V_{SS} and V_{ss} >0.9V_{ss} shall be 10% of V_{ss}.

Note 5: t_{fc1} thru t_{rc4} shall be within ±20% of t_{rc1} thru t_{rc4} respectively.

Note 6: All pins are required to withstand parameter.

Note 7: Output pins are required to withstand fig.5 without any degradation to the circuit.

TEST CIRCUIT

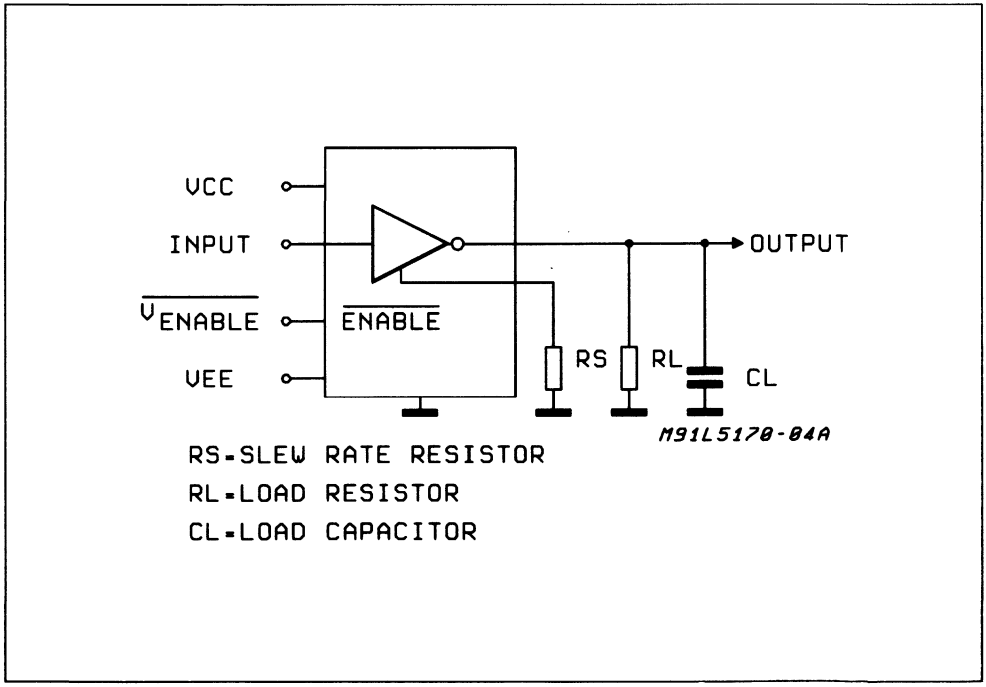


Figure 1: Output Leakage Test Circuit

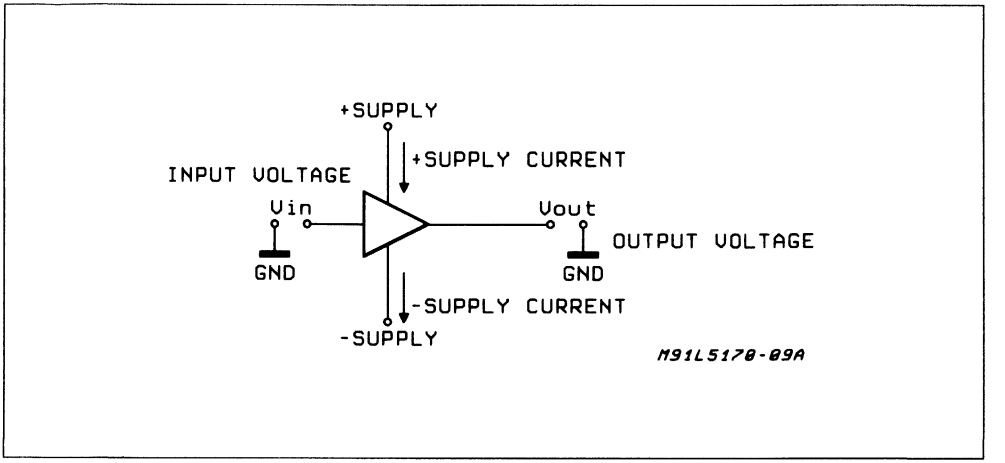


Figure 2: Output Voltage Rise Time

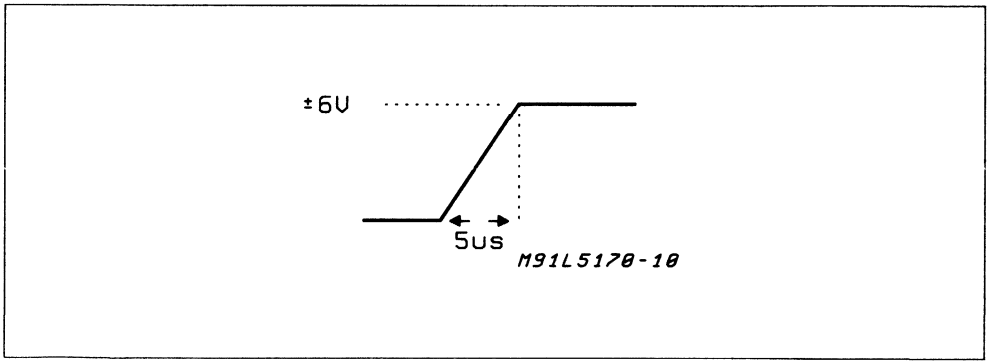


Figure 3: EOS Requirements

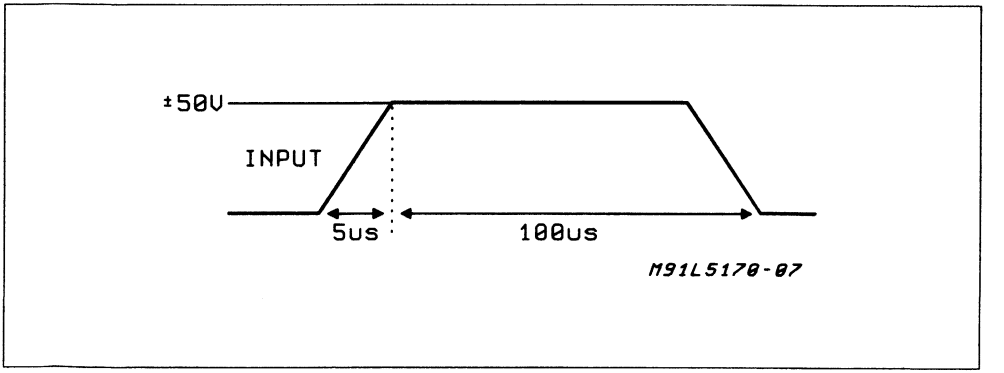
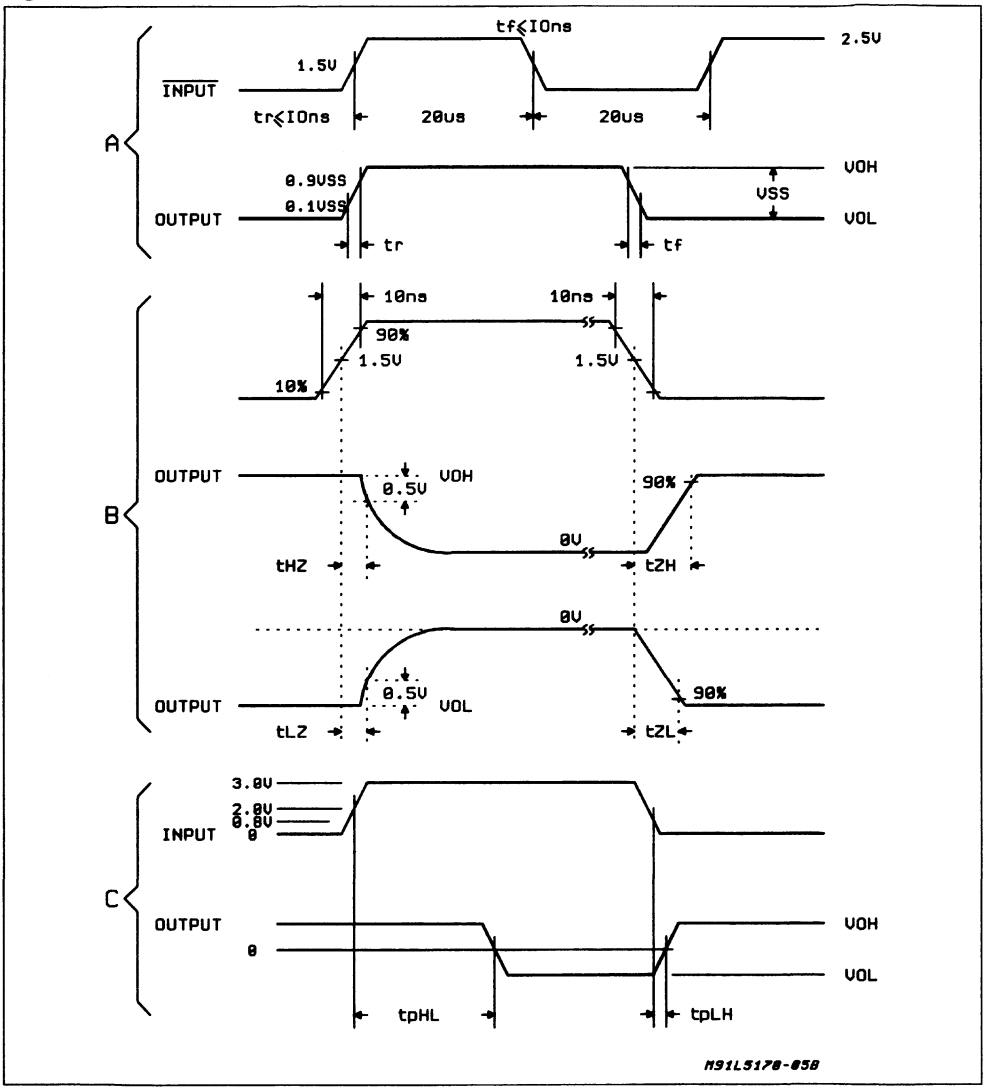


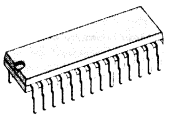
Figure 4: Waveforms



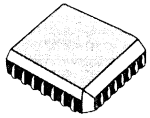
OCTAL LINE RECEIVER

PRODUCT PREVIEW

- OCTAL LINE RECEIVER FOR:
  - EIA STD RS232D, RS423A, RS422A
  - CCIT V.10, V.11, V.28, X.26
- NO EXTERNAL COMPONENTS
- INPUT FAIL SAFING CAPABILITY
- HIGH CROSSTALK REJECTION
- L6180 DATA RATE < 100KBIT/S
- L6181 DATA RATE < 1MBIT/S
- 50V EOS OUTPUT PROTECTION



DIP 28



PLCC 28

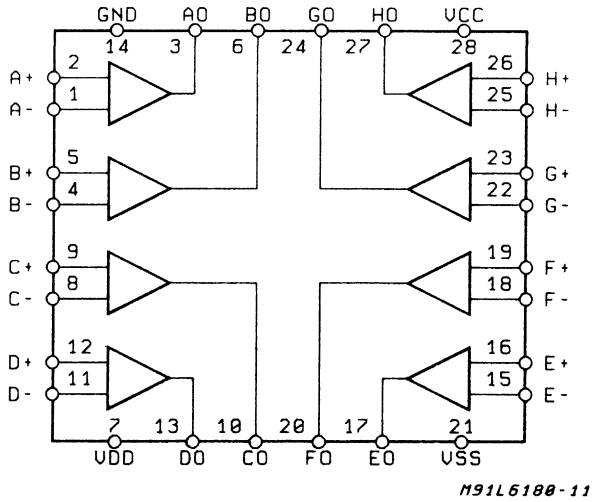
ORDERING NUMBER: L6180A DIP 28
L6180D PLCC28
L6181A DIP 28
L6181D PLCC28

DESCRIPTION

L6180/1 is an octal line receiver in a plastic DIP or PLCC designed to meet a wide range of digital communications requirements as outlined in the EIA standards RS232A without additional components, as well as the low speed applications of RS422A.

The receiver meets the CCIT recommendations V.10, V.11, X.26 and V.28 low speed applications (below 100KBS).
A low pass filter on the input starts to roll off at a frequency of 100KHz.

BLOCK DIAGRAM



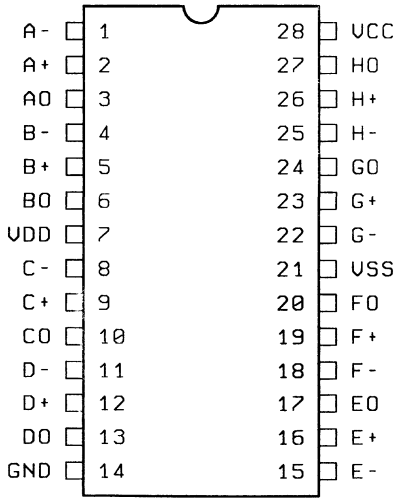
M91L6180-11

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	7	V
V_{DD}	Supply Voltage	13.5	V
V_{SS}	Logic Supply Voltage	-13.5	V
C_{RR}	Common Mode Range	±15	V
V_{ID}	Differential Input Voltage	±25	V
P_{tot}	Power Dissipation (PLCC 28)	800	mW
	Power Dissipation (DIP 28)	1200	mW
I_{OS}	Output Sink Current	50	mA
t	Output Short Circuit Time	1	sec
T_{op}	Operating Free Air Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature Range	-65 to 150	°C
	ESD	2KV max ESD 50µJ	
	Input Transient Protection	50V min EOS 100µs	

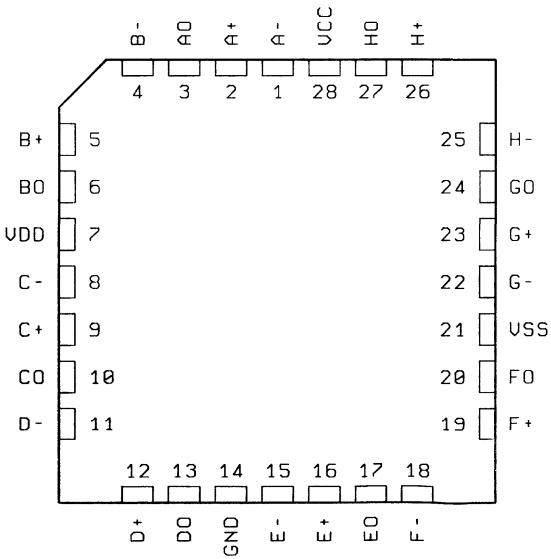
PIN CONNECTIONS (Top views)

DIP28



M91L6180-09

PLCC28



M91L6180-10

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±5%; V_{CM} = -7 to 7V; Tamb = 0 to 70°C; V_{SS} = -9 to 13.5V; V_{DD} = 9 to 13.5V; unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IN}	Input Current	(See Fig.1 and note2) V_{CC} = 0 to 5.25V; V_{SS}, V_{DD} = 0 to 13.5V V_{IN} = - 10 to 10V V_{IN} = - 15 to 15V			 ±3 ±4.25	 mA mA
R_I	Input Resistance	V_{IA} or V_{IB} = 3 to 15V; (see fig.1) $R_I = \frac{[(V_{IA} \text{ or } V_{IN}) - V_{IOC}]}{I_{IN}}$	3		7	KΩ
V_{FS}	Failsafe Output Voltage	I_O = -440µA (See Fig.3)	2.7			V
V_{OH}	High Level Output Voltage	V_{CC} = 4.75V; V_{ID} = -1V; I_{OH} = -440µA	2.7			V
V_{OL}	Low Level Output Voltage	V_{CC} = 5.25V; V_{ID} = -1V; I_{OL} = 2mA			0.4	V
V_{IT2}	V_{IOH} Comparator Threshold Voltage	(See Fig.4)	1.8	2.2	2.6	V
I_{IH2}	High Operating Threshold Voltage	V_{OL} = 0.4V; I_{OL} = 2mA; (See Fig.4)	-25		-75	mV
I_{IH1}	Low Operating Threshold Voltage	V_{OH} = 2.7V; I_O = -440µA (See Fig.4)	-125		-175	mV
V_H	Input Hysteresis Voltage	$\lvert V_{TH2} - V_{TH1} \rvert$	50		150	mV
V_{IOC1}	Open Circuit Input Voltage	Measured in accordance with V.28 and RS-232D (see note 4 and 7)		0.6	2	V
V_{IOCH}	Open Circuit Input Voltage	Measured in presence of AC Input Signal (see note 7)	3.5	4	4.5	V
I_{OS}	Open Short Circuit Current	V_{CC} = 5.25V; V_O = 0; V_{ID} = 1V; (see note 5)	20		100	mA
V_{IBV}	Input for Balance Test	(see Figure 7 and note 11)			0.4	V
C_I	Input Capacitance				100	pF
V_{CC}	Supply Current	V_{CC} = 4.75V to 5.25V; (see note 6)			100	mA
V_{dd}	Supply Current	V_{dd} = 9 to 3.5V; (see note 6)			30	mA
V_{SS}	Supplyt Current	V_{SS} = -9 to 13.5V; (see note 6)			30	mA
I_{OS}	Open Short Circuit Current	V_{CC} = 5.25V; V_O = 0; V_{ID} = 1V; (see note 5)	20		100	mA
T_{plh}	Propagation Delay Low to High	R_L = 390Ω; C_L = 50pF; $\lvert V_{IN} = 1V \rvert$; (see fig 5 test Circuit Fig. 6)	0		1500	ns
T_{phl}	Propagation Delay Low to High	R_L = 390Ω; C_L = 50pF; $\lvert V_{IN} = 1V \rvert$; (see fig 5 test Circuit Fig. 6)	0		1500	ns
V_{IOCH}	Delay V_{IOCL} to V_{IOCH} Switching	(see note 7A)			5	ms
V_{IOCL}	Delay V_{IOCH} to V_{IOCL} Switching	(see note 7B)	200			ms
V_{ist}	$\lvert T_{plh} - T_{phl} \rvert$	R_L = 390Ω; C_L = 50pF; $\lvert V_{IN} \rvert$ = 1V;(see fig. 5; Test Circuit Fig. 6)	0		500	ns
T_{SKEW1}	Skew between rec's in PKg Tp (1) hl/1h - Tp (2) hl/1h	R_L = 390Ω; C_L = 50pF; $\lvert V_{IN} \rvert$ = 1V;(see fig. 5; Test Circuit Fig. 6)	0		300	ns
f_A	Frequency Accepted (Receiver will Output)	V_{IN} = 200mVpp; (see fig. 8 and note 7;	100			KHz

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±5%; V_{CM} = -7 to 7V; Tamb = 0 to 70°C; V_{SS} = -9 to 13.5V; V_{DD} = 9 to 13.5V; unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
f_R	Frequency Rejected (No Receiver Output)	V_{IN} = 2Vpp; (see fig. 8 and note 7)		5		MHz

Note:

1) The algebric convention, where the less positive (more negative) is designed the minimum

2) With the voltage V_{IA} or (V_{IB}) ranging between ±15V, while V_{IB} or (V_{IA}) is open or grounded, the resultant input current I_{IA} or (I_{IB}) shall remain within the shaded region shown in the graph in Fig.1.

3) Either Point B' or Point A' is grounded in Figure 1

4) V_{ICC} measured from grounded to (+) input with (-) input grounded
V_{ICC} measured from grounded to (+) input with (-) input grounded

5) Not more than one output should be shorted at a time and for less than 1 seond

6) The sum of the product of the maximum supply currents and voltages cannot exceed themaximum power dissipation

7) A: The conditions for the inpit switching from V_{IOCL} to V_{IOCH} mode is: V_{id} in start bit "spacing condition"for less than TpV_{ioch} (5ms).
B: The conditions for the input switching from V_{IOCH} to V_{IOCL} mode is: Vid > W_{W2} for greater than TpV_{IOCL} (200ms)

8) An example of a frequency response plot meeting the rejection/acceptance requirements is provided in figure 8.

LINE TRANSIENT IMMUNITY (Considering the following cases; powered ON, Powered OFF-LOW impedance power supply and powered OFF-HIGH impedance supply)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
ESD	Static	tested per MIL-STD-883 (see note 9)	2			KV
EOS	Stress	transient pulse both polarities for 100µs (see note 9 and Fig. 2)	50			V

Note:

9) All pins are required to withstand this parameters.

10) Input pins are required to withstand fig.2 without any degradation to the circuit.

11) The balance test requirement can be met by use of a current limit circuit which reduces the input bias current I_{ib} (see figure 7) for input voltages below a threshold voltage given by (I_{ib} x 1K) - 400mV.

Figure 1: Input Current Voltage Mesurements

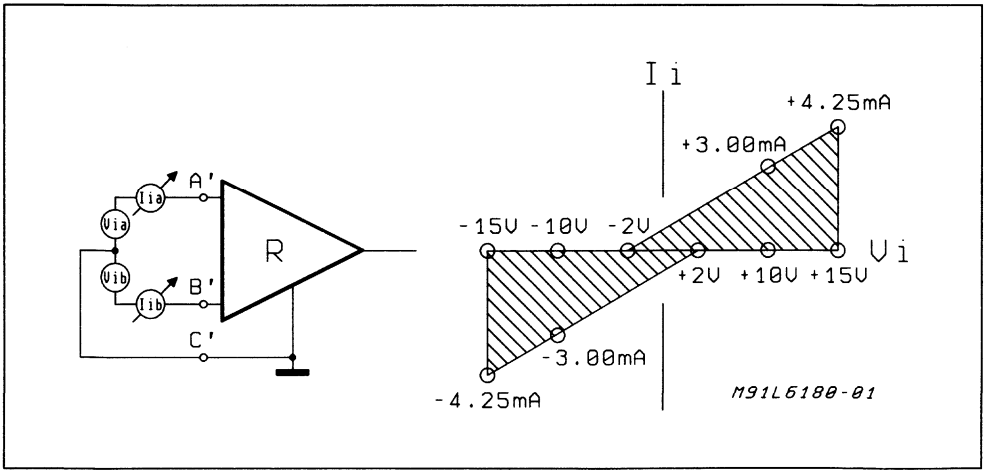


Figure 2: EOS Requiremets

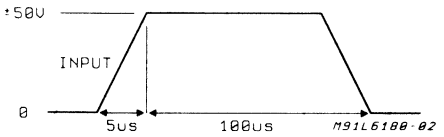
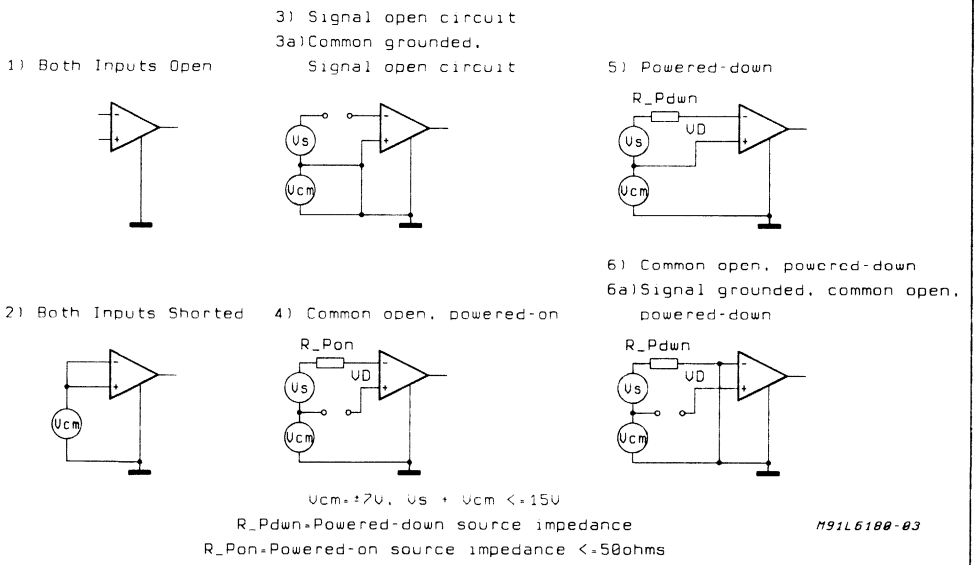


Figure 3: Output Failsafing



The output assumes a logic "1"under the following conditions, (see figure 3)

Both inputs open

2 Both inputs shorted

3 Signal Opencircuit

3a Common grounded, signal open circuit

4 Common open, generator powered-on

5 Generator powered-down (see note 7)

6 Common open, generator powered-down

6a Signal grounded, common open, generator powered-down

7 Less than 250mVpp differential signal

Figure 4: Threshold voltage definition

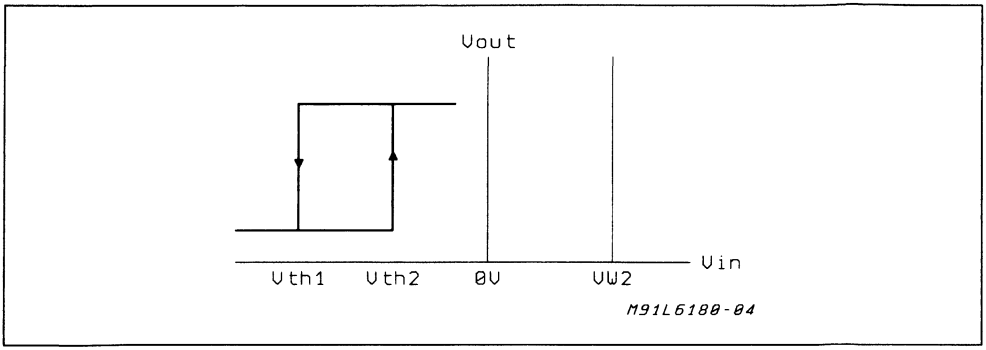


Figure 5: Propagation Delay

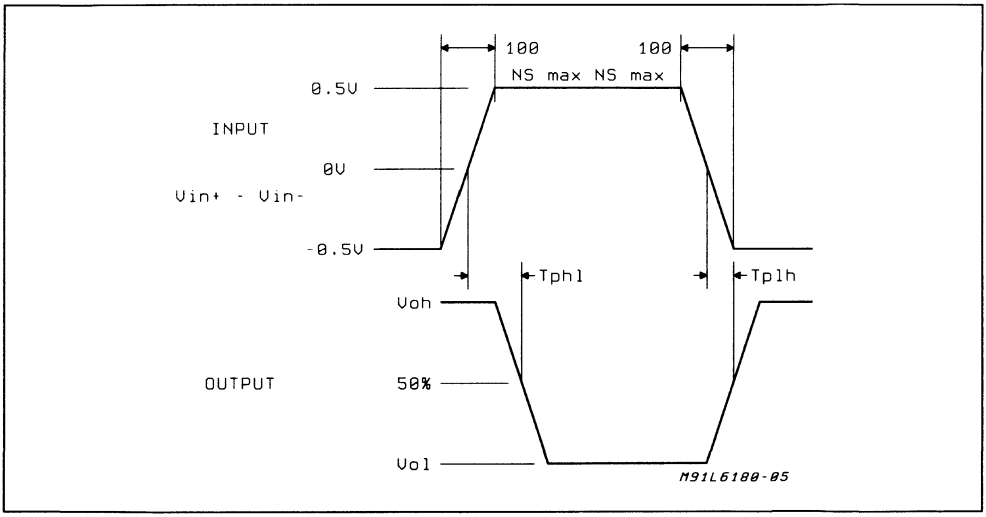


Figure 6: AC Test Circuit

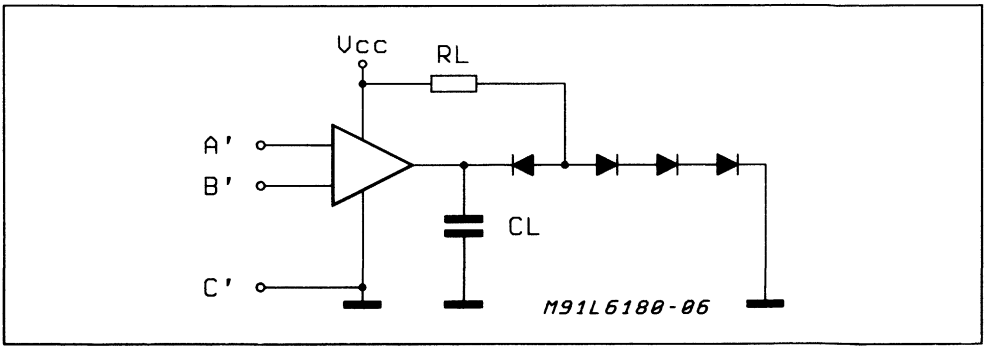
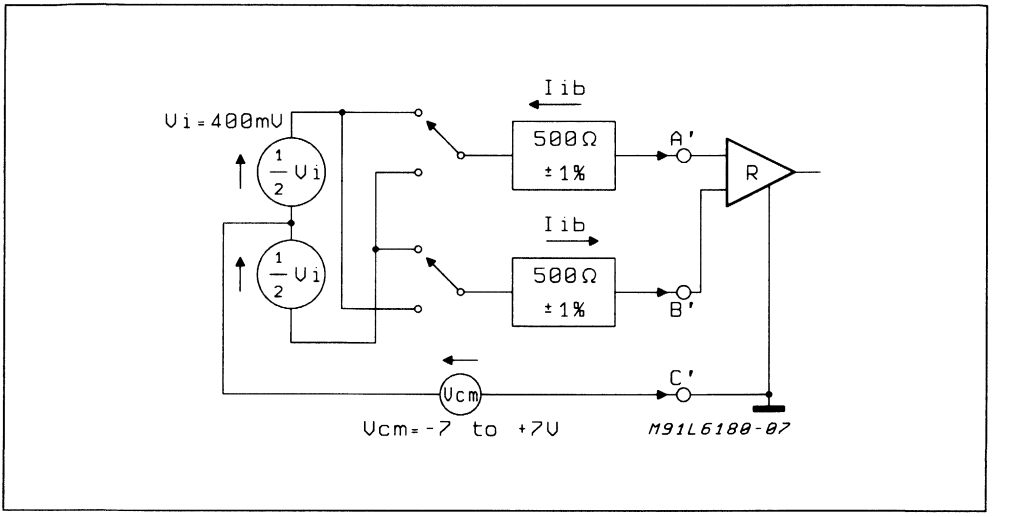


Figure 7: Receiver input Balance Measurement



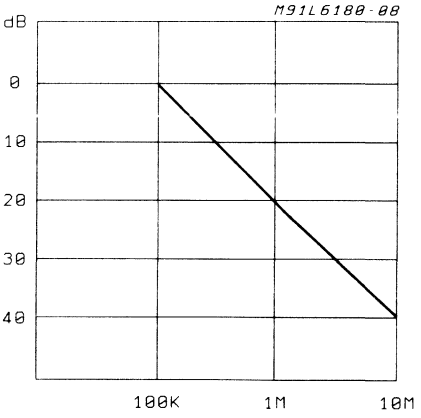
INPUT BALANCE MEASUREMENT

The balance of the receiver input voltage-current characteristics and bias voltages shall be such that the receiver will remain in the intended binary state when a differential voltage Vi of 400mV is applied through 500Ω ±1% to each input terminal, as shown above, and Vcm is varied between -7 and +7V.

When the polarity of Vi is reversed, the opposite binary state shall be maintained under the same conditions. Maintain input balance with input B common with another receiver.

The voltage input (V_{IN}) rejection is checked at the center point between the High Operating Threshold (V_{th2}) and the Low OperatingThreshold (V_{th1})

Figure 8: High Frequency Signal Rejection



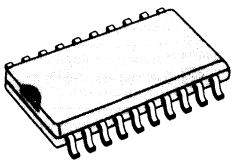
SGS-THOMSON MICROELECTRONICS

L6242

VOICE COIL MOTOR DRIVER

ADVANCE DATA

- OUTPUT CURRENT UP TO 1A
- OPERATES AT LOW VOLTAGES WITH LOW COIL RESISTANCE OF THE MOTOR
- LARGE COMMON MODE AND DIFFERENTIAL MODE RANGE
- LOW INPUT OFFSET VOLTAGE
- THERMAL SHUT-DOWN
- ENABLE FUNCTION
- INTERNAL CLAMP DIODES



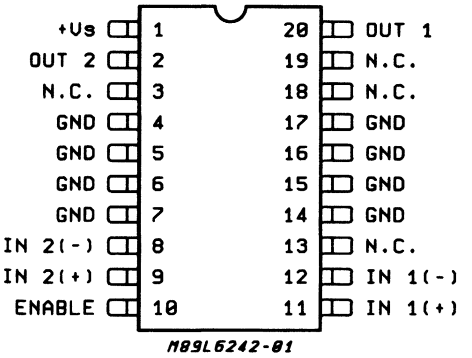
SO20

ORDERING NUMBER: L6242

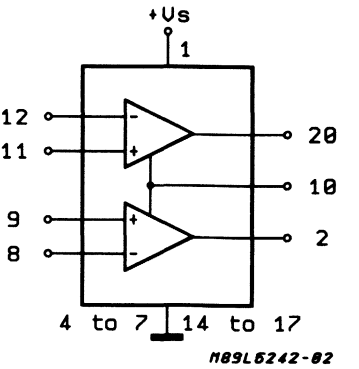
DESCRIPTION

The L6242 is a monolithic integrated circuit in SO-20 package intended for use as a dual power operational amplifier. It is particularly indicated for driving inductive loads as linear motor, and finds application in Hard Disc, Compact-Disc, etc.
The two power operational amplifiers are controlled by a common enable input.
The high gain and output power capability provide superior performance whatever a power booster is required.

PIN CONNECTION AND BLOCK DIAGRAM



M89L6242-01



M89L6242-02

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	28	V
V_i	Input Voltage	VS	V
V_i	Differential Input Voltage	$\pm V_S$	V
I_O	DC Output Current	1	A
I_P	Peak Output Current (non repetitive)	1.5	A
P_{tot}	Maximum Power Dissipation at T_{amb} = 85°C T_{CASE} = 75°C	1 5	W W
T_{stg}, T_J	Storage and Junction Temperature Range	-40 to 150	°C

ELECTRICAL CHARACTERISTICS (V_S = 12V, T_J = 25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		4		28	V
I_S	Quiescent Drain Current	$V_O = V_S/2$		10	15	mA
I_b	Input Bias Current			0.2	1	µA
V_{OS}	Input Offset Voltage				15	mV
I_{OS}	Input Offset Current			10	50	nA
S_r	Slew Rate			1.5		V/µs
R_i	Input Resistance		500			KΩ
G_V	Open Loop Voltage Gain	f = 100Hz	70	80		dB
CMR	Common Mode Rejection	f = 100Hz	66	84		dB
SVR	Supply Voltage Rejection	f = 100Hz R_g = 10KΩ V_r = 0.5V		54		dB
V_{drop}	High Drop Voltage	I = 100mA I = 500mA		0.7 1	 1.5	V V
V_{drop}	Low Drop Voltage	I = 100mA I = 500mA		0.3 0.6	 1	V V
T_{sd}	Thermal Shutdown Junction Temperature			145		°C
R_p	Internal Pull-up Resistor of the Enable Input				50	KΩ
V_e	Enable Low Voltage	T_J = 130°C	-0.3		1.2	V
I_{eq}	Quiescent Drain Current	En = L		2	5	mA
T_d	Enable Delay				50	µs
I_{ol}	Output Leakage Current			10		µA

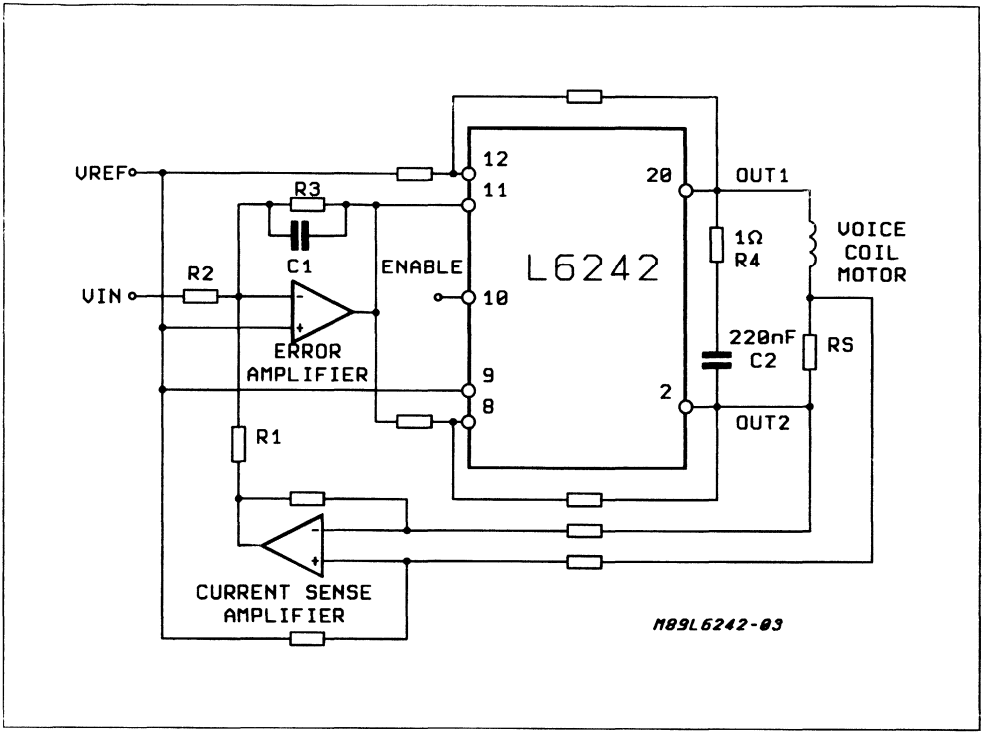
APPLICATION INFORMATIONS

Figure 1 shows the L6242 configurated as a transconductance amplifier, in order to drive linear motors as Voice Coil (VCM). The L6242 provides the power section of the Transconductance Amplifier. The two OP AMP are configurated one as inverting and the other as noninverting amplifier, with the same gain. Working in push-pull, they can be configurated as a bridge. The motor current can be controlled by means of the sense resistor (typical 1Ω) in series with the motor. The current sense amplifier provides the feedback signal, which is summed to the driving signal at the node which is the inverting input of the Error Amplifier. R1 closes the control loop. R2 converts the input voltage signal, into a current signal.

The snubber network provides the system stability, always required by the application. The network is directly connected to the output pins of the IC, OUT1 and OUT2, and in parallel with the load. R4 and C2 could be of different values, depending on the p.c.b. configuration and on the motor characteristics.

The DC transfer function may be expressed as:
gm = Iout/Vin = k • (R1/R2)
where k = 1/(Rsense • Ad)
and Ad = gain of the current sense amplifier.

Figure 1: Voice Coil Motor Control Circuit



OPTIMIZING LAYOUT

Optimizing a PC board layout involves to observe the following rules which in general can avoid application problems associated with ground loops and anomalous recirculation currents. The electrolytic capacitor for the power supply must be kept as close to the IC as possible. It is important that power grounds are close to each other on a wide enough. Copper side also, it is important to separate on the board the logic ground and the power ground in such a way that the ground traces for the logic signals and references do not cross the ground traces for the power signals. Logic ground and power ground must meet at one point on the board (startpoint grounding) far enough away from where the power ground traces terminate to ground (sense resistors and recirculation diodes). This is to avoid anomalous interface with the logic signals. It is generally a good idea to connect a non inductive capacitor (typically 100nF) between the pins VS and GND. In other cases it may be necessary to also place a by-pass capacitor between the pins Vref and GND.

SGS-THOMSON MICROELECTRONICS

L6506
L6506D

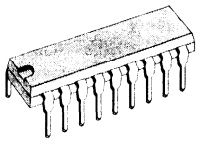
CURRENT CONTROLLER FOR STEPPING MOTORS

ADVANCE DATA

DESCRIPTION

The L6506/D is a linear integrated circuit designed to sense and control the current in stepping motors and similar devices. When used in conjunction with the L293, L298, L7150, L6114/L6115, the chip set forms a constant current drive for an inductive load and performs all the interface function from the control logic thru the power stage.

Two or more devices may be synchronized using the sync pin. In this mode of operation the oscillator in the master chip sets the operating frequency in all chips.

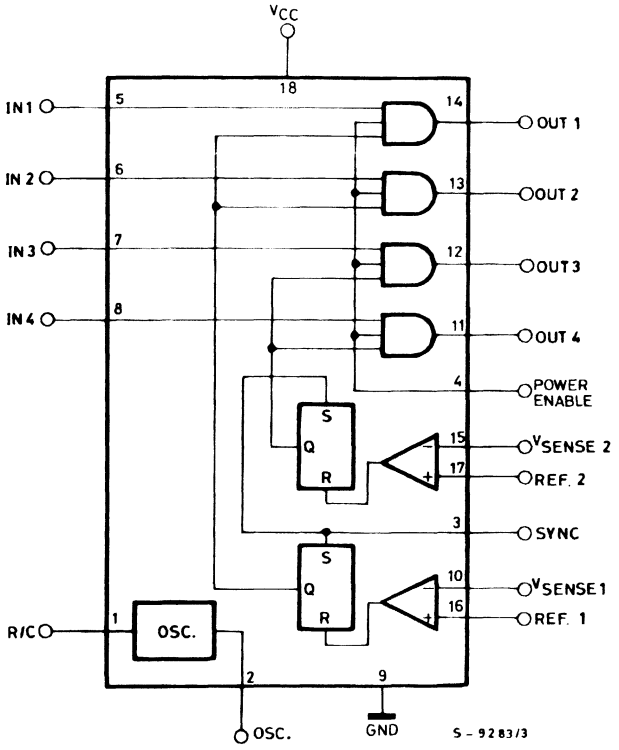


DIP-18 **SO-20**

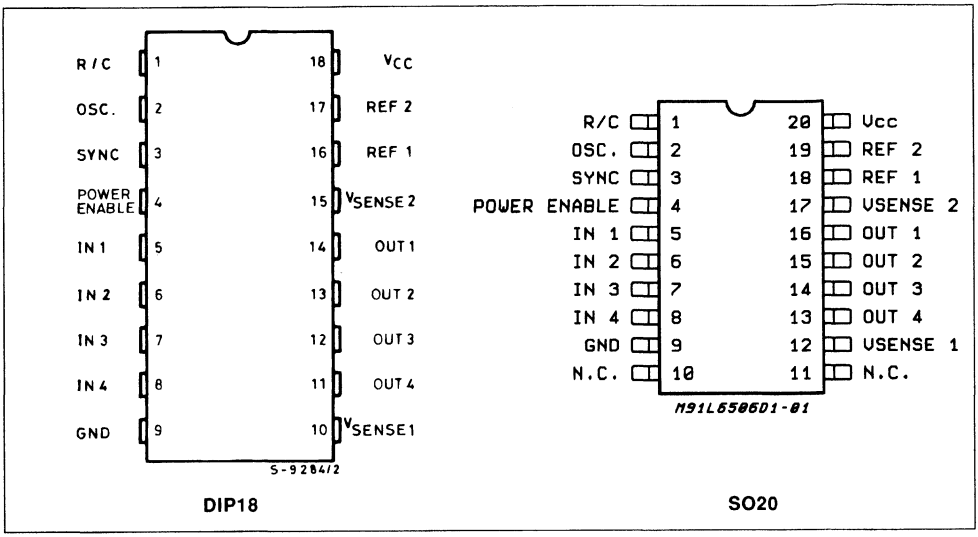
ORDERING NUMBERS:

L6506 L6506D1

BLOCK DIAGRAM (pin's number referred to DIP-18)



PIN CONNECTIONS (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	10	V
V_i	Input Signals	7	V
P_{tot}	Total Power Dissipation (T_{amb} = 70°C) for DIP18 for SO20	1 0.8	W W
T_j	Junction Temperature	150	°C
T_{stg}	Storage Temperature	-40 to 150	°C

THERMAL DATA

Symbol	Parameter		DIP18	SO20	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	80	100	°C/W

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_{amb} = 25 °C ; unless otherwise noted)

Symbol	Parameter	Test Condtions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		4.5		7	V
I_{CC}	Quiescent Supply Current	V_{CC} = 7 V			25	mA

COMPARATOR SECTION

V_{IN}	Input Voltage Range	V_{sense} Inputs	– 0.3		3	V
V_{IO}	Input Offset Voltage	V_{IN} = 1.4 V			± 5.0	mV
I_{IO}	Input Offset Current				± 200	nA
I_{IB}	Input Bias Current				1	µA
	Response Time	V_{REF} = 1.4 V V_{SENS} = 0 to 5 V		0.8	1.5	µs

ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit

COMPARATOR SECTION PERFORMANCE (over operating temperature range)

V_{IO}	Input Offset Voltage	V_{IN} = 1.4 V			± 20	mV
I_{IO}	Input Offset Current				± 500	nA

LOGIC SECTION(over operating temperature range) - (TTL compatible inputs & outputs)

V_{IH}	Input High Voltage		2.0		V_s	V
V_{IL}	Input Low Voltage				0.8	V
V_{OH}	Output High Voltage	V_{CC} = 4.75 V I_{OH} = 400 µA	2	3.5		V
V_{OL}	Ouptut Low Voltage	V_{CC} = 4.75 V I_{OH} = 4.0 mA		0.25	0.4	V
I_{OH}	Ouput Source Current Outputs 1 - 4	V_{CC} = 4.75 V	2.75			mA

OSCILLATOR

f_{osc}	Frequency Range		5		70	KHz
V_{thL}	Lower Threshold Voltage			0.33 V_{CC}		V
V_{thH}	Higher Threshold Voltage			0.66 V_{CC}		V
R_i	Internal Discharge Resistor		0.7	1	1.3	KΩ

CIRCUIT OPERATION

The L6506 is intended for use with dual bridge drivers, such as the L298, quad darlington arrays, such as the L7150, quad DMOS array such as L6114-L6115, or discrete power transistors to drive stepper motors and other similar loads. The main function of the device is to sense and control the current in each of the load windings.

A common on-chip oscillator drives the dual chopper and sets the operating frequency for the pulse width modulated drive. The RC network on pin 1 sets the operating frequency which is given by the equation :

$$f = \frac{1}{0.69\ RC} \quad \text{for } R > 10\ K$$

The oscillator provides pulses to set the two flip-flops which in turn cause the outputs to activate the drive. When the current in the load winding reaches the programmed peak value, the voltage across the sense resistor (R_{sense}) is equal to V_{ref} and the corresponding comparator resets its flip-flop interrupting the drive current until the next oscillator pulse occurs. The peak current in each winding is programmed by selecting the value of the sense resistor and V_{ref}. Since separate inputs are provided for each chopper, each of the loads may be programmed independently allowing the device to be used to implement microstepping of the motor. Lower threshold of L6506's oscillator is 1/3 V_{CC}. Upper threshold is 2/3 V_{CC} and internal discharge resistor is 1 KΩ ± 30 %.

Ground noise problems in multiple configurations can be avoided by synchronizing the oscillators. This may be done by connecting the sync pins of each of the devices with the oscillator output of the master device and connecting the R/C pin of the unused oscillators to ground.

The equations for the active time of the sync pulse (T2), the inactive time of the sync signal (T1) and the duty cycle can be found by looking at the figure 1 and are :

$$T2 = 0.69\ C1\ \frac{R1\ R_{IN}}{R1 + R_{IN}} \qquad (1)$$

$$T1 = 0.69\ R1\ C1 \qquad (2)$$

$$DC = \frac{T2}{T1 + T2} \qquad (3)$$

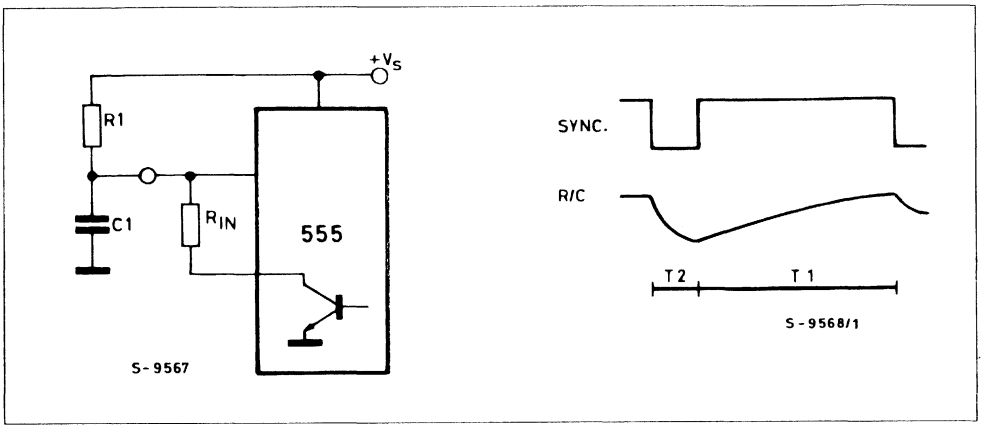
By substituting equations 1 and 2 into equation 3 and solving for the value of R1 the following equations for the external components can be derived :

$$R1 = (\frac{1}{DC} - 2)\, R_{IN} \quad (4)$$

$$C1 = \frac{T1}{0.69\ R1} \quad (5)$$

Looking at equation 1 it can easily be seen that the minimum pulse width of T2 will occur when the value of R1 is at its minimum and the value of R1 at its maximum. Therefore, when evaluating equation 4 the minimum value for R1 of 700Ω (1 KΩ – 30 %) should be used to guarantee the required pulse width.

Figure 1 : Oscillator Circuit and Waveforms.



APPLICATIONS INFORMATION

The circuits shown in figure 2 use the L6506 to implement constant current drives for stepper motors. Figure 2 shows the L6506 used with the L298 to drive a 2 phase bipolar motor. The peak current can be calculated using the equation :

$$I_{peak} = \frac{V_{ref}}{R_{sense}}$$

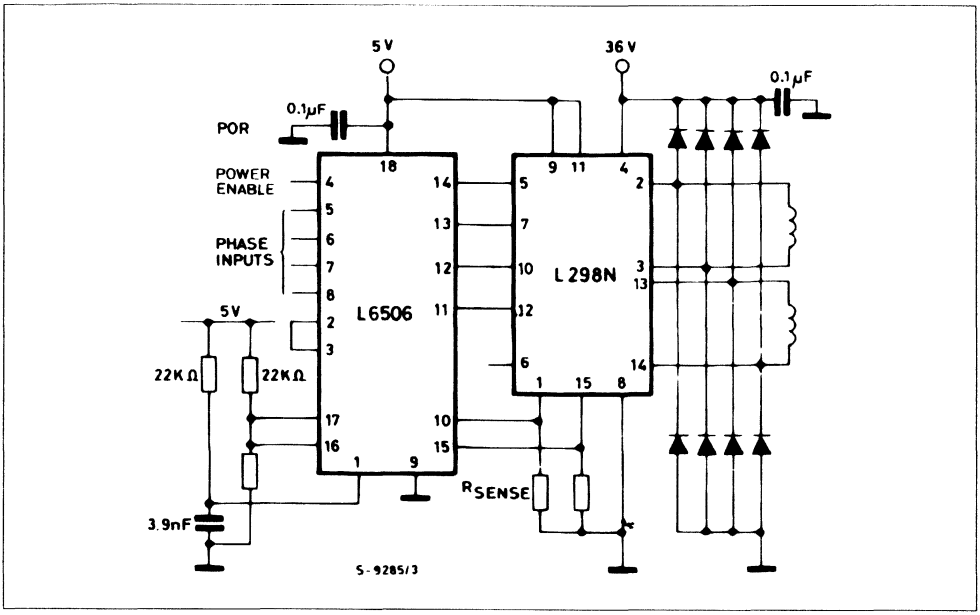
The circuit of Fig.2 can be used in applications requiring different peak and hold current values by modifying the reference voltage.

The L6506 may be used to implement either full step or half step drives. In the case of 2 phase bipolar stepper motor applications, if a half step drive is used, the bridge requires an additional input to disable the power stage during the half step. If used in conjunction with the L298 the enable inputs may be used for this purpose.

For quad darlington array in 4 phase unipolar motor applications half step may be implemented using the 4 phase inputs.

The L6506 may also be used to implement microstepping of either bipolar or unipolar motors.

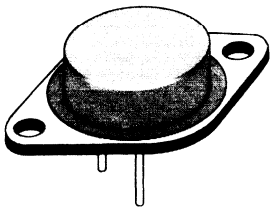
Figure 2 : Application Circuit Bipolar Stepper Motor Driver. (pin's number referred to DIP18)



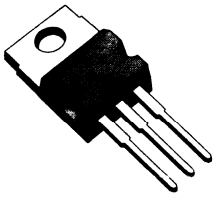
POSITIVE VOLTAGE REGULATORS

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST/1)

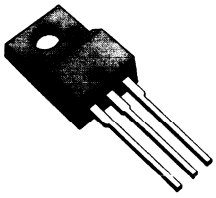
- OUTPUT CURRENT UP TO 1.5A
- OUTPUT VOLTAGES OF 5; 5.2; 6; 8; 8.5; 9; 12; 15; 18; 20; 24V
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTOR SOA PROTECTION



TO-3



TO-220

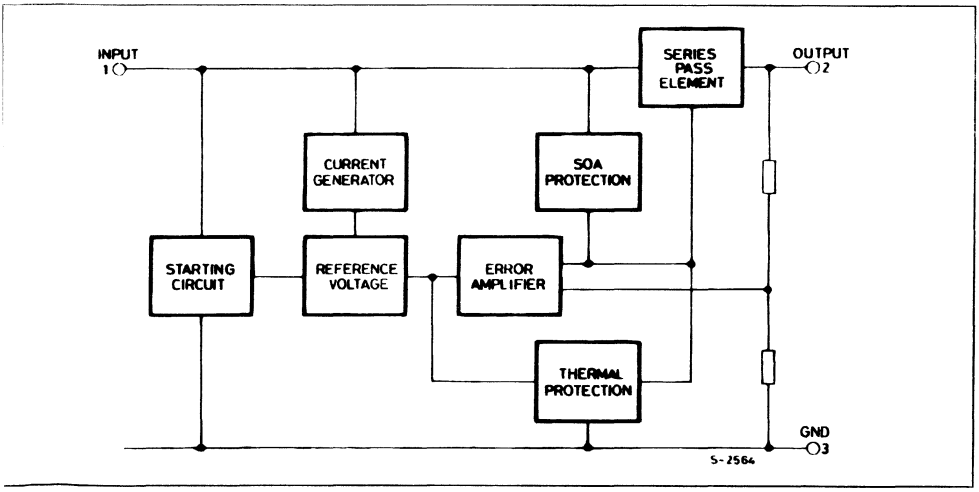


ISOWATT220

DESCRIPTION

The L7800 series of three-terminal positive regulator is available in TO-220, ISOWATT220 and TO-3 packages and with several fixed output voltages making it useful in a wide range of applications. These regulators can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

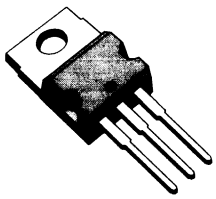
BLOCK DIAGRAM



PRECISION 1A REGULATORS

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST/1)

- OUTPUT CURRENT IN EXCESS OF 1A
- OUTPUT VOLTAGES OF 5; 6; 8; 9; 12; 15; 18; 24V
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTOR SOA PROTECTION
- 2% OUTPUT VOLTAGE TOLERANCE
- GUARANTEED IN EXTENDED TEMPERATURE RANGES

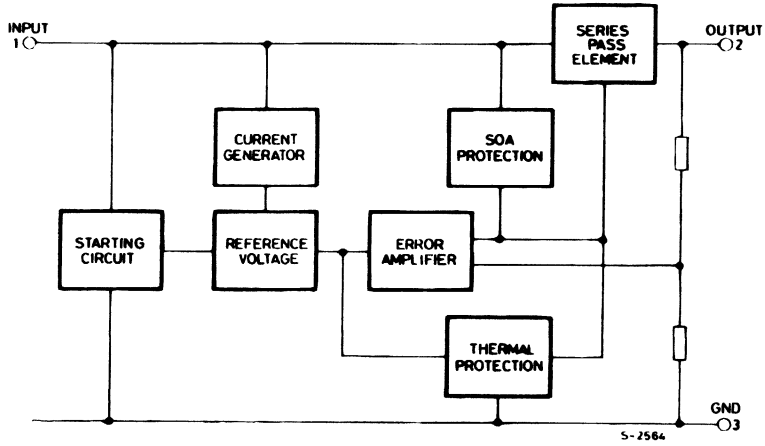


TO-220

DESCRIPTION

The L7800A series of three-terminal positive regulators is available in TO-220 and TO-3 packages and with several fixed output voltages, making it useful in a wide range of applications. These regulators can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

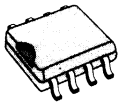
BLOCK DIAGRAM



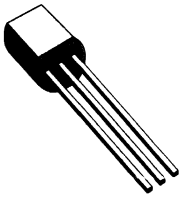
POSITIVE VOLTAGE REGULATORS

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST/1)

- OUTPUT CURRENT UP TO 100 mA
- OUTPUT VOLTAGES OF 5; 6; 8; 9; 12; 15; 18; 24V
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- NO EXTERNAL COMPONENTS ARE REQUIRED
- AVAILABLE IN EITHER ± 5% (AC) OR ± 10% (C) SELECTION



SO-8



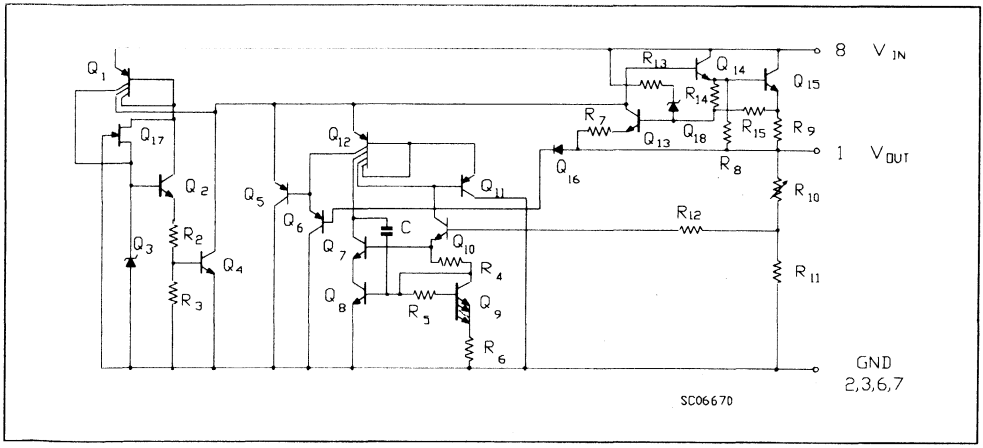
TO-92

DESCRIPTION

The L78L00 series of three-terminal positive regulators employ internal current limiting and thermal shutdown, making them essentially indestructible. If adequate heatsink is provided, they can deliver up to 100 mA output current. They are intended as fixed voltage regulators in a wide range of applications including local or on-card regulation for elimination of noise and distribution problems associated with single-point regulation. In addition, they can be used with power pass elements to make high-current voltage regulators.

The L78L00 series used as Zener diode/resistor combination replacement, offers an effective output impedance improvement of typically two orders of magnetude, along with lower quiescent current and lower noise.

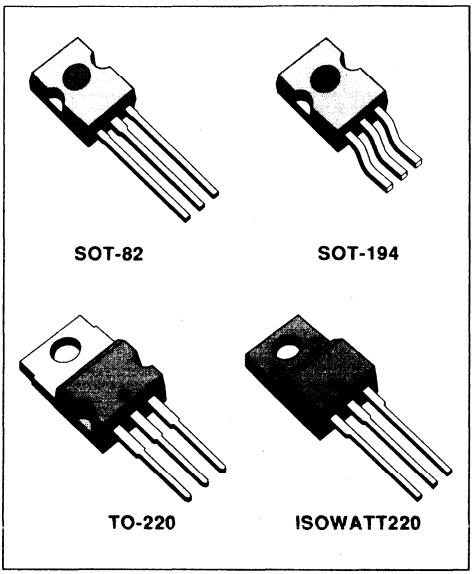
SCHEMATIC DIAGRAM



POSITIVE VOLTAGE REGULATORS

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST/1)

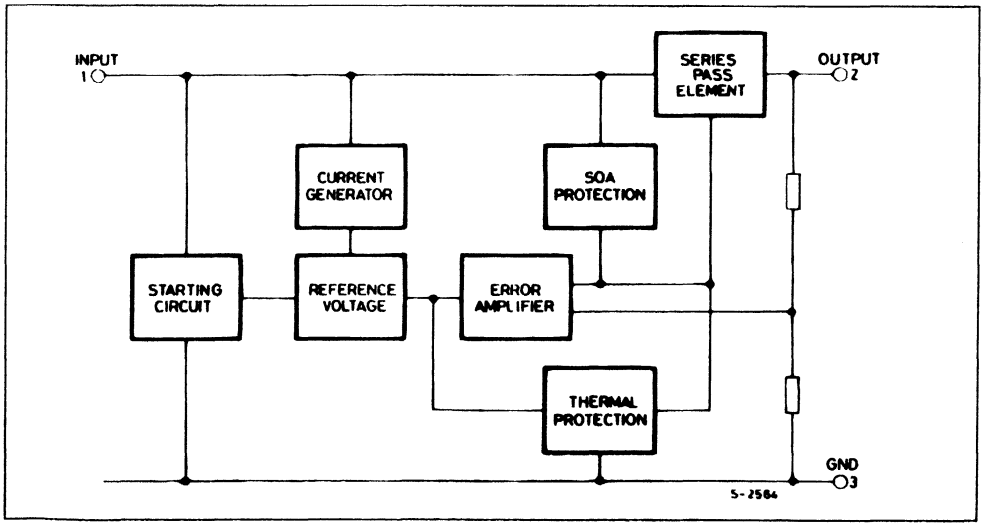
- OUTPUT CURRENT TO 0.5A
- OUTPUT VOLTAGES OF 5; 6; 8; 9: 10:12; 15; 18; 20; 24V
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTOR SOA PROTECTION



DESCRIPTION

The L78M00 series of three-terminal positive regulators is available in TO-220 ISOWATT220 and SOT-82 packages and with several fixed output voltages, making it useful in a wide range of applications. These regulators can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 0.5A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

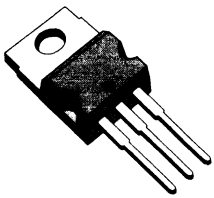
BLOCK DIAGRAM



PRECISION 500mA REGULATORS

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST/1)

- OUTPUT CURRENT UP TO 0.5A
- OUTPUT VOLTAGES OF 5; 6; 8; 9: 10: 12; 15; 18; 20; 24V
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTORS SOA PROTECTION
- ± 2% OUTPUT VOLTAGE TOLERANCE
- GUARANTEED IN EXTENDED TEMPERATURE RANGES

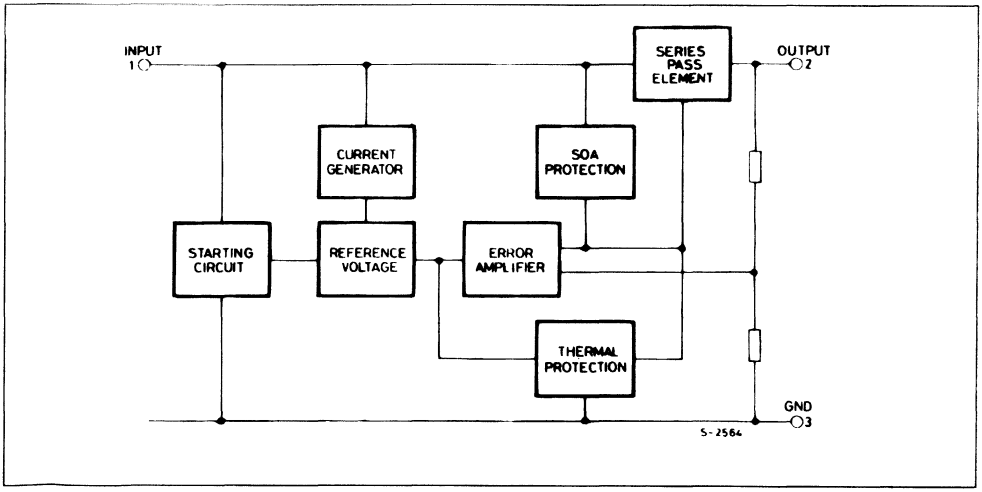


TO-220

DESCRIPTION

The L78M00AB series of three-therminal positive regulators is available in TO-220 package and with several fixed output voltages, making it useful in a wide range of applications. These regulators can provide local on-card regulation eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 0.5A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

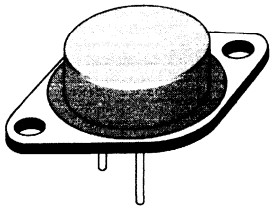
BLOCK DIAGRAM



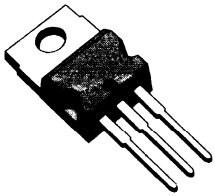
2A POSITIVE VOLTAGE REGULATORS

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST/1)

- OUTPUT CURRENT TO 2A
- OUTPUT VOLTAGES OF 5 ; 7.5 ; 9 ; 10 ; 12 ; 15 ; 18 ; 24V
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTOR SOA PROTECTION



TO-3

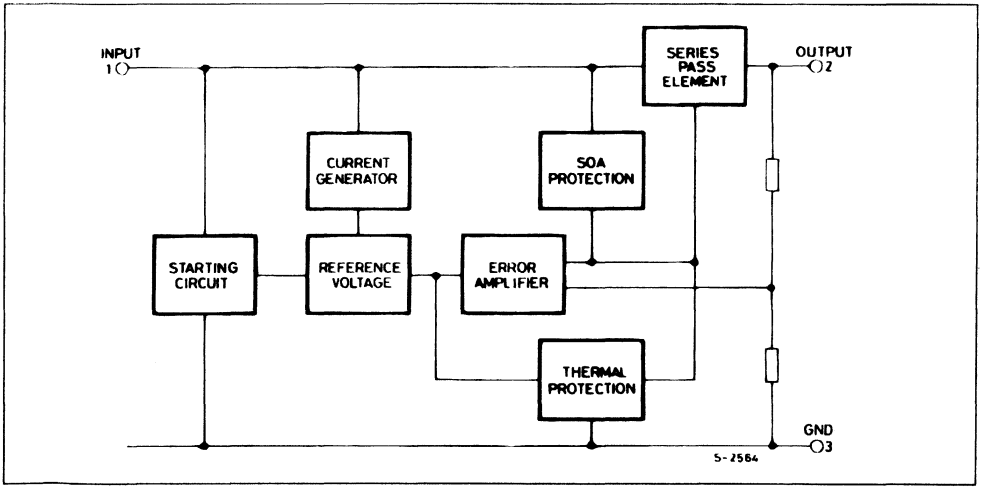


TO-220

DESCRIPTION

The L78S00 series of three-terminal positive regulators is available in TO-220 and TO-3 packages and with several fixed output voltages, making it useful in a wide range of applications. These regulators can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 2A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

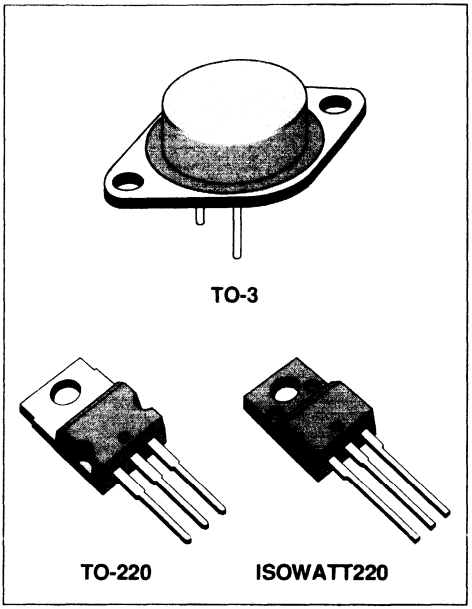
BLOCK DIAGRAM



NEGATIVE VOLTAGE REGULATORS

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST/1)

- OUTPUT CURRENT UP TO 1.5A
- OUTPUT VOLTAGES OF –5; –5.2; -6; –8; –12; –15; –18; – 20; – 22; – 24V
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTOR SOA PROTECTION

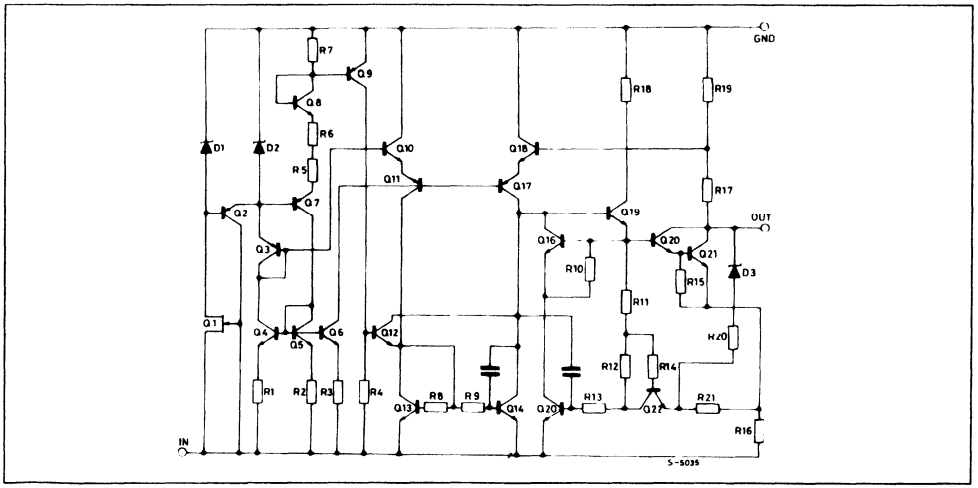


DESCRIPTION

The L7900 series of three-terminal negative regulators is available in TO-220 and TO-3 packages and with several output voltages. They can provide local on-card regulation, eliminating the distribution problems associated with single point regulation; furthermore, having the same voltage options as the L7800 positive standard series, they are particularly suited for split power supplies. In addition, the –5.2V is also available for ECL system.

If adeguate heatsinking is provided, the L7900 series can deliver an output current in excess of 1.5A. Although designed primarly as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

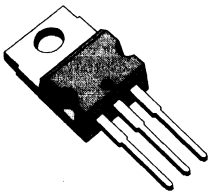
SCHEMATIC DIAGRAM



± 2% NEGATIVE VOLTAGE REGULATORS

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST/1)

- OUTPUT CURRENT UP TO 1.5A
- OUTPUT VOLTAGES OF – 5; – 5.2; -6; – 8; –12; –15; – 18; – 20; – 22; – 24V
- THERMAL CIRCUIT PROTECTION
- OUTPUT TRANSISTOR SOA PROTECTION



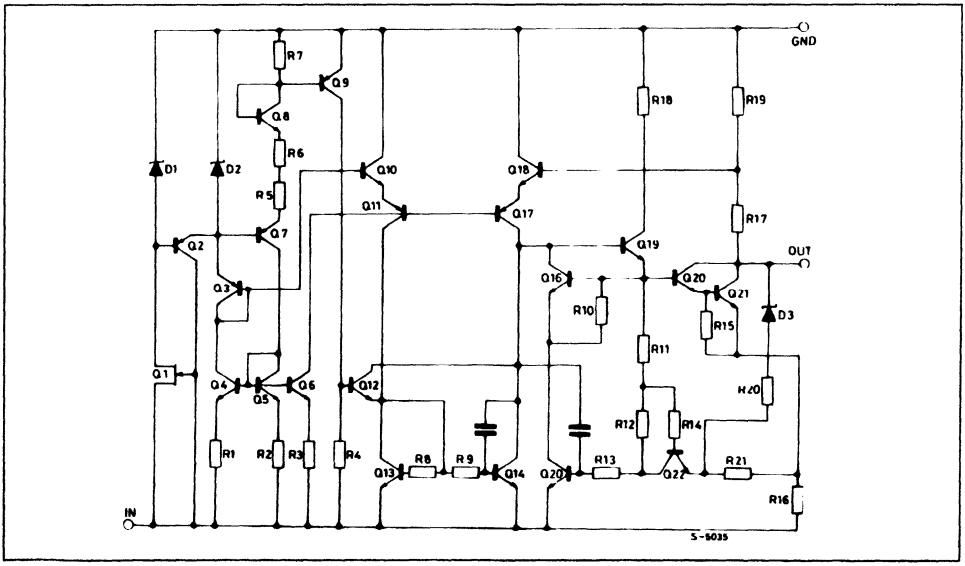
TO-220

DESCRIPTION

The L7900A series of three-terminal negative regulators is available in TO-220 package and with several output voltage. They can provide local on-card regulation, eliminating the distribution problems associated with single point regulation ; furthermore, having the same voltage options as the L7800 positive standard series, they are particularly suited for split power supplies. In addition, the -5.2V is also available for ECL system.

If adeguate heatsinking is provided, the L7900A series can deliver an output current in excess of 1.5A. Although designed primarly as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

SCHEMATIC DIAGRAM

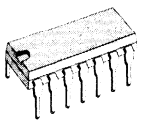


SGS-THOMSON MICROELECTRONICS

LF147 - LF247 LF347/B

WIDE BANDWIDTH QUAD J-FET OPERATIONAL AMPLIFIERS

- LOW POWER CONSUMPTION
- WIDE COMMON-MODE (UP TO V_{CC}^+) AND DIFFERENTIAL VOLTAGE RANGE
- LOW INPUT BIAS AND OFFSET CURRENT
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J-FET INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : 16V/µs (typ)



N
DIP14
(Plastic Package)

D
SO14
(Plastic Micropackage)

DESCRIPTION

These circuits are high speed J-FET input quad operational amplifiers incorporating well matched, high voltage J-FET and bipolar transistors in a monolithic integrated circuit.

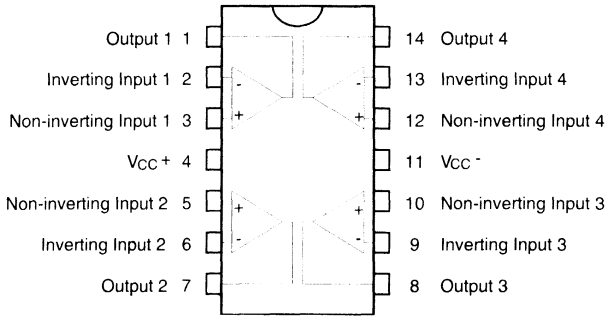
The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.

ORDER CODES

Part Number	Temperature	Package	
		N	D
LF347/B	0°C, +70°C	•	•
LF247	–40°C, +105°C	•	•
LF147	–55°C, +125°C	•	•

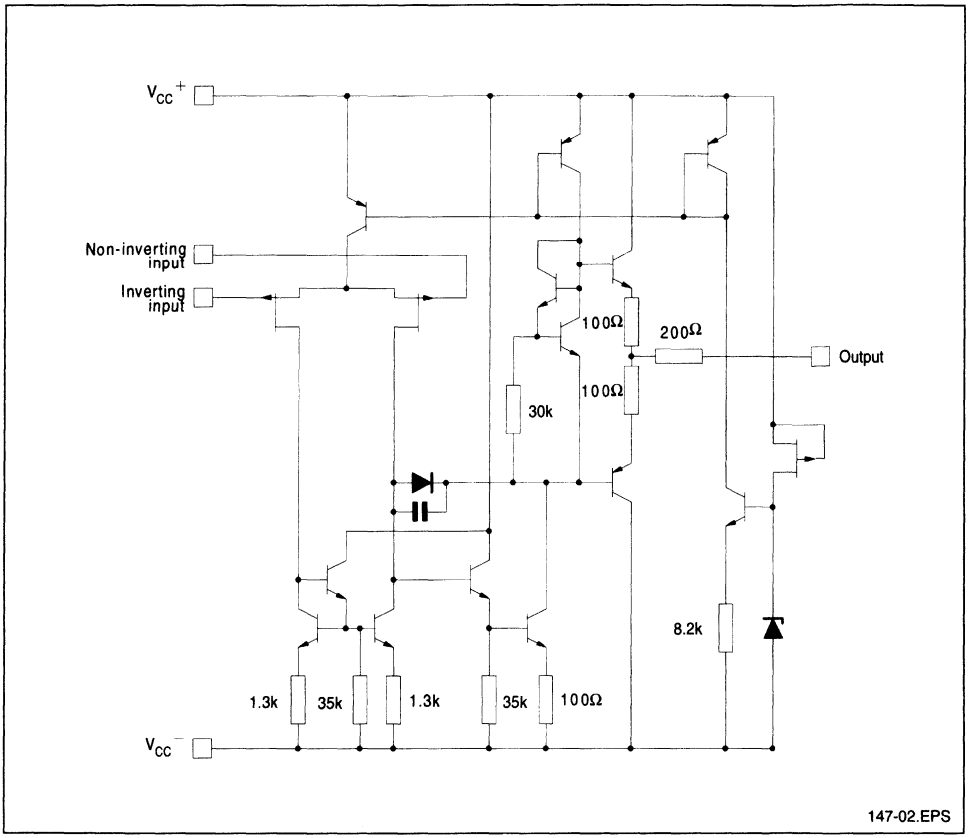
147-01.TBL

PIN CONNECTIONS (top view)



147-01.EPS

SCHEMATIC DIAGRAM (each amplifier)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage - (note 1)		±18	V
V_i	Input Voltage - (note 3)		±15	V
V_{id}	Differential Input Voltage - (note 2)		±30	V
P_{tot}	Power Dissipation		680	mW
	Output Short-circuit Duration - (note 4)		Infinite	
T_{oper}	Operating Free Air Temperature Range	LF347, B LF247 LF147	0 to 70 –40 to 105 –55 to 125	°C
T_{stg}	Storage Temperature Range		–65 to 150	°C

Notes :
1. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.
2. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and /or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

ELECTRICAL CHARACTERISTICS

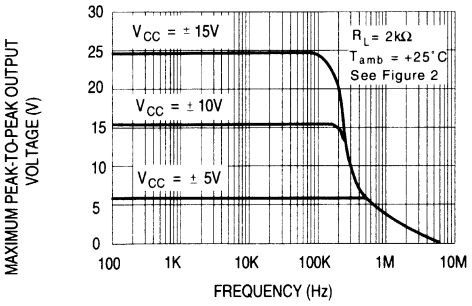
V_{CC} = ±15V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter		LF147 - LF247 LF347/B Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage (R_S = 10kΩ)					mV
	T_{amb} = 25°C			3	10	
		LF347B			5	
	$T_{min.} \le T_{amb} \le T_{max.}$				13	
		LF347B			7	
DV_{io}	Input Offset Voltage Drift			10		µV/°C
I_{io}	Input Offset Current *					
	T_{amb} = 25°C			5	100	pA
	$T_{min.} \le T_{amb} \le T_{max.}$				4	nA
I_{ib}	Input Bias Current *					
	T_{amb} = 25°C			20	200	pA
	$T_{min.} \le T_{amb} \le T_{max.}$				20	nA
A_{vd}	Large Signal Voltage Gain (R_L = 2kΩ, V_O = ±10V)					V/mV
	T_{amb} = 25°C		50	200		
	$T_{min.} \le T_{amb} \le T_{max}$		25			
SVR	Supply Voltage Rejection Ratio (R_S = 10kΩ)					dB
	T_{amb} = 25°C		80	86		
	$T_{min.} \le T_{amb} \le T_{max.}$		80			
I_{CC}	Supply Current, per Amp, no Load					mA
	T_{amb} = 25°C			1.4	2.7	
	$T_{min.} \le T_{amb} \le T_{max.}$				2.7	
V_{icm}	Input Common Mode Voltage Range		±11	+15 -12		V
CMR	Common Mode Rejection Ratio (R_S = 10kΩ)					dB
	T_{amb} = 25°C		70	86		
	$T_{min.} \le T_{amb} \le T_{max.}$		70			
Ios	Output Short-circuit Current					mA
	T_{amb} = 25°C		10	40	60	
	$T_{min.} \le T_{amb} \le T_{max.}$		10		60	
$\pm V_{OPP}$	Output Voltage Swing					V
	T_{amb} = 25°C	R_L = 2kΩ	10	12		
		R_L = 10kΩ	12	13.5		
	$T_{min.} \le T_{amb} \le T_{max.}$	R_L = 2kΩ	10			
		R_L = 10kΩ	12			
SR	Slew Rate (V_i = 10V, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)		12	16		V/µs
t_r	Rise Time (V_i = 20mV, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)			0.1		µs
K_{OV}	Overshoot (V_i = 20mV, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)			10		%
GBP	Gain Bandwidth Product (f = 100kHz, T_{amb} = 25°C, V_{in} = 10mV, R_L = 2kΩ, C_L = 100pF)		2.5	4		MHz
R_i	Input Resistance			10^{12}		Ω
THD	Total Harmonic Distortion (f = 1kHz, A_V = 20dB, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, V_O = $2V_{PP}$)			0.01		%
e_n	Equivalent Input Noise Voltage (f = 1kHz, R_s = 100Ω)			15		$\frac{nV}{\sqrt{Hz}}$
∅m	Phase Margin			45		Degrees
V_{O1}/V_{O2}	Channel Separation (A_v = 100, T_{amb} = 25°C)			120		dB

* The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature.

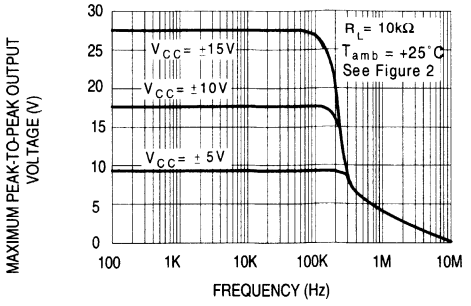
147-03.TBL

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



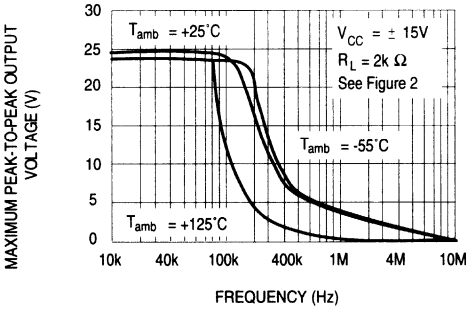
147-03.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



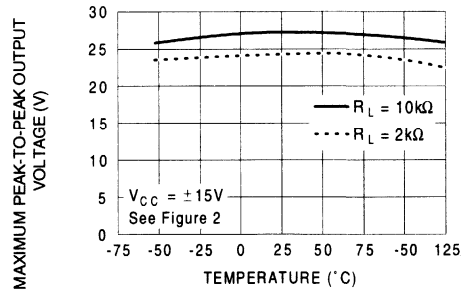
147-04.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



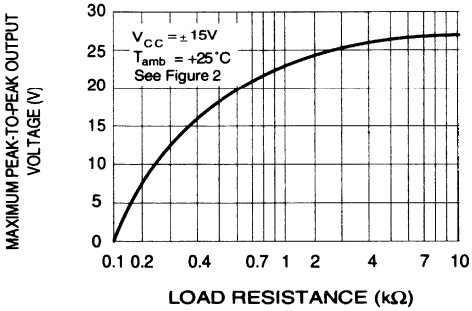
147-05.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREE AIR TEMP.



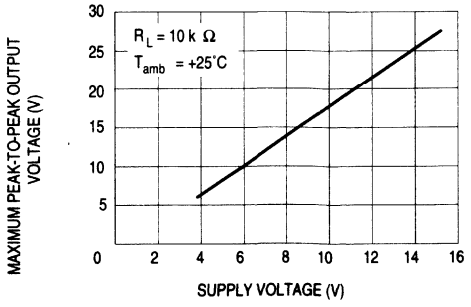
147-06.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS LOAD RESISTANCE



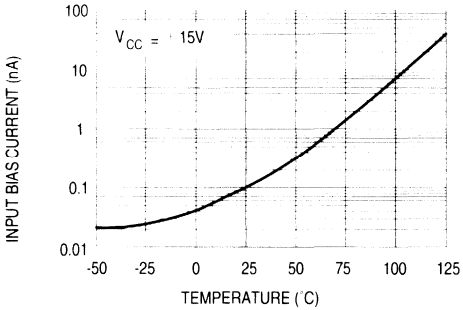
147-07.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS SUPPLY VOLTAGE



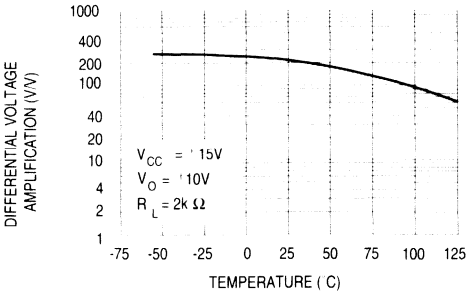
147-08.EPS

INPUT BIAS CURRENT VERSUS FREE AIR TEMPERATURE



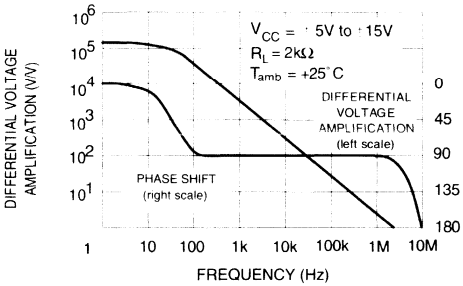
147-09.EPS

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION VERSUS FREE AIR TEMPERATURE



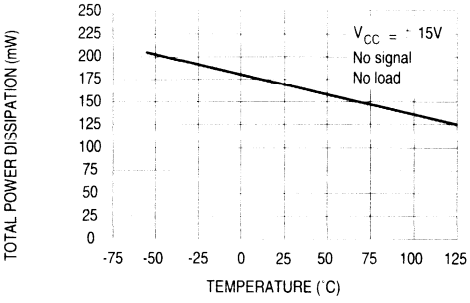
147-10.EPS

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT VERSUS FREQUENCY



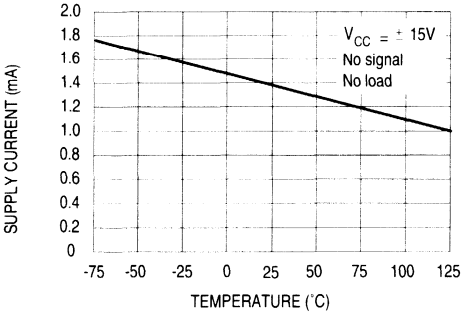
147-11.EPS

TOTAL POWER DISSIPATION VERSUS FREE AIR TEMPERATURE



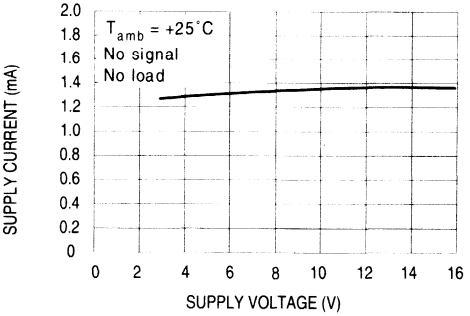
147-12.EPS

SUPPLY CURRENT PER AMPLIFIER VERSUS FREE AIR TEMPERATURE



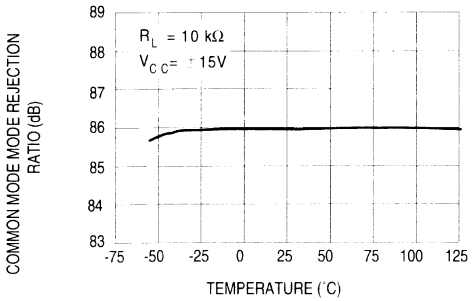
147-13.EPS

SUPPLY CURRENT PER AMPLIFIER VERSUS SUPPLY VOLTAGE



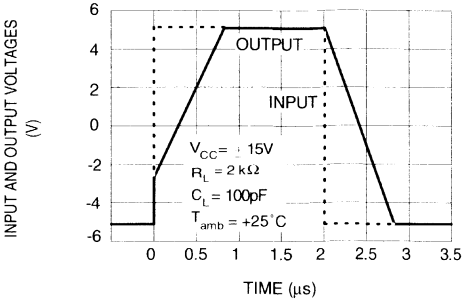
147-14.EPS

COMMON MODE REJECTION RATIO VERSUS FREE AIR TEMPERATURE



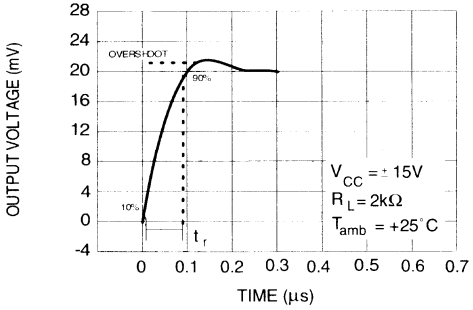
147-15.EPS

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



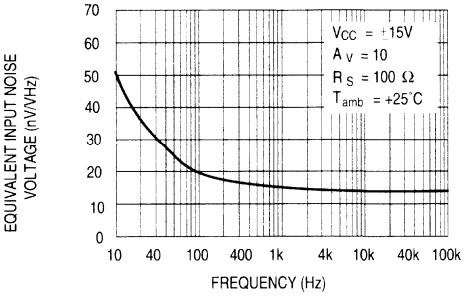
147-16.EPS

OUTPUT VOLTAGE VERSUS ELAPSED TIME



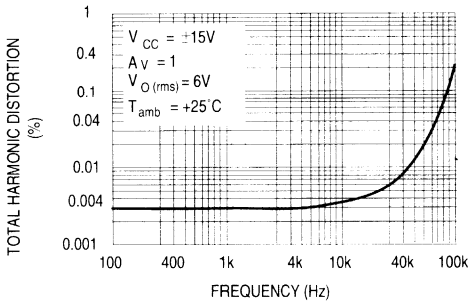
147-17.EPS

EQUIVALENT INPUT NOISE VOLTAGE VERSUS FREQUENCY



147-18.EPS

TOTAL HARMONIC DISTORTION VERSUS FREQUENCY



147-19.EPS

PARAMETER MEASUREMENT INFORMATION

Figure 1 : Voltage Follower

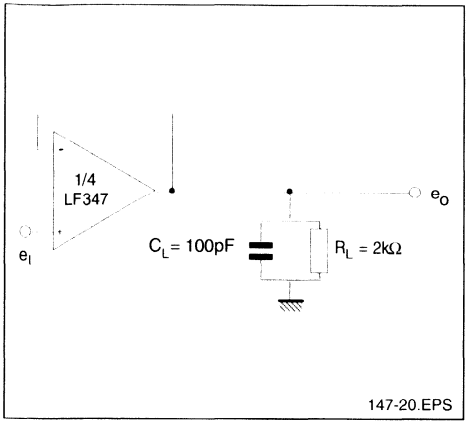
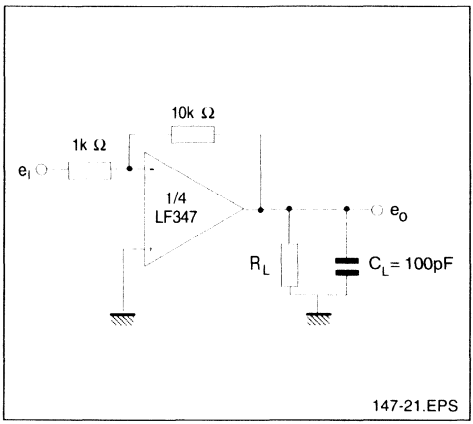
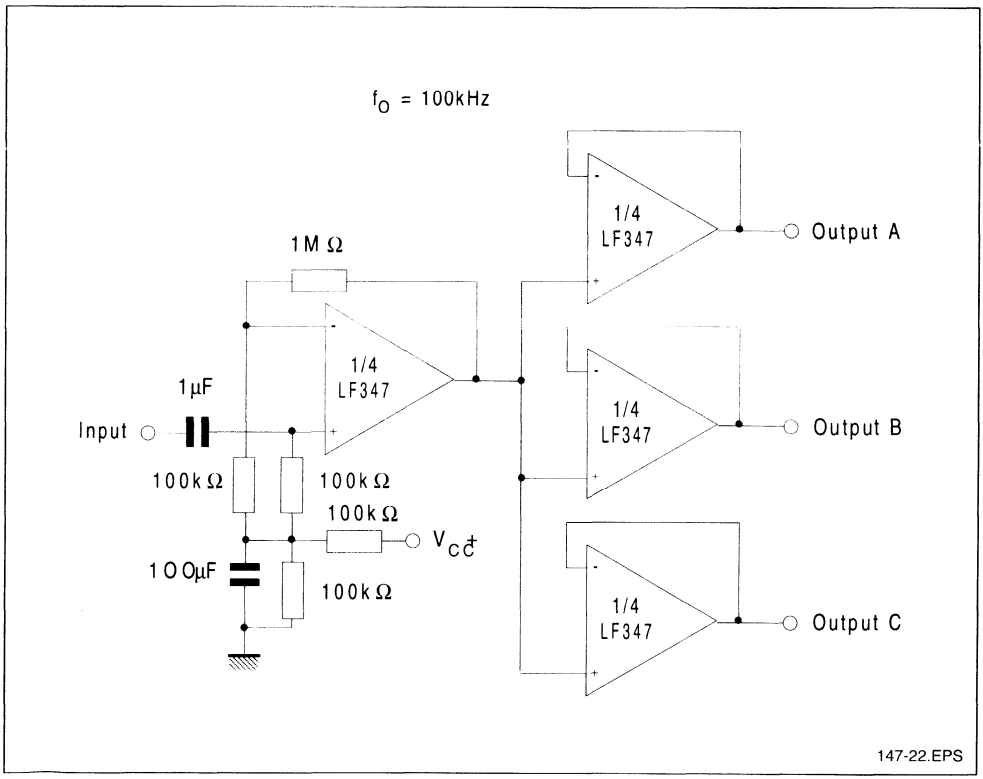


Figure 2 : Gain-of-10 Inverting Amplifier



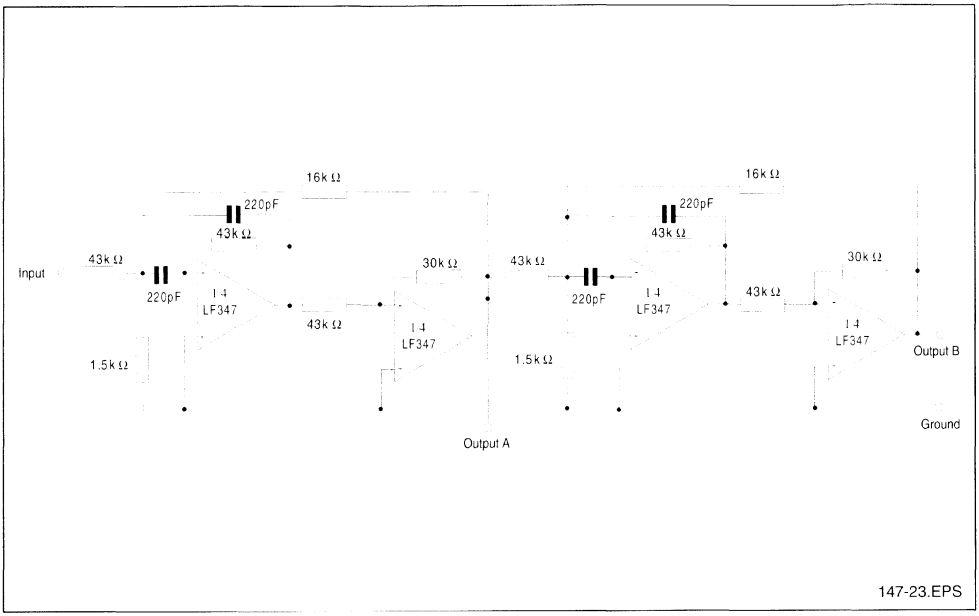
TYPICAL APPLICATIONS

AUDIO DISTRIBUTION AMPLIFIER

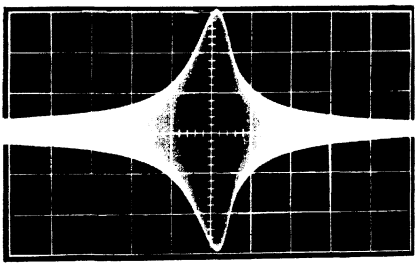


TYPICAL APPLICATIONS (continued)

POSITIVE FEEDBACK BANDPASS FILTER

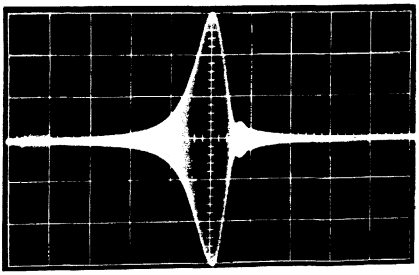


OUTPUT A



SECOND ORDER BANDPASS FILTER
fo = 100kHz ; Q = 30 ; Gain = 4

OUTPUT B



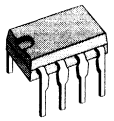
CASCADED BANDPASS FILTER
fo = 100kHz ; Q = 69 ; Gain = 16

SGS-THOMSON MICROELECTRONICS

LF151
LF251 - LF351

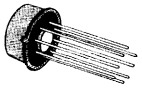
WIDE BANDWIDTH SINGLE J-FET OPERATIONAL AMPLIFIERS

- LOW POWER CONSUMPTION
- WIDE COMMON-MODE (UP TO V_{CC}^+) AND DIFFERENTIAL VOLTAGE RANGE
- LOW INPUT BIAS AND OFFSET CURRENT
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J-FET INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : 16V/µs (typ)



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)



H
TO99
(Metal Can)

DESCRIPTION

These circuits are high speed J-FET input single operational amplifiers incorporating well matched, high voltage J-FET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.

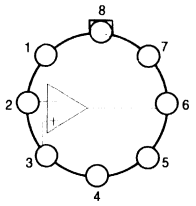
ORDER CODES

Part Number	Temperature	Package		
		H	N	D
LF351	0°C, +70°C	•	•	•
LF251	–40°C, +105°C	•	•	•
LF151	–55°C, +125°C	•	•	•

151-01.TBL

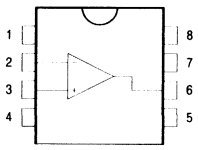
PIN CONNECTIONS (top views)

TO99



151-01.EPS

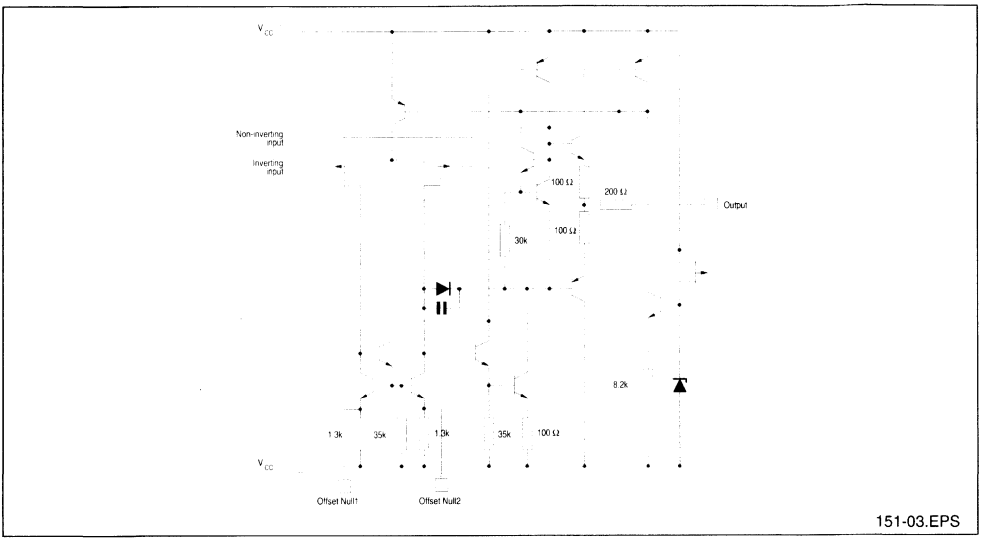
DIP8/SO8



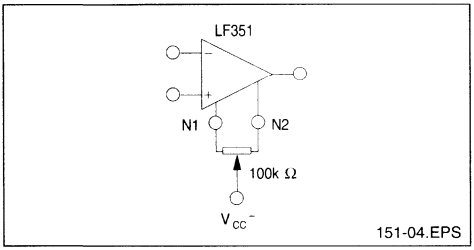
151-02.EPS

1 - Offset Null 1
2 - Inverting input
3 - Non-inverting input
4 - V_{CC}^-
5 - Offset Null 2
6 - Output
7 - V_{CC}^+
8 - N.C.

SCHEMATIC DIAGRAM



INPUT OFFSET VOLTAGE NULL CIRCUITS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage - (note 1)		±18	V
V_i	Input Voltage - (note 3)		±15	V
V_{id}	Differential Input Voltage - (note 2)		±30	V
P_{tot}	Power Dissipation		680	mW
	Output Short-circuit Duration - (note 4)		Infinite	
T_{oper}	Operating Free Air Temperature Range	LF351 LF251 LF151	0 to 70 –40 to 105 –55 to 125	°C
T_{stg}	Storage Temperature Range		–65 to 150	°C

151-02.TBL

Notes :
1. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.
2. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and /or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

ELECTRICAL CHARACTERISTICS

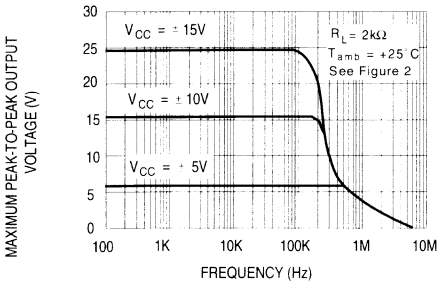
V_{CC} = ±15V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	LF151 - LF251 - LF351			Unit
		Min.	Typ.	Max.	
V_{io}	Input Offset Voltage (R_S = 10kΩ) T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$		3	10 13	mV
DV_{io}	Input Offset Voltage Drift		10		µV/°C
I_{io}	Input Offset Current * T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$		5	100 4	pA nA
I_{ib}	Input Bias Current * T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$		20	200 20	pA nA
A_{vd}	Large Signal Voltage Gain (R_L = 2kΩ, V_O = ±10V) T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$	50 25	200		V/mV
SVR	Supply Voltage Rejection Ratio (R_S = 10kΩ) T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$	80 80	86		dB
I_{CC}	Supply Current (no load) T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$		1.4	3.4 3.4	mA
V_{icm}	Input Common Mode Voltage Range	±11	+15 -12		V
CMR	Common Mode Rejection Ratio (R_S = 10kΩ) T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$	70 70	86		dB
Ios	Output Short-circuit Current T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$	10 10	40	60 60	mA
$\pm V_{OPP}$	Output Voltage Swing T_{amb} = 25°C R_L = 2kΩ R_L = 10kΩ $T_{min.} \le T_{amb} \le T_{max.}$ R_L = 2kΩ R_L = 10kΩ	10 12 10 12	12 13.5		V
SR	Slew Rate (V_i = 10V, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)	12	16		V/µs
t_r	Rise Time (V_i = 20mV, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)		0.1		µs
K_{OV}	Overshoot (V_i = 20mV, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)		10		%
GBP	Gain Bandwidth Product (f = 100kHz, T_{amb} = 25°C, V_{in} = 10mV, R_L = 2kΩ, C_L = 100pF)	2.5	4		MHz
R_i	Input Resistance		10^{12}		Ω
THD	Total Harmonic Distortion (f = 1kHz, A_V = 20dB, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, V_O = 2V_{PP})		0.01		%
e_n	Equivalent Input Noise Voltage (f = 1kHz, R_s = 100Ω)		15		$\frac{nV}{\sqrt{Hz}}$
Øm	Phase Margin		45		Degrees

151-03.TBL

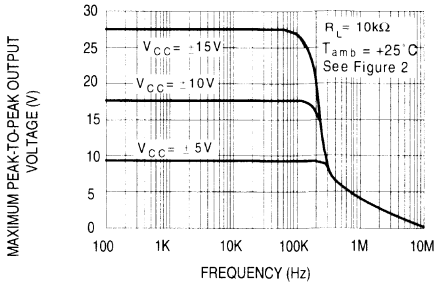
* The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature.

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



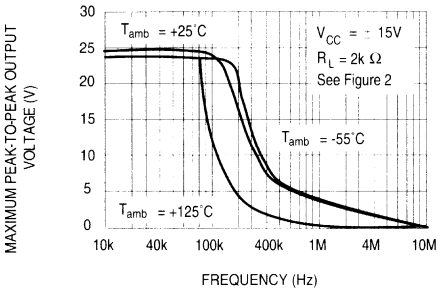
151-05.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



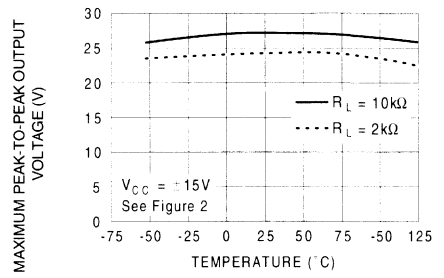
151-06.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



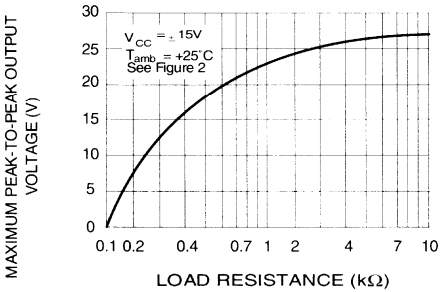
151-07.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREE AIR TEMP.



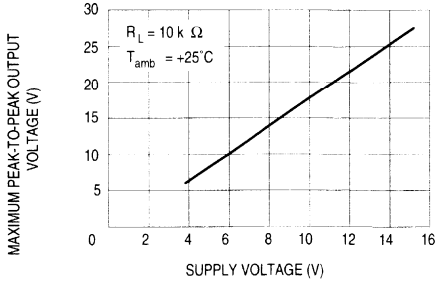
151-08.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS LOAD RESISTANCE



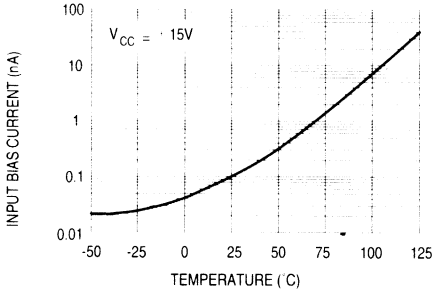
151-09.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS SUPPLY VOLTAGE



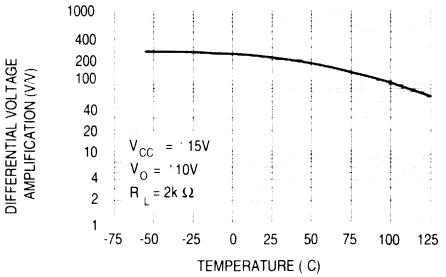
151-10.EPS

INPUT BIAS CURRENT VERSUS FREE AIR TEMPERATURE



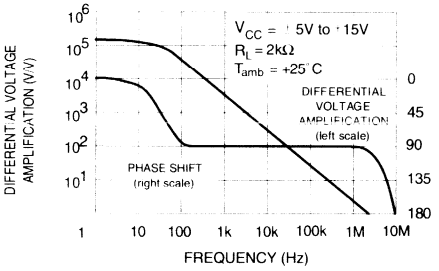
151-11.EPS

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION VERSUS FREE AIR TEMPERATURE



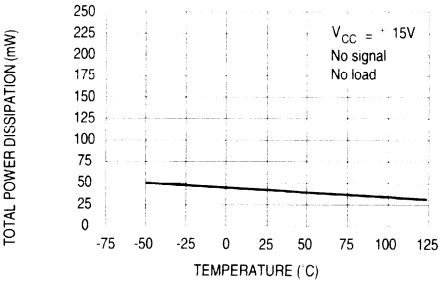
151-12.EPS

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT VERSUS FREQUENCY



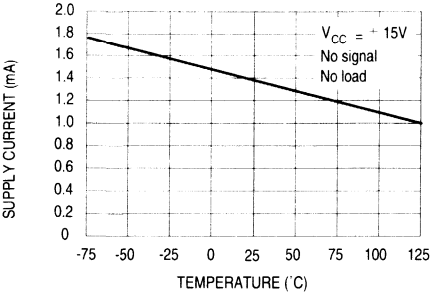
151-13.EPS

TOTAL POWER DISSIPATION VERSUS FREE AIR TEMPERATURE



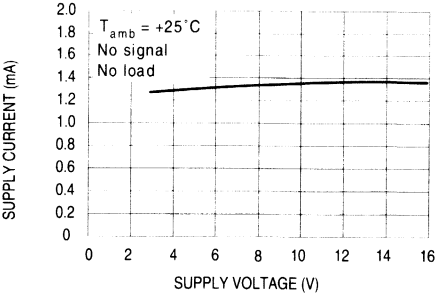
151-14.EPS

SUPPLY CURRENT PER AMPLIFIER VERSUS FREE AIR TEMPERATURE



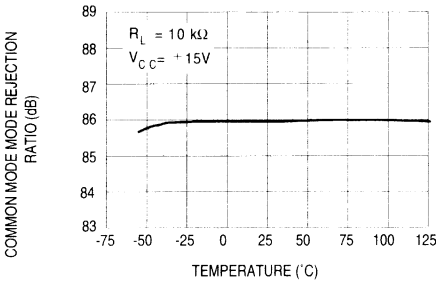
151-15.EPS

SUPPLY CURRENT PER AMPLIFIER VERSUS SUPPLY VOLTAGE



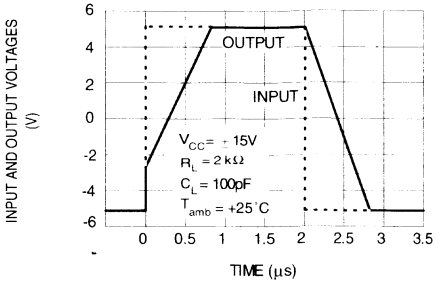
151-16.EPS

COMMON MODE REJECTION RATIO VERSUS FREE AIR TEMPERATURE



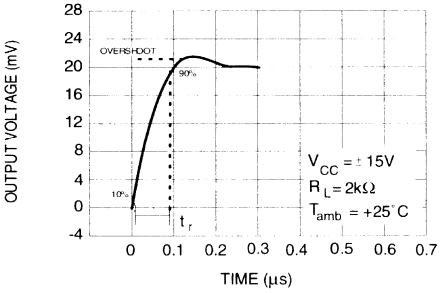
151-17.EPS

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



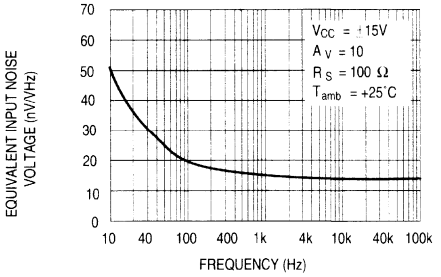
151-18.EPS

OUTPUT VOLTAGE VERSUS ELAPSED TIME



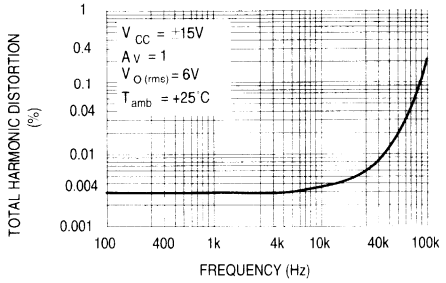
151-19.EPS

EQUIVALENT INPUT NOISE VOLTAGE VERSUS FREQUENCY



151-20.EPS

TOTAL HARMONIC DISTORTION VERSUS FREQUENCY



151-21.EPS

PARAMETER MEASUREMENT INFORMATION

Figure 1 : Voltage Follower

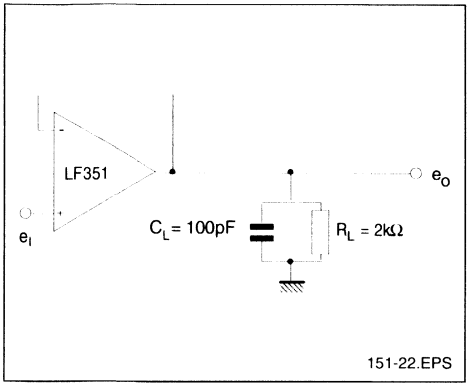
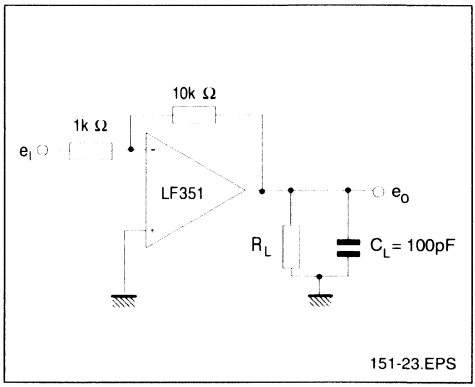
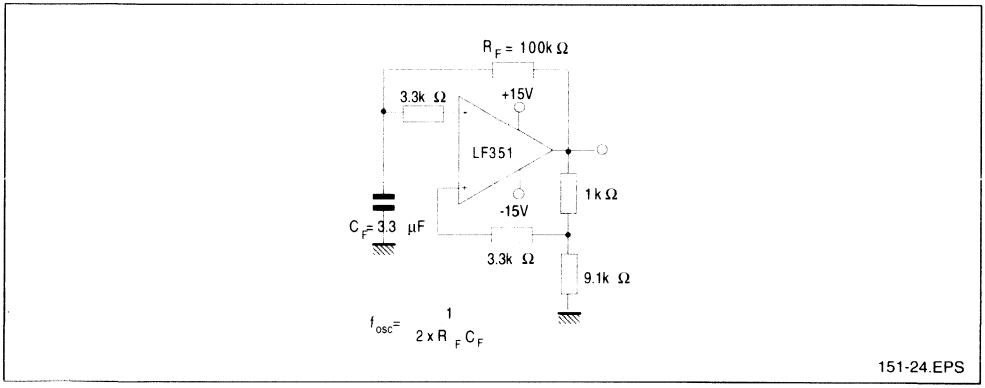


Figure 2 : Gain-of-10 Inverting Amplifier

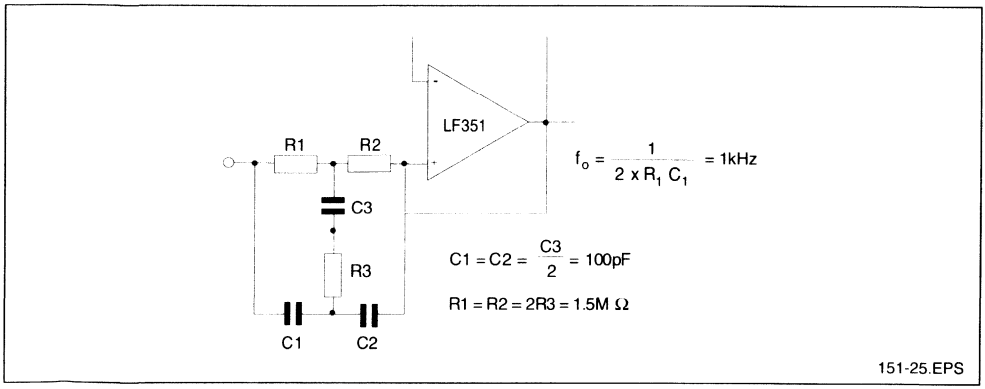


TYPICAL APPLICATIONS

(0.5Hz) SQUARE WAVE OSCILLATOR



HIGH Q NOTCH FILTER

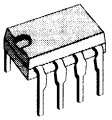


SGS-THOMSON MICROELECTRONICS

LF153
LF253 - LF353

WIDE BANDWIDTH DUAL J-FET OPERATIONAL AMPLIFIERS

- LOW POWER CONSUMPTION
- WIDE COMMON-MODE (UP TO V_{CC}^+) AND DIFFERENTIAL VOLTAGE RANGE
- LOW INPUT BIAS AND OFFSET CURRENT
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J-FET INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : 16V/µs (typ)



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

H
TO99
(Metal Can)

DESCRIPTION

The LF353 are high speed J-FET input dual operational amplifiers incorporating well matched, high voltage J-FET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.

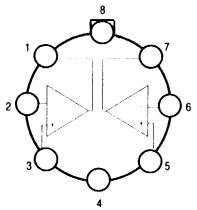
ORDER CODES

Part Number	Temperature	Package		
		H	N	D
LF353	0°C, +70°C	•	•	•
LF253	–40°C, +105°C	•	•	•
LF153	–55°C, +125°C	•	•	•

153-01.TBL

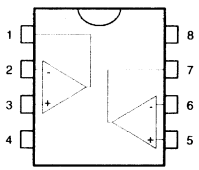
PIN CONNECTIONS (top views)

TO99



153-01.EPS

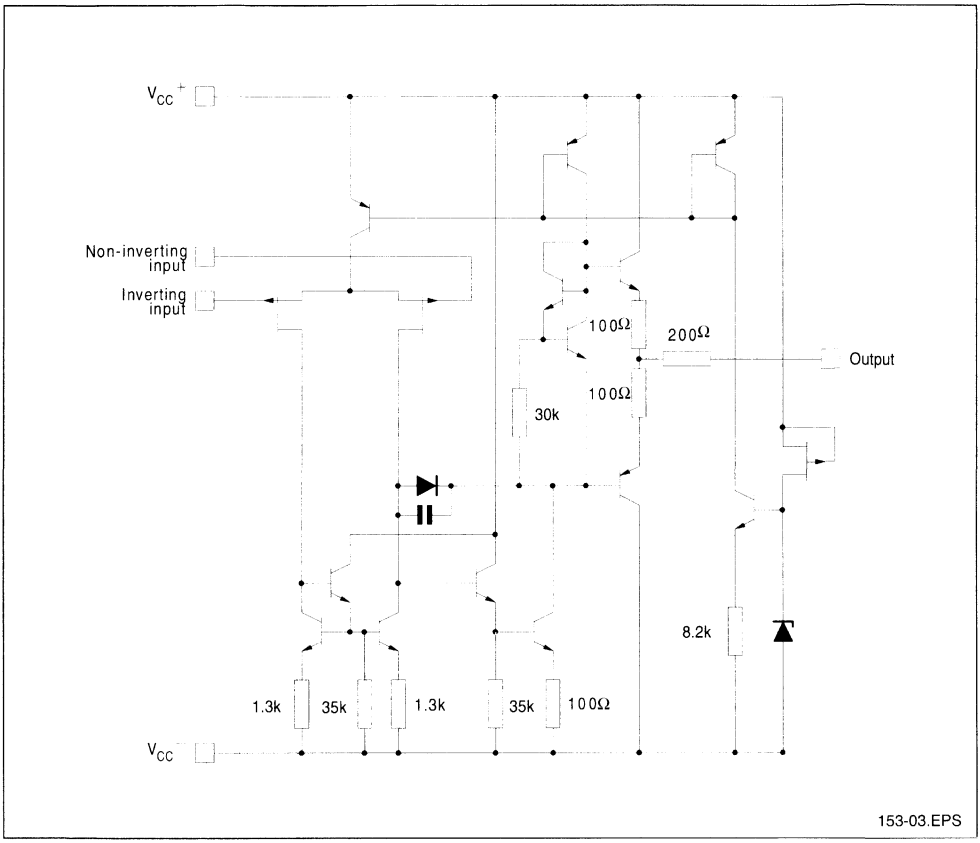
DIP8/SO8



153-02.EPS

1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^-
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - V_{CC}^+

SCHEMATIC DIAGRAM (each amplifier)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage - (note 1)		±18	V
V_i	Input Voltage - (note 3)		±15	V
V_{id}	Differential Input Voltage - (note 2)		±30	V
P_{tot}	Power Dissipation		680	mW
	Output Short-circuit Duration - (note 4)		Infinite	
T_{oper}	Operating Free Air Temperature Range	LF353 LF253 LF153	0 to 70 –40 to 105 –55 to 125	°C
T_{stg}	Storage Temperature Range		–65 to 150	°C

Notes :
1. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.
2. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and /or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

ELECTRICAL CHARACTERISTICS

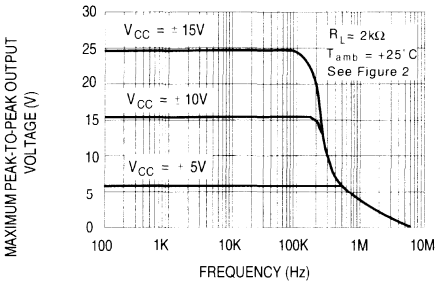
V_{CC} = ±15V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	LF153 - LF253 - LF353			Unit
		Min.	Typ.	Max.	
V_{io}	Input Offset Voltage (R_S = 10kΩ) T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$		3	10 13	mV
DV_{io}	Input Offset Voltage Drift		10		µV/°C
I_{io}	Input Offset Current * T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$		5	100 4	pA nA
I_{ib}	Input Bias Current * T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$		20	200 20	pA nA
A_{vd}	Large Signal Voltage Gain (R_L = 2kΩ, V_O = ±10V) T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$	50 25	200		V/mV
SVR	Supply Voltage Rejection Ratio (R_S = 10kΩ) T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$	80 80	86		dB
I_{CC}	Supply Current, per Amp, no Load T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$		1.4	3.2 3.2	mA
V_{icm}	Input Common Mode Voltage Range	±11	+15 -12		V
CMR	Common Mode Rejection Ratio (R_S = 10kΩ) T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$	70 70	86		dB
Ios	Output Short-circuit Current T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$	10 10	40	60 60	mA
$\pm V_{OPP}$	Output Voltage Swing T_{amb} = 25°C R_L = 2kΩ R_L = 10kΩ $T_{min.} \le T_{amb} \le T_{max.}$ R_L = 2kΩ R_L = 10kΩ	10 12 10 12	12 13.5		V
SR	Slew Rate (V_i = 10V, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)	12	16		V/µs
t_r	Rise Time (V_i = 20mV, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)		0.1		µs
K_{OV}	Overshoot (V_i = 20mV, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)		10		%
GBP	Gain Bandwidth Product (f = 100kHz, T_{amb} = 25°C, V_{in} = 10mV, R_L = 2kΩ, C_L = 100pF)	2.5	4		MHz
R_i	Input Resistance		10^{12}		Ω
THD	Total Harmonic Distortion (f = 1kHz, A_V = 20dB, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, V_O = $2V_{PP}$)		0.01		%
e_n	Equivalent Input Noise Voltage (f = 1kHz, R_s = 100Ω)		15		$\frac{nV}{\sqrt{Hz}}$
Øm	Phase Margin		45		Degrees
V_{O1}/V_{O2}	Channel Separation (A_v = 100, T_{amb} = 25°C)		120		dB

153-03.TBL

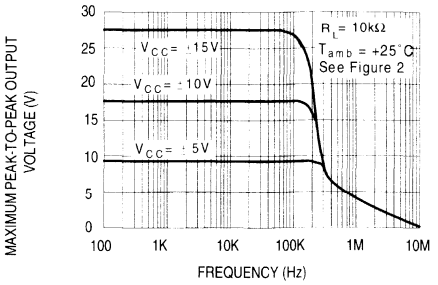
* The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature.

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



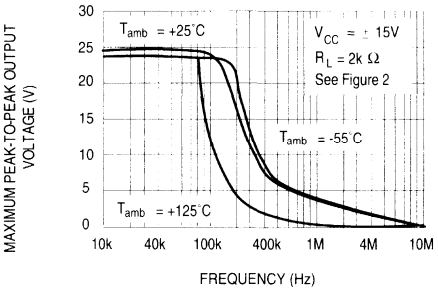
153-04.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



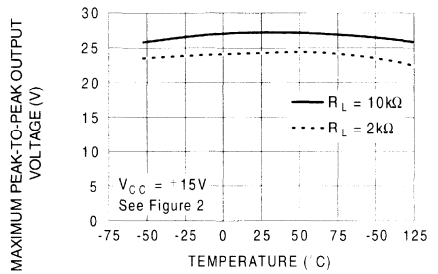
153-05.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



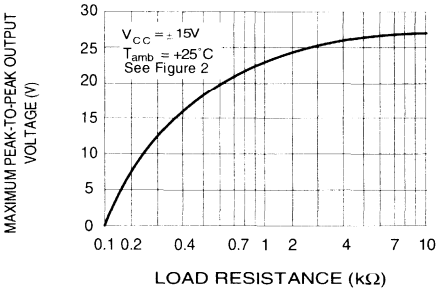
153-06.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREE AIR TEMP.



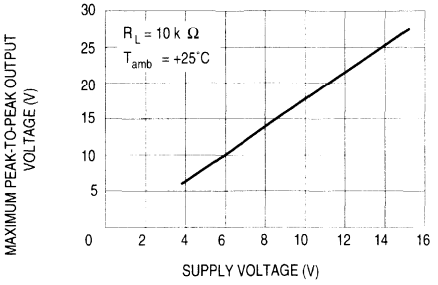
153-07.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS LOAD RESISTANCE



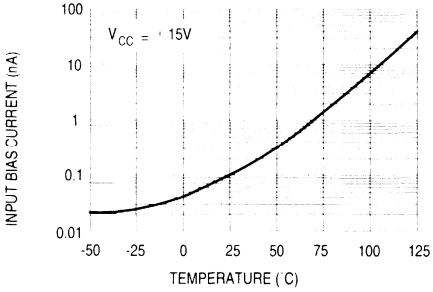
153-08.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS SUPPLY VOLTAGE



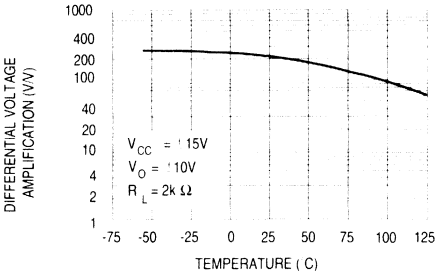
153-09.EPS

INPUT BIAS CURRENT VERSUS FREE AIR TEMPERATURE



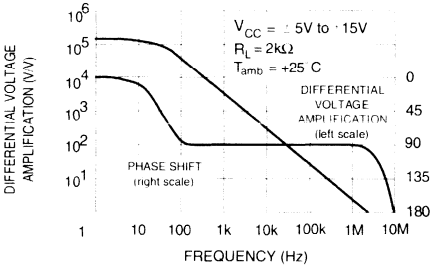
153-10.EPS

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION VERSUS FREE AIR TEMPERATURE



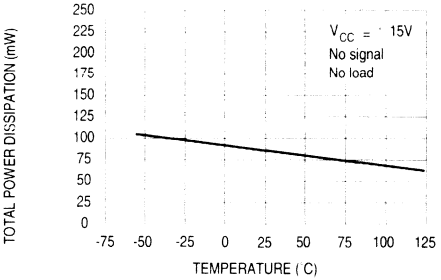
153-11.EPS

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT VERSUS FREQUENCY



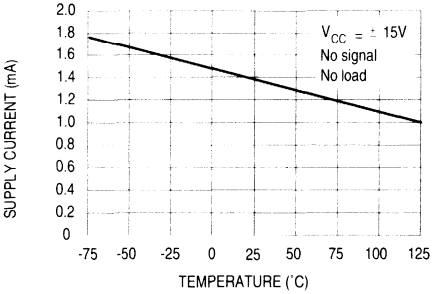
153-12.EPS

TOTAL POWER DISSIPATION VERSUS FREE AIR TEMPERATURE



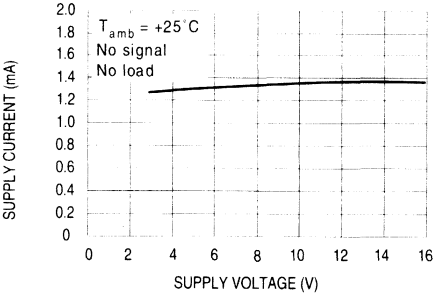
153-13.EPS

SUPPLY CURRENT PER AMPLIFIER VERSUS FREE AIR TEMPERATURE



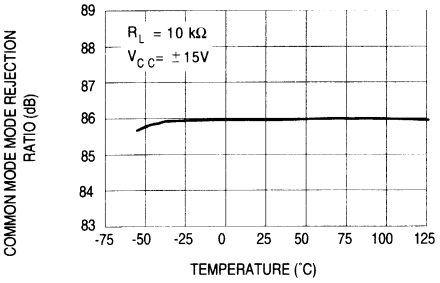
153-14.EPS

SUPPLY CURRENT PER AMPLIFIER VERSUS SUPPLY VOLTAGE



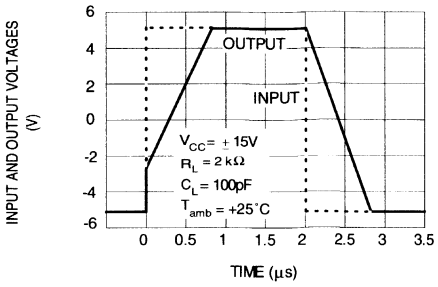
153-15.EPS

COMMON MODE REJECTION RATIO VERSUS FREE AIR TEMPERATURE



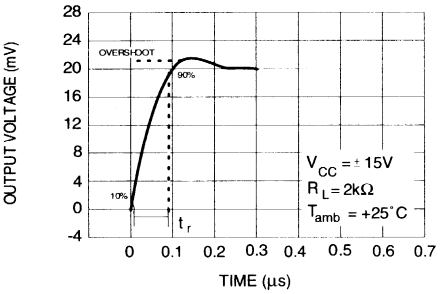
153-16.EPS

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



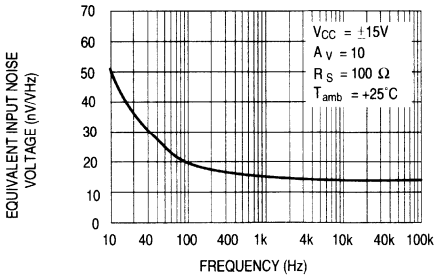
153-17.EPS

OUTPUT VOLTAGE VERSUS ELAPSED TIME



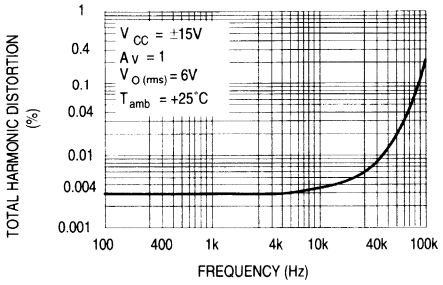
153-18.EPS

EQUIVALENT INPUT NOISE VOLTAGE VERSUS FREQUENCY



153-19.EPS

TOTAL HARMONIC DISTORTION VERSUS FREQUENCY



153-20.EPS

PARAMETER MEASUREMENT INFORMATION

Figure 1 : Voltage Follower

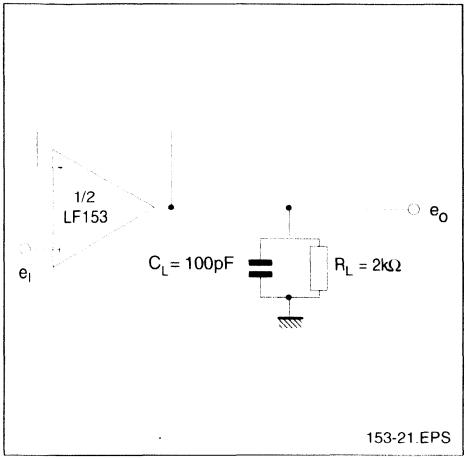
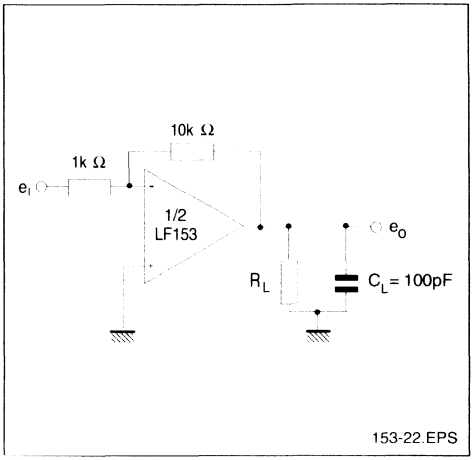
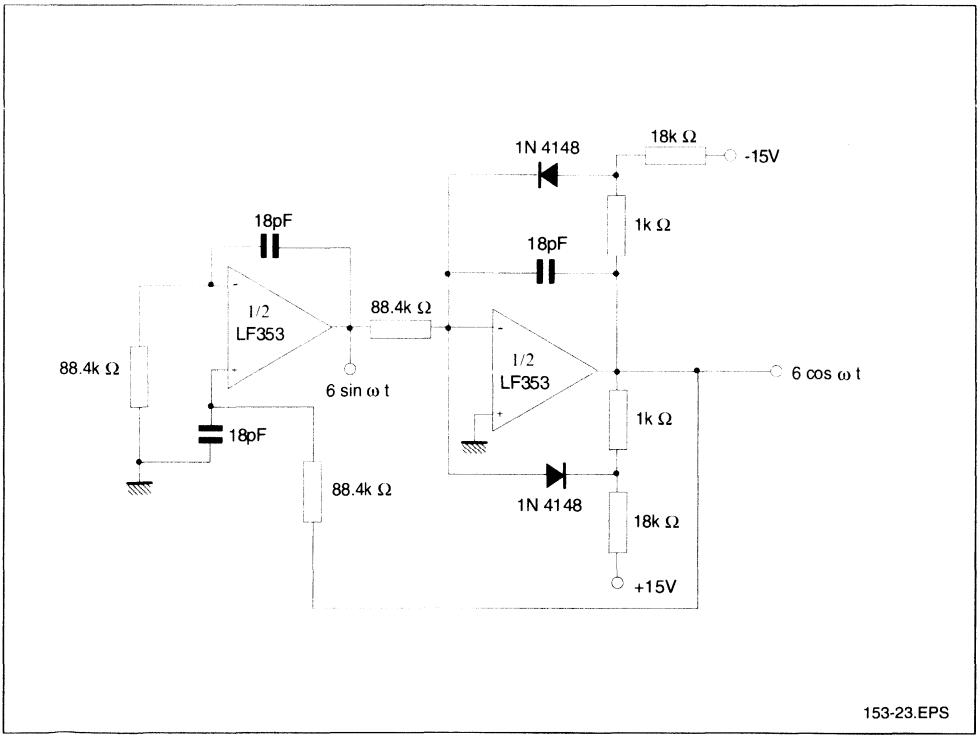


Figure 2 : Gain-of-10 Inverting Amplifier



TYPICAL APPLICATION

QUADRUPLE OSCILLATOR

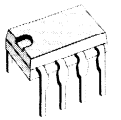


SGS-THOMSON MICROELECTRONICS

LF155 - LF255 - LF355
LF156 - LF256 - LF356
LF157 - LF257 - LF357

WIDE BANDWIDTH SINGLE J-FET OPERATIONAL AMPLIFIERS

- REPLACE HYBRID AND MODULE FET OP AMPs
- RUGGED J-FETs ALLOW BLOW-OUT FREE-HANDLING COMPARED WITH MOSFET INPUT DEVICES
- EXCELLENT FOR LOW NOISE APPLICATIONS USING EITHER HIGH OR LOW SOURCE IMPEDANCE (VERY LOW I/F CORNER)
- OFFSET VOLTAGE ADJUST DOES NOT DEGRADE DRIFT OR COMMON-MODE REJECTION AS IN MOST MONOLITHIC AMPLIFIERS
- INTERNAL COMPENSATION AND LARGE DIFFERENTIAL INPUT VOLTAGE CAPABILITY (UP TO V_{CC}^+)



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

H
TO99
(Metal Can)

TYPICAL APPLICATIONS

- PRECISION HIGH SPEED INTEGRATORS
- FAST D/A AND A/D CONVERTERS
- HIGH IMPEDANCE BUFFERS
- WIDEBAND, LOW NOISE, LOW DRIFT AMPLIFIERS
- LOGARITHMIC AMPLIFIERS
- PHOTOCELL AMPLIFIERS
- SAMPLE AND HOLD CIRCUITS

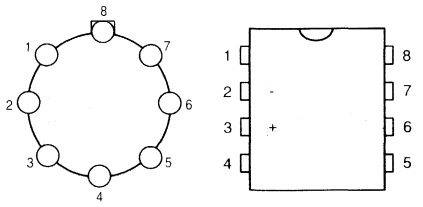
ORDER CODES

Part Number	Temperature Range	Package		
		H	N	D
LF355, LF356, LF357	0°C, +70°C	•	•	•
LF255, LF256, LF257	-40°C, +105°C	•	•	•
LF155, LF156, LF157	-55°C, +125°C	•	•	•

Examples : LF355N, LF155H

155-01.TBL

PIN CONNECTIONS (top views)



1 - Offset null 1
2 - Inverting input
3 - Non-inverting input
4 - V_{CC}^-
5 - Offset null 2
6 - Output
7 - V_{CC}^+
8 - N.C.

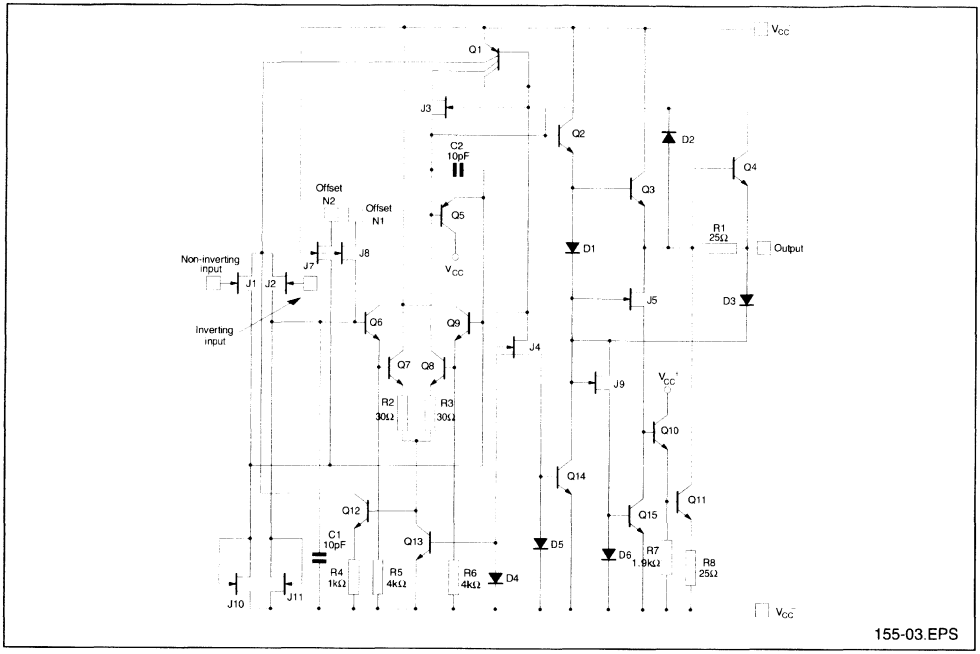
DESCRIPTION

These circuits are monolithic J-FET input operational amplifiers incorporating well matched, high voltage J-FET on the same chip with standard bipolar transistors.

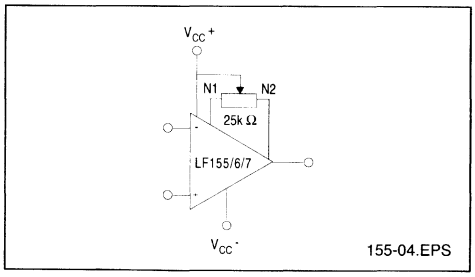
This amplifiers feature low input bias and offset currents, low input offset voltage and input offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection.

The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low I/f noise corner.

SCHEMATIC DIAGRAM



V_{io} ADJUSTMENT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		±22	V
V_i	Input Voltage - (note 1)		±20	V
V_{id}	Differential Input Voltage		±40	V
P_{tot}	Power Dissipation		570	mW
	Output Short-circuit Duration		Infinite	
T_{oper}	Operating Free Air Temperature Range	LF155-LF156-LF157 LF255-LF256-LF257 LF355-LF356-LF357	–55 to +125 –40 to +105 0 to +70	°C
T_{stg}	Storage Temperature Range		–65 to 150	°C

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ELECTRICAL CHARACTERISTICS

LF155, LF156, LF157 $-55^{o}C \leq T_{amb} \leq +125^{o}C$ $\pm 15V \leq V_{CC} \leq \pm 20V$

LF255, LF256, LF257 $-40^{o}C \leq T_{amb} \leq +105^{o}C$ $\pm 15V \leq V_{CC} \leq \pm 20V$

(unless otherwise specified)

Symbol	Parameter		LF155 - LF156 - LF157 LF255 - LF256 - LF257 Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage ($R_S = 50\Omega$)					mV
	$T_{amb} = +25^{o}C$			3	5	
	$T_{min.} \leq T_{amb} \leq T_{max.}$	LF155, LF156, LF157			7	
		LF255, LF256, LF257			6.5	
I_{io}	Input Offset Current - (note 3)					
	$T_{amb} = +25^{o}C$			3	20	pA
	$T_{min.} \leq T_{amb} \leq T_{max.}$	LF155, LF156, LF157			20	nA
		LF255, LF256, LF257			1	nA
I_{ib}	Input Bias Current - (note 3)					
	$T_{amb} = 25^{o}C$			20	100	pA
	$T_{min.} \leq T_{amb} \leq T_{max.}$	LF155, LF156, LF157			50	nA
		LF255, LF256, LF257			5	nA
A_{vd}	Large Signal Voltage Gain ($R_L = 2k\Omega$, $V_o = \pm 10V$, $V_{CC} = \pm 15V$)					V/mV
	$T_{amb} = +25^{o}C$		50	200		
	$T_{min.} \leq T_{amb} \leq T_{max.}$		25			
SVR	Supply Voltage Rejection Ratio - (note 4)		85	100		dB
I_{CC}	Supply Current, ($V_{CC} = \pm 15V$, no load)					mA
	$T_{amb} = +25^{o}C$	LF155, LF255		2	4	
		LF156, LF256		5	7	
		LF157, LF257		5	7	
DV_{io}	Input Offset Voltage Drift ($R_S = 50\Omega$)			5		$\mu V/^{o}C$
DV_{io}/V_{io}	Change in Average Temperature Coefficient with V_{IO} adjust ($R_S = 50\Omega$) - (note 2)			0.5		$\mu V/^{o}C$ per mV
V_{icm}	Input Common Mode Voltage Range ($V_{CC} = \pm 15V$, $T_{amb} = 25^{o}C$)		± 11	+15.1 -12		V
CMR	Common Mode Rejection Ratio		85	100		dB
$\pm V_{OPP}$	Output Voltage Swing ($V_{CC} = \pm 15V$)					V
	$R_L = 10k\Omega$		± 12	± 13		
	$R_L = 2k\Omega$		± 10	± 12		
GBP	Gain Bandwidth Product ($V_{CC} = \pm 15V$, $T_{amb} = 25^{o}C$)					MHz
		LF155, LF255		2.5		
		LF156, LF256		5		
		LF157, LF257		20		
SR	Slew Rate ($V_{CC} = \pm 15V$, $T_{amb} = 25^{o}C$)					V/µs
	$A_V = 1$	LF155, LF255		5		
		LF156, LF256	7.5	12		
	$A_V = 5$	LF157, LF257	30	50		
R_i	Input Resistance ($T_{amb} = +25^{o}C$)			10^{12}		Ω
C_i	Input Capacitance ($V_{CC} = \pm 15V$, $T_{amb} = 25^{o}C$)			3		pF
e_n	Equivalent Input Noise Voltage ($V_{CC} = \pm 15V$, $T_{amb} = 25^{o}C$, $R_S = 100\Omega$)					$\frac{nV}{\sqrt{Hz}}$
	f = 1000Hz	LF155, LF255		20		
		LF156, LF256		12		
		LF157, LF257		12		
	f = 100Hz	LF155, LF255		25		
		LF156, LF256		15		
		LF157, LF257		15		
i_n	Equivalent Input Noise Current ($V_{CC} = \pm 15V$, $T_{amb} = 25^{o}C$, f = 100Hz or f = 1000Hz)			0.01		$\frac{pA}{\sqrt{Hz}}$
t_s	Settling Time ($V_{CC} = \pm 15V$, $T_{amb} = 25^{o}C$) - (note 5)					µs
		LF155, LF255		4		
		LF156, LF256		1.5		
		LF157, LF257		1.5		

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ELECTRICAL CHARACTERISTICS

LF355, LF356, LF357 $0^{o}C \leq T_{amb} \leq +70^{o}C$ $V_{CC} = \pm 15V$

(unless otherwise specified)

Symbol	Parameter		LF355 - LF356 - LF357 Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage ($R_S = 50\Omega$) $T_{amb} = +25^{o}C$ $T_{min.} \leq T_{amb} \leq T_{max.}$			3	10 13	mV
I_{io}	Input Offset Current - (note 3) $T_{amb} = +25^{o}C$ $T_{min.} \leq T_{amb} \leq T_{max.}$			3	50 2	pA nA
I_{ib}	Input Bias Current - (note 3) $T_{amb} = 25^{o}C$ $T_{min.} \leq T_{amb} \leq T_{max.}$			20	200 8	pA nA
A_{vd}	Large Signal Voltage Gain ($R_L = 2k\Omega$, $V_o = \pm 10V$) $T_{amb} =+ 25^{o}C$ $T_{min.} \leq T_{amb} \leq T_{max.}$		25 15	200		V/mV
SVR	Supply Voltage Rejection Ratio - (note 4)		80	100		dB
I_{CC}	Supply Current, no Load $T_{amb} = 25^{o}C$	LF355 LF356, LF357		2 5	4 10	mA
DV_{io}	Input Offset Voltage Drift ($R_S = 50\Omega$) - (note 2)			5		$\mu V/^{o}C$
DV_{io}/V_{io}	Change in Average Temperature Coefficient with V_{IO} adjust ($R_S = 50\Omega$)			0.5		$\mu V/^{o}C$ per mV
V_{icm}	Input Common Mode Voltage Range ($T_{amb} = 25^{o}C$)		±10	+15.1 -12		V
CMR	Common Mode Rejection Ratio		80	100		dB
$\pm V_{OPP}$	Output Voltage Swing	$R_L = 10k\Omega$ $R_L = 2k\Omega$	±12 ±10	±13 ±12		V
GBP	Gain Bandwidth Product ($T_{amb} = 25^{o}C$)	LF355 LF356 LF357		2.5 5 20		MHz
SR	Slew Rate ($T_{amb} = 25^{o}C$) $A_V = 1$ $A_V = 5$	 LF355 LF356 LF357		 5 12 50		V/µs
R_i	Input Resistance ($T_{amb} = +25^{o}C$)			10^{12}		Ω
C_i	Input Capacitance ($T_{amb} = 25^{o}C$)			3		pF
e_n	Equivalent Input Noise Voltage ($T_{amb} = 25^{o}C$, $R_S = 100\Omega$) f = 1000Hz f = 100Hz	 LF355 LF356, LF357 LF355 LF356, LF357		 20 12 25 15		$\frac{nV}{\sqrt{Hz}}$
i_n	Equivalent Input Noise Current ($T_{amb} = 25^{o}C$, f = 100Hz or f = 1000Hz)			0.01		$\frac{pA}{\sqrt{Hz}}$
t_s	Settling Time ($T_{amb} = 25^{o}C$) - (note 5)	LF355 LF356, LF357		4 1.5		µs

155-04.TBL

Notes :

1. Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
2. The temperature coefficient of the adjusted input offset voltage changes only a small amount ($0.5\mu V/^{o}C$ typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.
3. The input bias currents are junction leakage currents which approximately double for every $10^{o}C$ increase in the junction temperature T_{amb}. Due to limited production test time, the input bias current measured is correlated to junction temperature.
   In a normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_{tot}-$T_{amb} = T_{amb} + R_{th(j\text{-}a)} \times P_{tot}$ where $R_{th(j\text{-}a)}$ is the thermal resistance from junction to ambient. Use of a heatsink is recommended if input currents are to be kept to a minimum.
4. Supply voltage rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practise.
5. Settling time is defined here, for a unity gain inverter connection using 2kΩ resistors for the LF155, LF156 series. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. For the LF157 series A_V = -5, the feedback resistor from output to input is 2kΩ and the output step is 10V.

APPLICATION HINTS

The LF155, LF156, LF157 series are op amps with J-FET input transistors. These JFETs have large reverse breakdown voltages from gate to source or drain eliminating the need of clamps across the inputs. Therefore large differential input voltages can easily be accommodated without a large increase of input currents. The maximum differential input voltage is independent of the supply voltage. However, neither of the negative input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive suplly can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unilimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

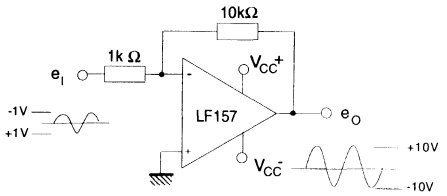
All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltages.

As with most amplifiers, care should be taken with lead dress, components placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimiz "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six time the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of that added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

TYPICAL CIRCUITS

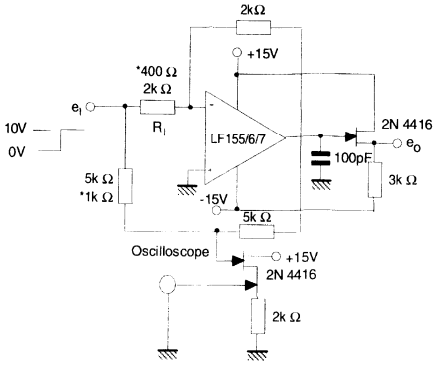
LARGE POWER BW AMPLIFIER



155-05.EPS

For distortion < 1% and a 20 V_{PP} V_O swing, power bandwidth is : 500kHz.

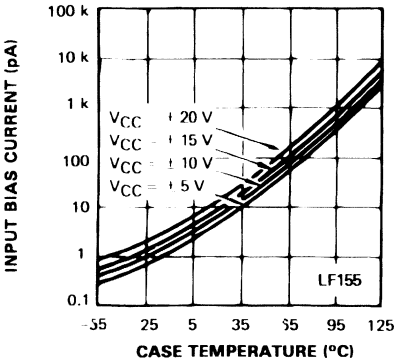
SETTLING TIME TEST CIRCUIT



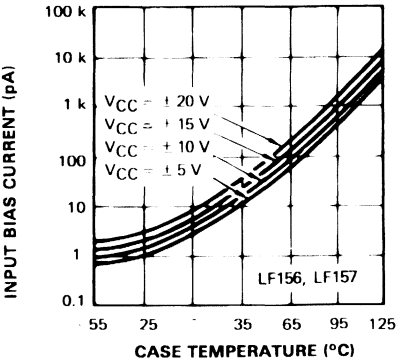
155-06.EPS

Settling time is tested with the LF155, LF156 connected as unity gain converter R_I = 2kΩ and LF157 connected for A_V = -5, R_I = 0.4kΩ

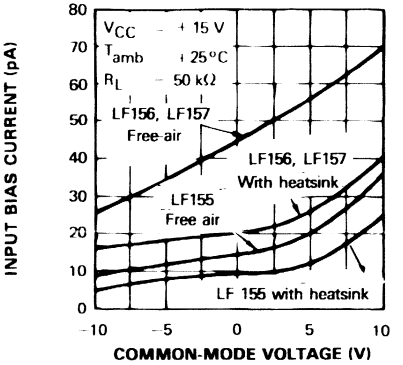
INPUT BIAS CURRENT



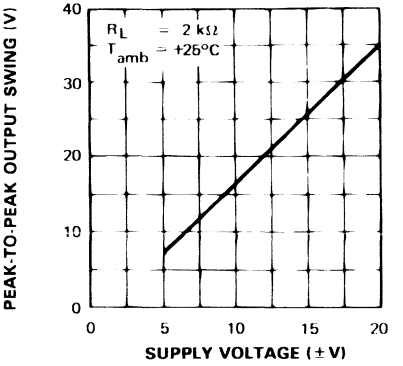
INPUT BIAS CURRENT



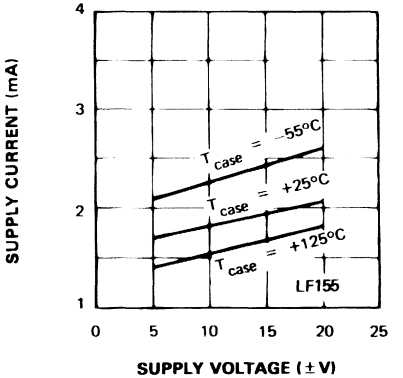
INPUT BIAS CURRENT



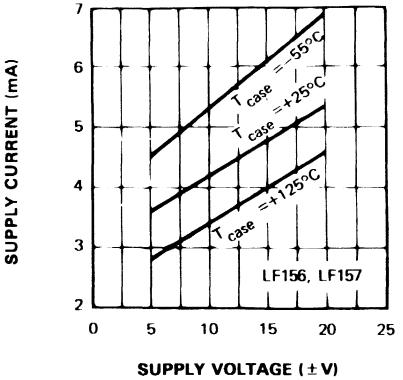
VOLTAGE SWING



SUPPLY CURRENT

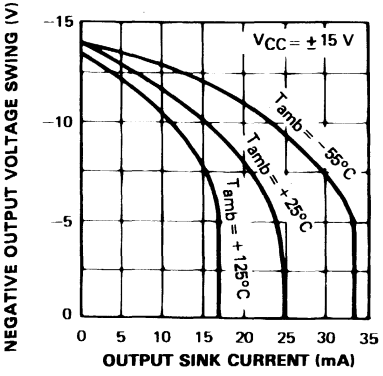


SUPPLY CURRENT

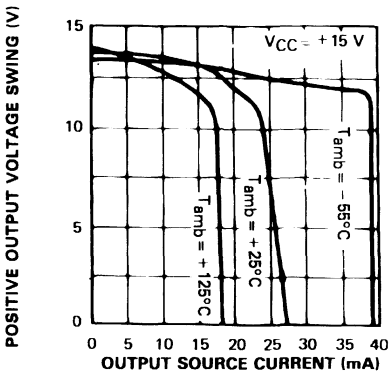


155-07.EPS

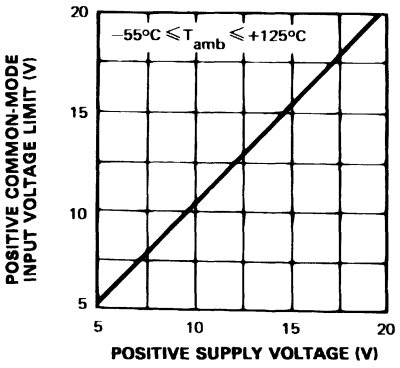
MAXIMUM NEGATIVE CURRENT



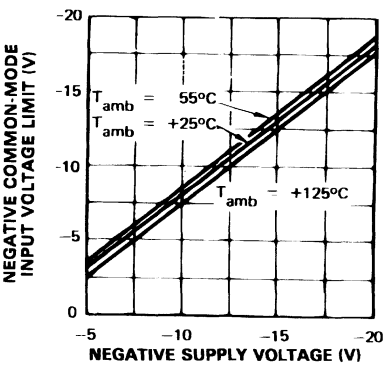
MAXIMUM POSITIVE CURRENT



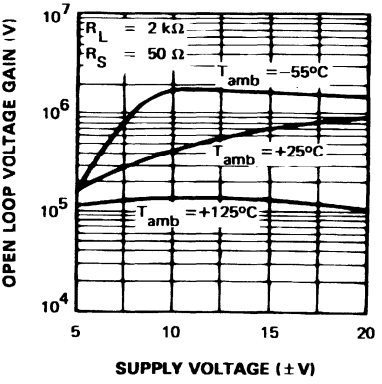
MAXIMUM POSITIVE COMMON-MODE INPUT VOLTAGE



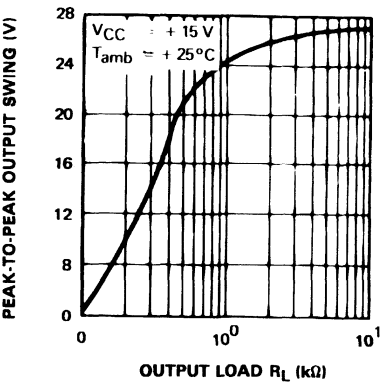
MAXIMUM NEGATIVE COMMON-MODE INPUT VOLTAGE



OPEN LOOP VOLTAGE GAIN

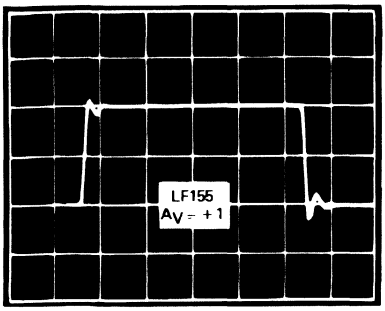


OUTPUT VOLTAGE SWING



155-08.EPS

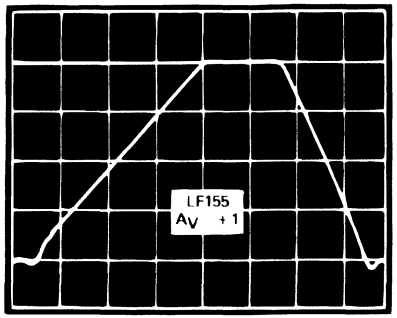
SMALL SIGNAL PULSE RESPONSE



OUTPUT VOLTAGE SWING (50 mV/DIV)

TIME (0.5 μs/DIV)

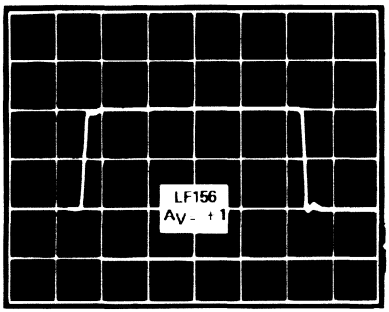
LARGE SIGNAL PULSE RESPONSE



OUTPUT VOLTAGE SWING (5 V/DIV)

TIME (1 μs/DIV)

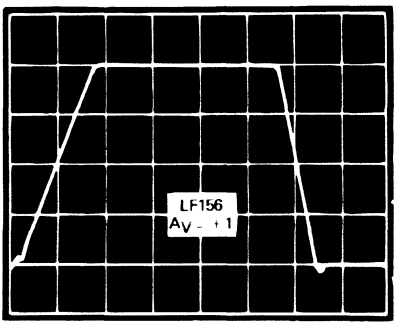
SMALL SIGNAL PULSE RESPONSE



OUTPUT VOLTAGE SWING (50 mV/DIV)

TIME (0.5 μs/DIV)

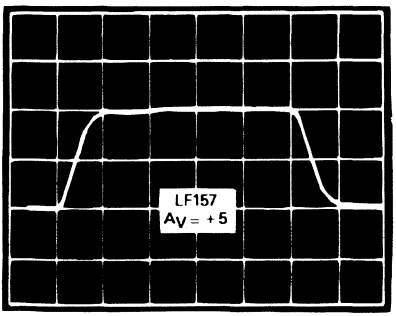
LARGE SIGNAL PULSE RESPONSE



OUTPUT VOLTAGE SWING (5 V/DIV)

TIME (1 μs/DIV)

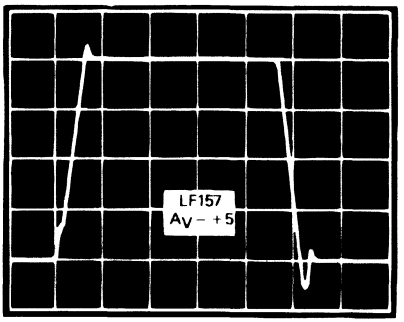
SMALL SIGNAL PULSE RESPONSE



OUTPUT VOLTAGE SWING (50 mV/DIV)

TIME (0.1 μs/DIV)

LARGE SIGNAL PULSE RESPONSE

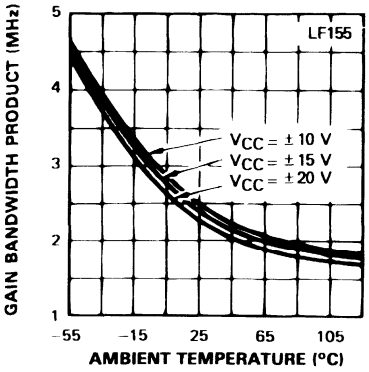


OUTPUT VOLTAGE SWING (5 V/DIV)

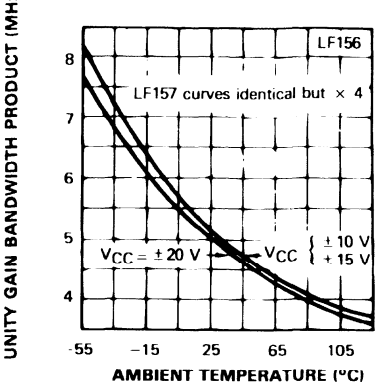
TIME (0.5 μs/DIV)

155-09.EPS

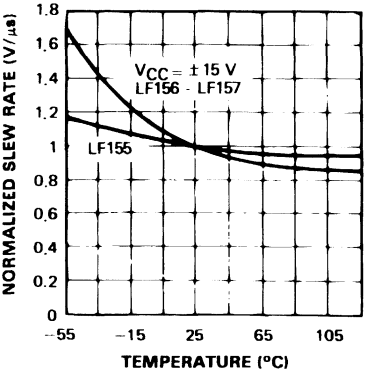
GAIN BANDWIDTH PRODUCT



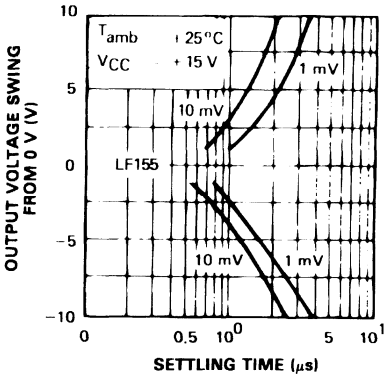
GAIN BANDWIDTH PRODUCT



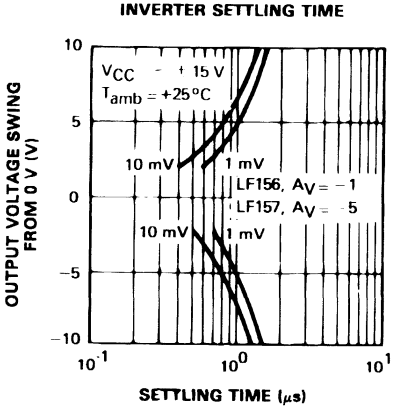
NORMALIZED SLEW RATE



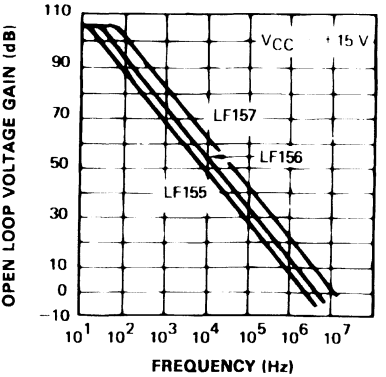
INVERTER SETTLING TIME



INVERTER SETTLING TIME

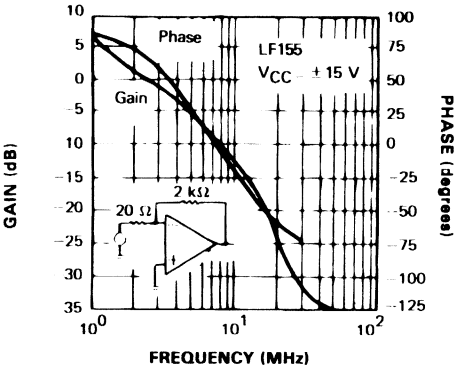


OPEN LOOP FREQUENCY RESPONSE

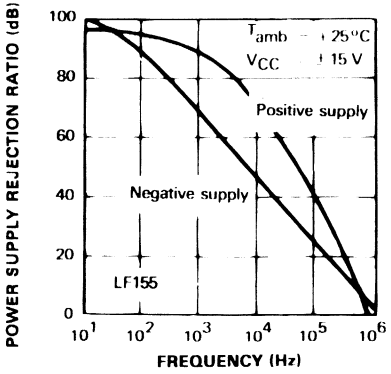


155-10.EPS

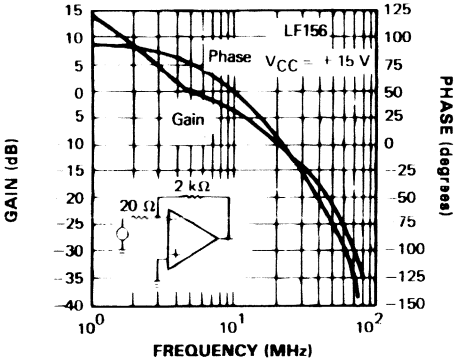
BODE PLOT



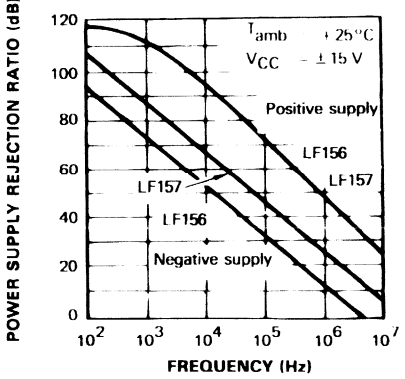
POWER SUPPLY REJECTION RATIO



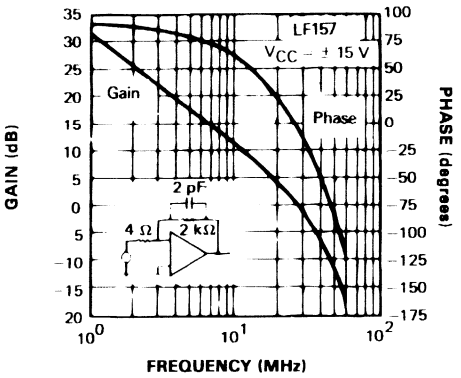
BODE PLOT



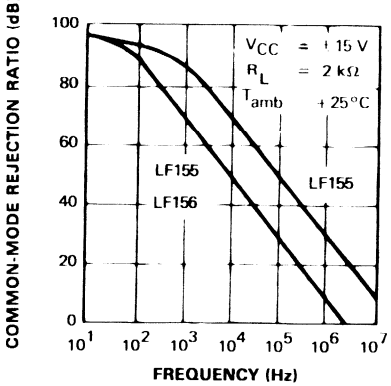
POWER SUPPLY REJECTION RATIO



BODE PLOT

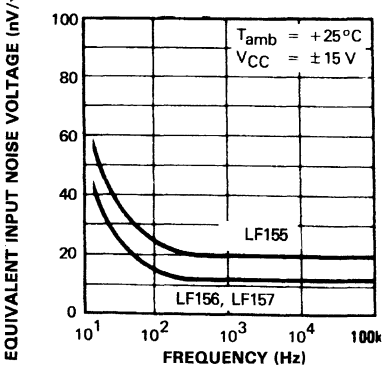


COMMON-MODE REJECTION RATIO

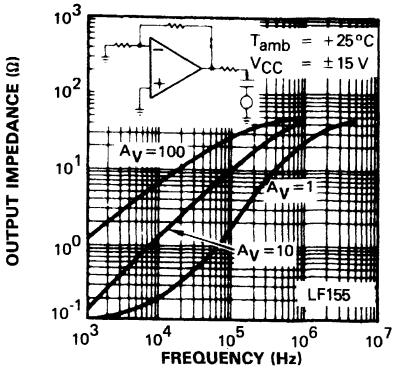


155-11.EPS

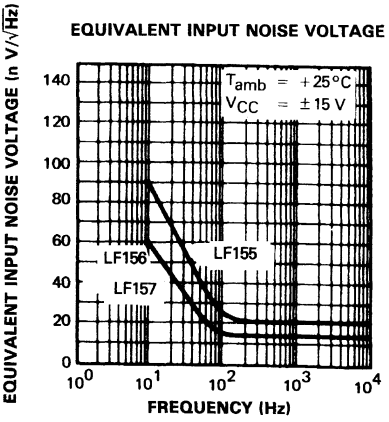
EQUIVALENT INPUT NOISE VOLTAGE (EXPANDED SCALE)



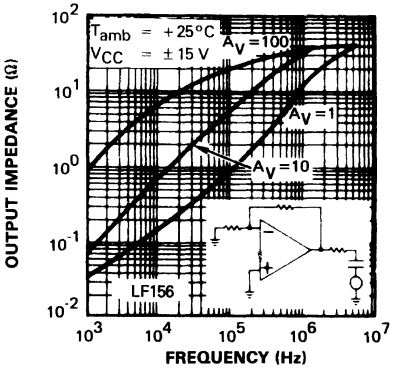
OUTPUT IMPEDANCE



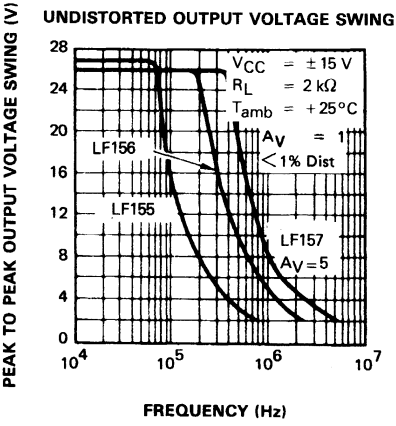
EQUIVALENT INPUT NOISE VOLTAGE



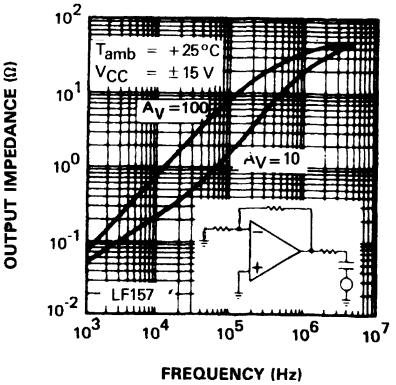
OUTPUT IMPEDANCE



UNDISTORTED OUTPUT VOLTAGE SWING



OUTPUT IMPEDANCE

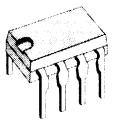


155-12.EPS

LM101A - LM201A LM301A

SINGLE OPERATIONAL AMPLIFIERS

	LM101A LM201A	LM301A
■ INPUT OFFSET VOLTAGE	0.7mV	2mV
■ INPUT BIAS CURRENT	25nA	70nA
■ INPUT OFFSET CURRENT	1.5nA	2nA
■ SLEW RATE AS INVERTING AMPLIFIER	10V/µs	10V/µs



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

J
CERDIP8
(Cerdip Package)

H
TO99
(Metal Can)

DESCRIPTION

The LM101A is a general-purpose operational amplifier. This amplifier offers many features : supply voltages from ±5 V to ±22 V, low current drain, overload protection on the input and output, no latch-up when the common-mode range is exceeded, freedom from oscillations and compensation with a single 30pF capacitor. It has advantages over internally compensated amplifiers in that the compensation can be tailored to the particular application : slew rates of 10 V/µs and bandwidths of 3.5MHz can be easily achieved.

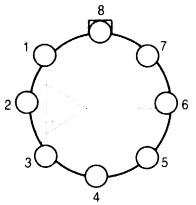
ORDER CODES

Part Number	Temperature Range	Package			
		H	N	J	D
LM101A	–55, +125°C	•	•	•	•
LM201A	–40, +105°C	•	•	•	•
LM301A	0, +70°C	•	•	•	•
Examples : LM101AH, LM201AN					

101-01.TBL

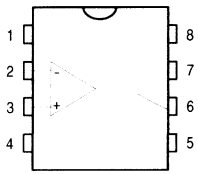
PIN CONNECTIONS (top views)

TO99



101-01.EPS

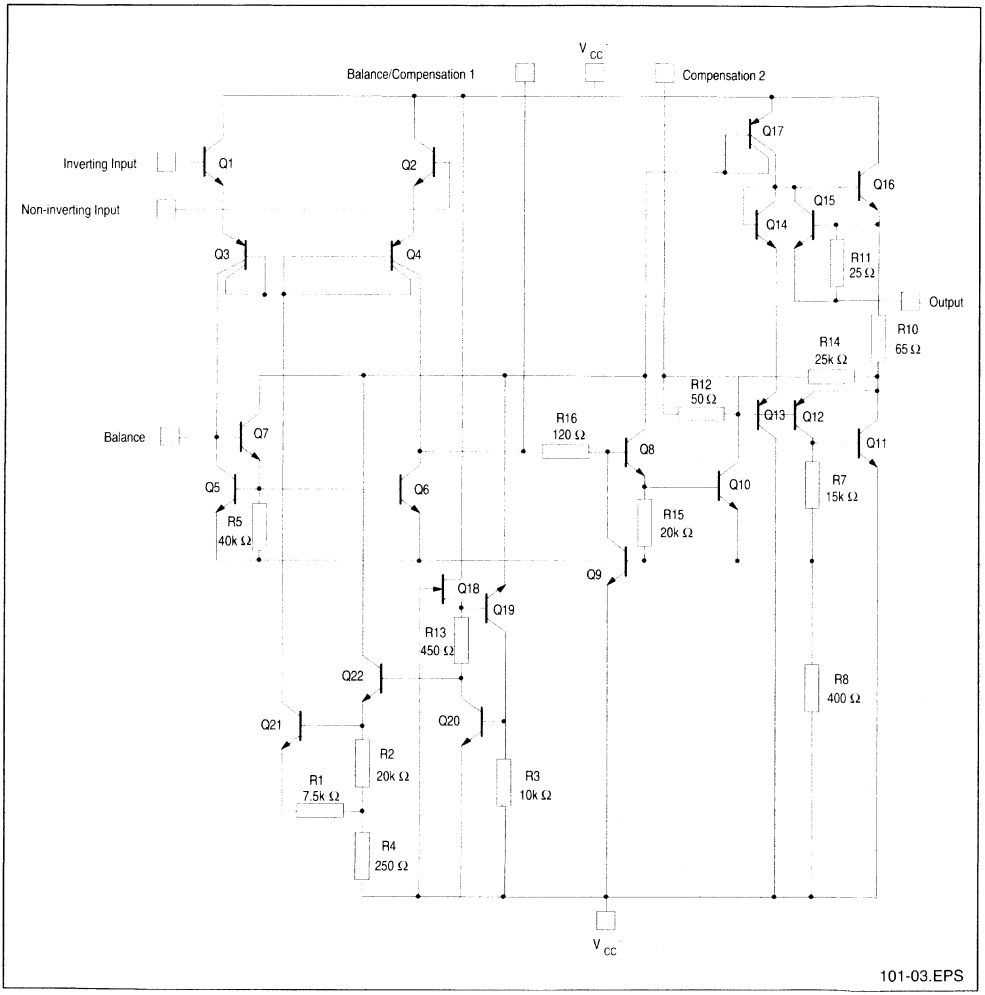
DIP8/CERDIP8
SO8



101-02.EPS

1 - Balance compensation 1
2 - Inverting input
3 - Non-inverting input
4 - V_{CC}^-
5 - Balance
6 - Output
7 - V_{CC}^+
8 - Compensation 2

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		LM101A	LM201A	LM301A	Unit
V_{CC}	Supply Voltage		±22	±22	±22	V
V_{id}	Differential Input Voltage		±30	±30	±30	V
V_i	Input Voltage		±15	±15	±15	V
	Output Short-circuit Duration			Infinite		
P_{tot}	Power Dissipation	N.J.H. Suffix D Suffix		500 300		mW
T_{oper}	Operating Free-air Temperature Range		−55 to +125	−40 to +105	0 to +70	°C
T_{stg}	Storage Temperature Range		−65 to +150	−65 to +150	−65 to +150	°C

101-02.TBL

ELECTRICAL CHARACTERISTICS

LM301A	$0^oC < Tamb < +70^oC$	$\pm5V \leq V_{CC} \leq \pm20V$	C1 = 30pF
LM201A	$-40^oC < Tamb < +105^oC$	$\pm5V \leq V_{CC} \leq \pm20V$	C1 = 30pF
LM101A	$-55^oC < Tamb < +125^oC$	$\pm5V \leq V_{CC} \leq \pm20V$	C1 = 30pF

* => $V_{CC} = \pm15V$, $T_{amb} = 25^oC$(unless otherwise specified)

Symbol	Parameter	LM101A - LM201A			LM301A			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage ($R_S \leq 10k\Omega$) $T_{amb} = 25^oC$ $T_{min.} \leq T_{amb} \leq T_{max.}$		0.7	2 3		2	7.5 10	mV
I_{ib}	Input Bias Current $T_{amb} = 25^oC$ $T_{min.} \leq T_{amb} \leq T_{max.}$		25	75 100		70	250 300	nA
I_{io}	Input Offset Current $T_{amb} = 25^oC$ $T_{min.} \leq T_{amb} \leq T_{max.}$		1.5	10 20		2	50 70	nA
A_{vd}	Large Signal Voltage Gain * ($V_O = \pm10V$, $R_L = 2k\Omega$) $T_{amb} = 25^oC$ $T_{min.} \leq T_{amb} \leq T_{max.}$	 50 25	 100		 25 15	 100		V/mV
SVR	Supply Voltage Rejection Ratio ($R_S \leq 10k\Omega$) $T_{amb} = 25^oC$ $T_{min.} \leq T_{amb} \leq T_{max.}$	 80 80	 96		 70 70	 96		dB
I_{CC}	Supply Current no Load $T_{amb} = 25^oC$ $T_{min.} \leq T_{amb} \leq T_{max.}$		1.8	3 3		1.8	3 3	mA
V_{icm}	Input Common Mode Voltage Range ($V_{CC} = \pm20V$) $T_{amb} = 25^oC$ $T_{min.} \leq T_{amb} \leq T_{max.}$	 ±15 ±15			 ±15 ±15			V
CMR	Common Mode Rejection Ratio ($R_S \leq 10k\Omega$) $T_{amb} = 25^oC$ $T_{min.} \leq T_{amb} \leq T_{max.}$	 80 80	 96		 70 70	 96		dB
I_{OS}	Output Short-circuit Current * $T_{amb} = 25^oC$	10	30	50	10	30	50	mA
$\pm V_{OPP}$	Output Voltage Swing * $T_{amb} = 25^oC$ $R_L = 10k\Omega$ $R_L = 2k\Omega$ $T_{min.} \leq T_{amb} \leq T_{max.}$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	 12 10 12 10	 14 13		 12 10 12 10	 14 13		V

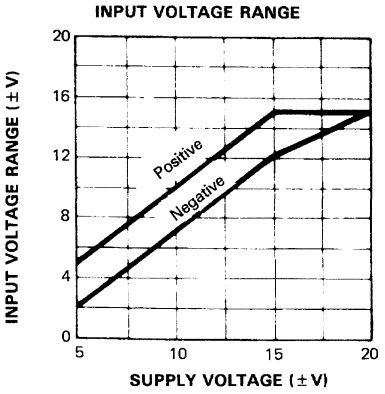
101-03.TBL

ELECTRICAL CHARACTERISTICS (continued)

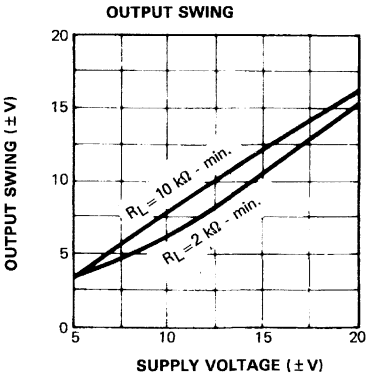
Symbol	Parameter	LM101A - LM201A			LM301A			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
SR	Slew Rate (V_I = ±10V, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain) - (note 1) *	0.25	0.5		0.25	0.5		V/µs
t_r	Rise Time (V_I = ±20 µV, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain) *		0.3			0.3		µs
K_{OV}	Overshoot (V_I = 20 mV, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)		5			5		%
Z_i	Input Impedance *	1.5	4		1.5	4		MΩ
R_o	Output Resistance *		75			75		Ω
GBP	Gain Bandwidth Product * (V_I = 10mV, R_L = 2kΩ, C_L = 100pF, f = 100kHz, T_{amb} = 25°C)	0.5	1		0.5	1		MHz
THD	Total Harmonic Distortion (f = 1kHz, A_V = 20dB, R_L = 2kΩ, V_O = $2V_{PP}$, C_L = 100pF, T_{amb} = 25°C)		0.015			0.015		%
e_n	Equivalent Input Noise Voltage (f = 1kHz, R_S = 100Ω)		25			25		$\frac{nV}{\sqrt{Hz}}$
DV_{io}	Input Offset Voltage Drift $T_{min.} \leq T_{amb} \leq T_{max.}$		3	15		6	30	µV/°C
DI_{io}	Input Offset Current Drift 25°C ≤ T_{amb} ≤ $T_{max.}$ $T_{min.} \leq T_{amb} \leq$ 25°C		10 20	100 200		10 20	300 600	pA/°C

101-04.TBL

Note : 1.May be improved up to 10V/µs in inverting amplifier configuration (see basic diagram).

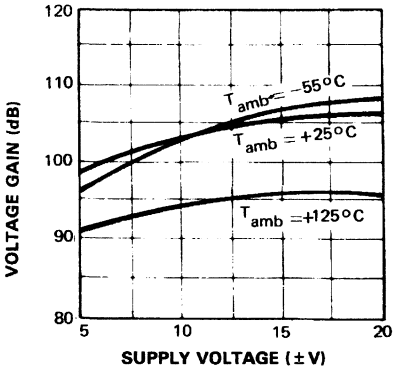


101-04.EPS



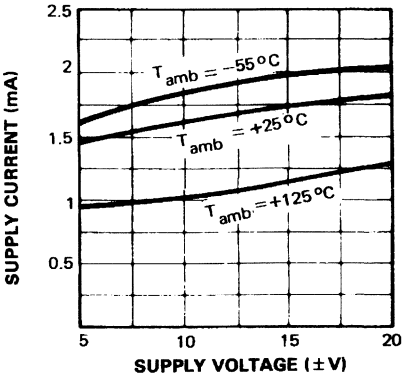
101-05.EPS

VOLTAGE GAIN



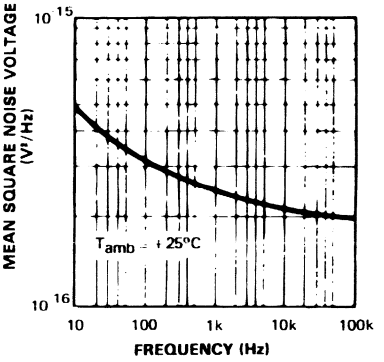
101-06.EPS

SUPPLY CURRENT



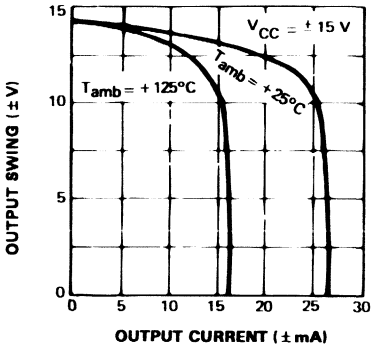
101-07.EPS

INPUT NOISE VOLTAGE



101-08.EPS

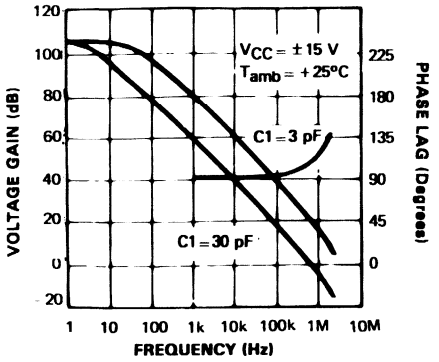
CURRENT LIMITING



101-09.EPS

SINGLE POLE COMPENSATION

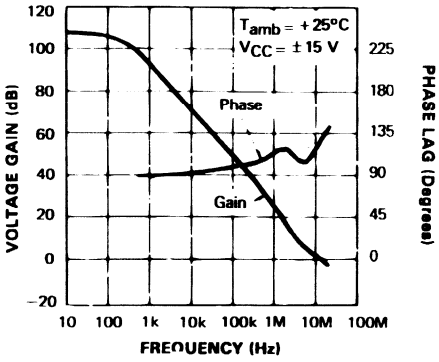
OPEN LOOP FREQUENCY RESPONSE



101-10.EPS

FEED FORWARD COMPENSATION

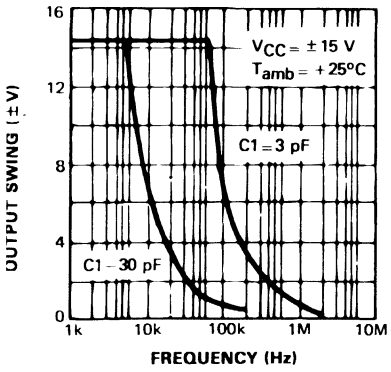
OPEN LOOP FREQUENCY RESPONSE



101-11.EPS

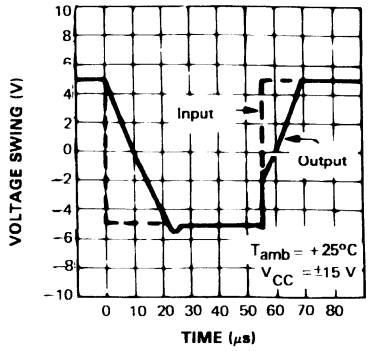
SINGLE POLE COMPENSATION

LARGE SIGNAL FREQUENCY RESPONSE



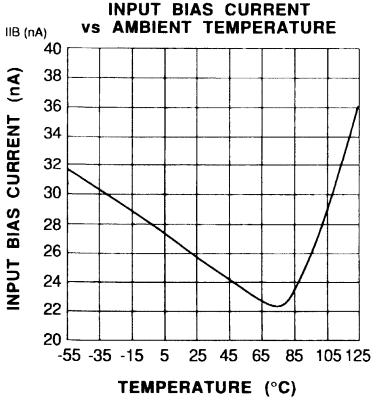
101-12.EPS

VOLTAGE FOLLOWER PULSE RESPONSE



101-14.EPS

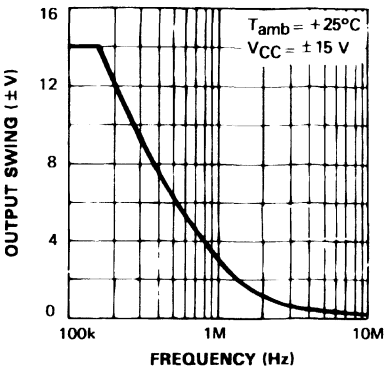
INPUT BIAS CURRENT vs AMBIENT TEMPERATURE



101-16.EPS

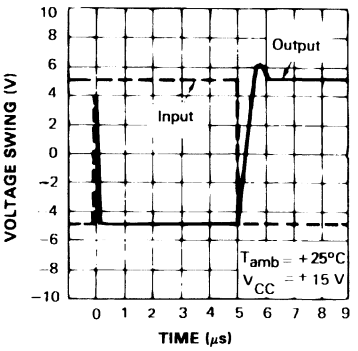
FEED FORWARD COMPENSATION

LARGE SIGNAL FREQUENCY RESPONSE



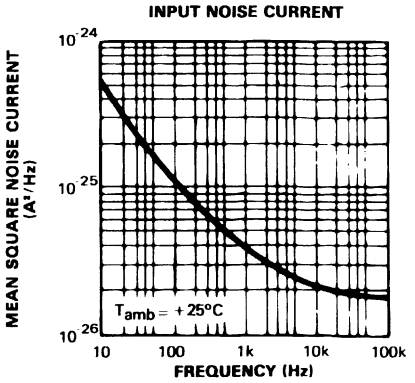
101-13.EPS

INVERTER PULSE RESPONSE



101-15.EPS

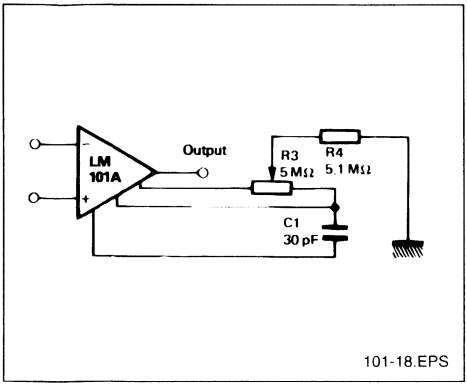
INPUT NOISE CURRENT



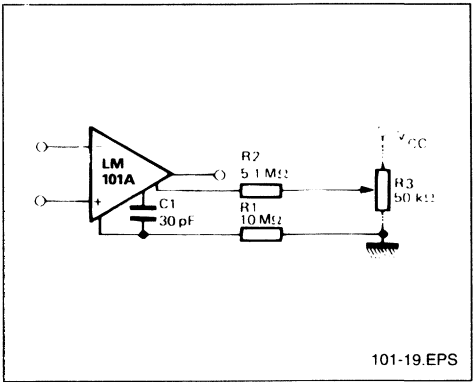
101-17.EPS

BASIC DIAGRAM

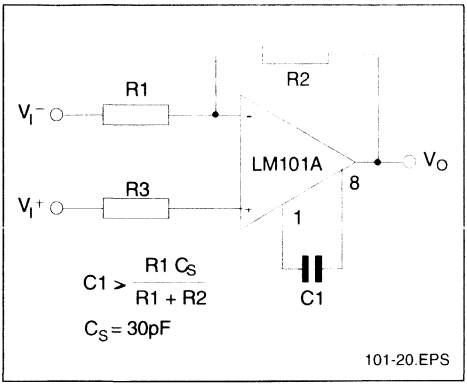
BALANCING CIRCUIT



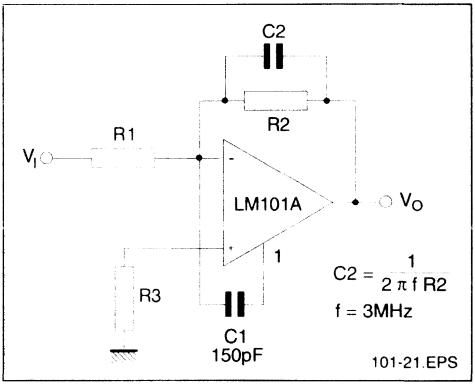
ALTERNATE BALANCING CIRCUIT



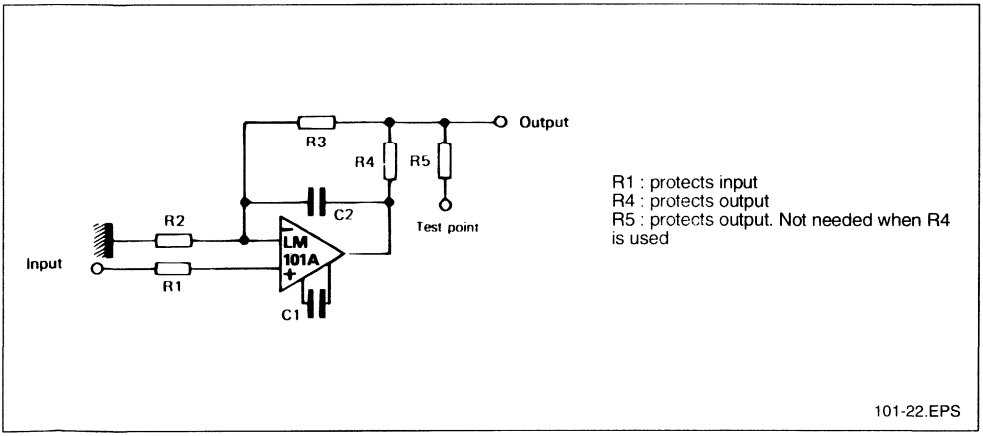
SINGLE POLE COMPENSATION



FEEDFORWARD COMPENSATION

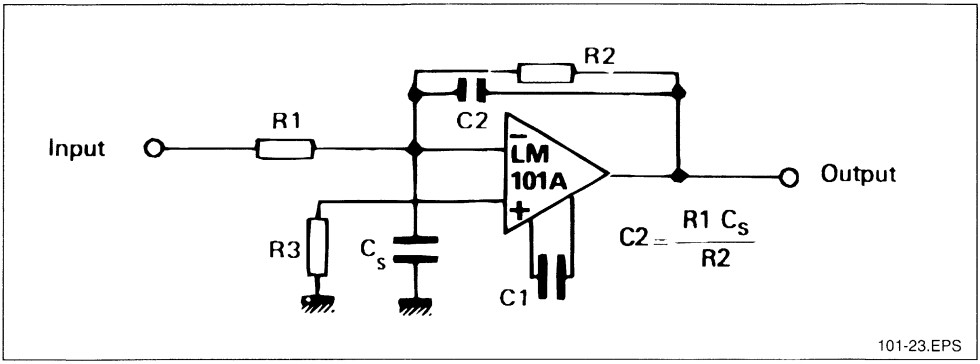


PROTECTING AGAINST GROSS FAULT CONDITIONS

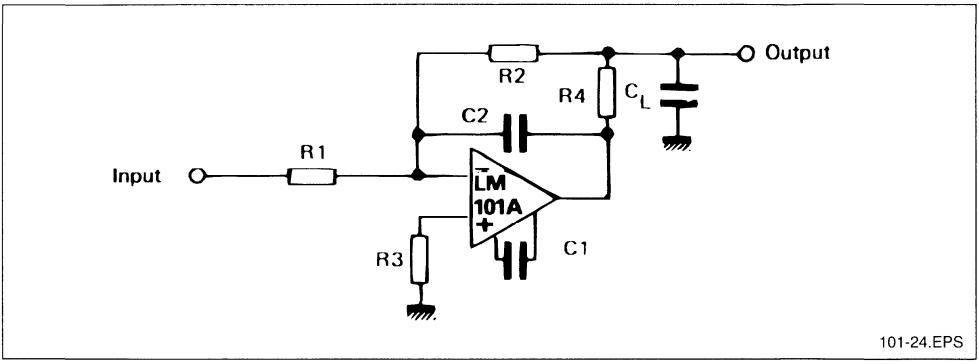


BASIC DIAGRAM (continued)

COMPENSATING FOR STRAY INPUT CAPACITANCES OR LARGE FEEDBACK RESISTOR

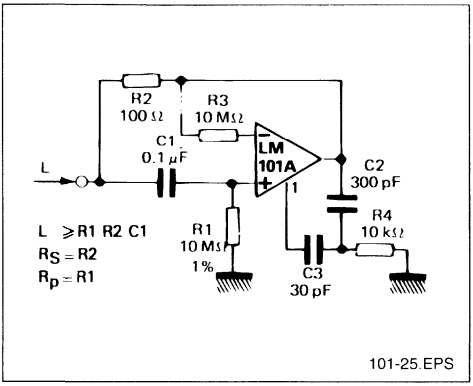


ISOLATING LARGE CAPACITIVE LOADS

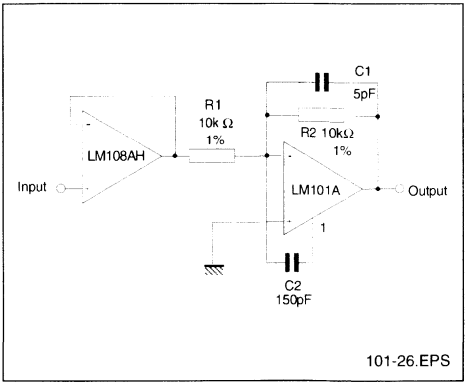


TYPICAL APPLICATIONS

SIMULATED INDUCTOR

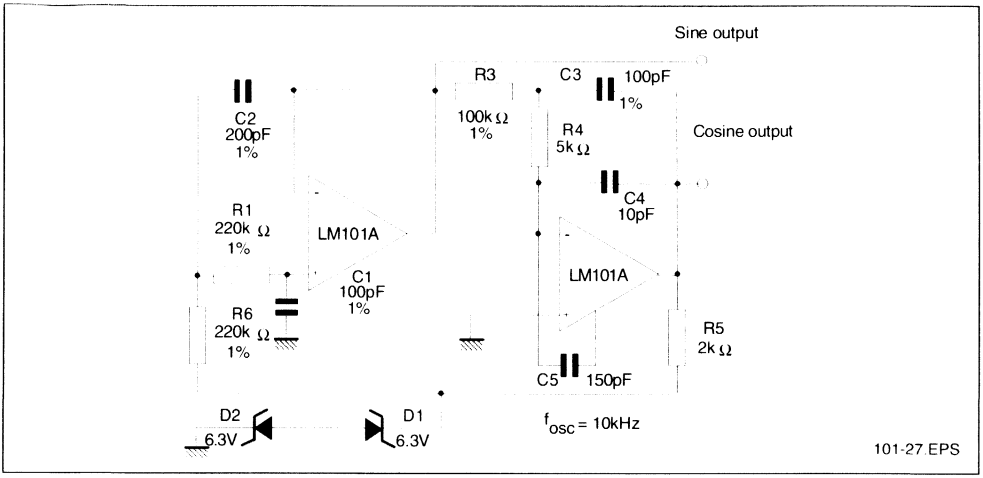


FAST AMPLIFIER WITH HIGH INPUT IMPEDANCE

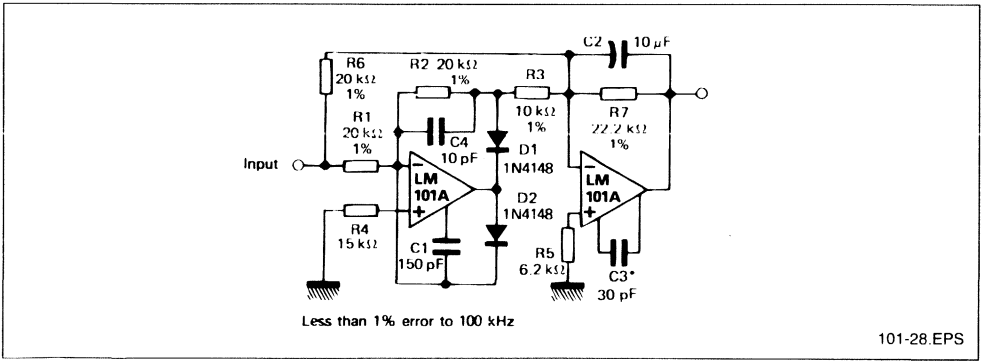


TYPICAL APPLICATIONS (continued)

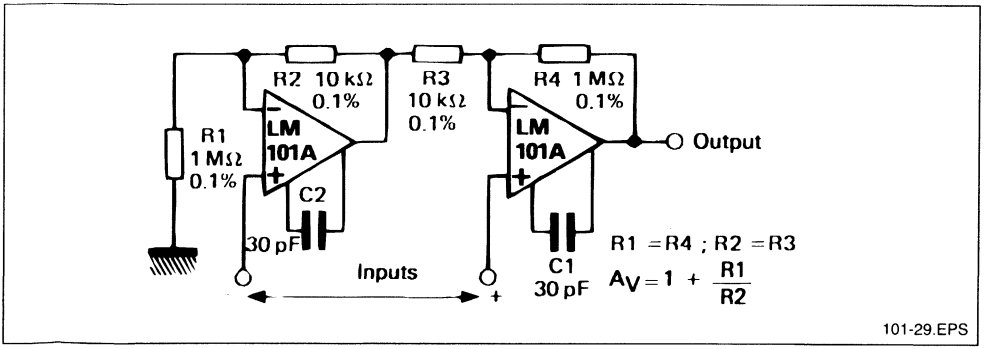
SINE WAVE OSCILLATOR



FAST AC/DC CONVERTER

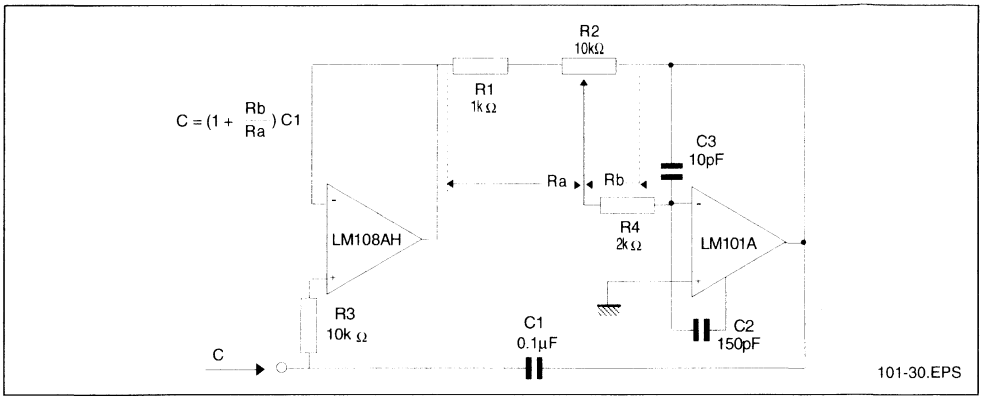


INSTRUMENTATION AMPLIFIER

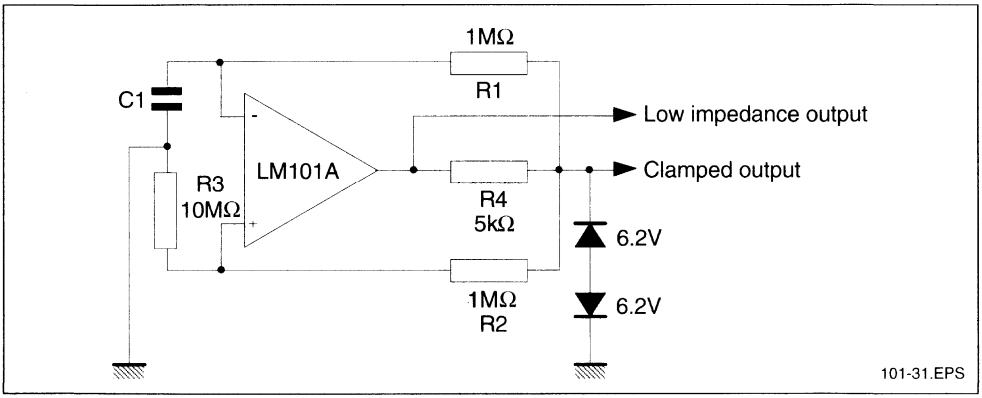


TYPICAL APPLICATIONS (continued)

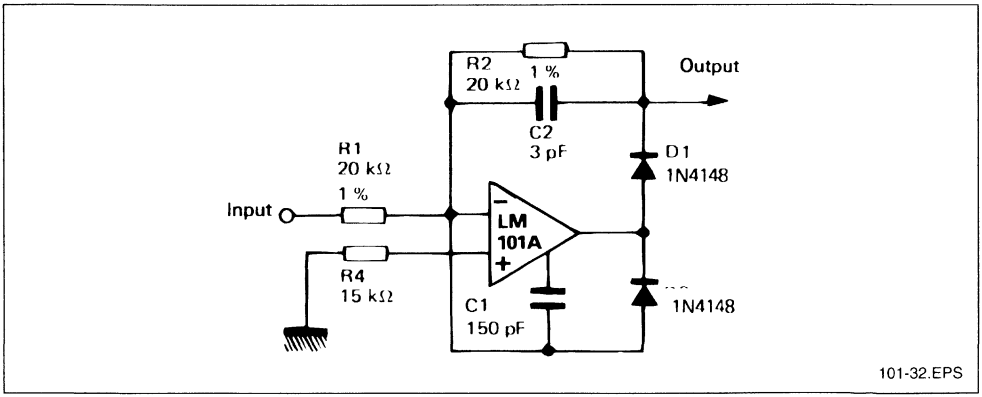
VARIABLE CAPACITANCE MULTIPLIER



LOW FREQUENCY SQUARE WAVE GENERATOR



FAST HALF WAVE RECTIFIER

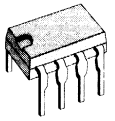


LM108/A - LM208/A LM308/A

PRECISION SINGLE OPERATIONAL AMPLIFIERS

Outstanding characteristics of LM108A :

- INPUT OFFSET VOLTAGE : 0.5mV MAXIMUM
- INPUT BIAS CURRENT : 3nA MAXIMUM OVER FULL TEMPERATURE RANGE
- INPUT OFFSET CURRENT : 0.4nA MAXIMUM OVER FULL TEMPERATURE RANGE
- POWER SUPPLY CURRENT : 600µA MAXIMUM
- GUARANTEED DRIFT CHARACTERISTICS
- SLEW RATE OF 10V/µs AS INVERTING AMPLIFIER



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

J
CERDIP8
(Cerdip Package)

H
TO99
(Metal Can)

DESCRIPTION

The LM308,A is a precision operational amplifier having specifications a factor ten better than FET amplifiers over a -55°C to +125°C temperature range. Selected units are available with offset voltages less than 1mV and drifts less than 5mV/°C. This makes it possible to eliminate offset adjustments, in most cases.

The device operates with supply voltages from ±2V to ±22V and has sufficient supply rejection to use unregulated supplies. Although the circuit is interchangeable with and uses the same compensation as the LM101A, an alternate compensation scheme can be used to make it particularly insensitive to power supply noise and to make supply bypass capacitors unnecessary.

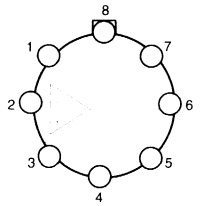
ORDER CODES

Part Number	Temperature Range	Package			
		H	N	J	D
LM108/A	–55, +125°C	•	•	•	•
LM208/A	–40, +105°C	•	•	•	•
LM308/A	0, +70°C	•	•	•	•
Examples : LM108H, LM108AH, LM308N					

108-01.TBL

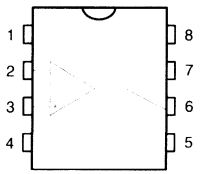
PIN CONNECTIONS (top views)

TO99



108-01.EPS

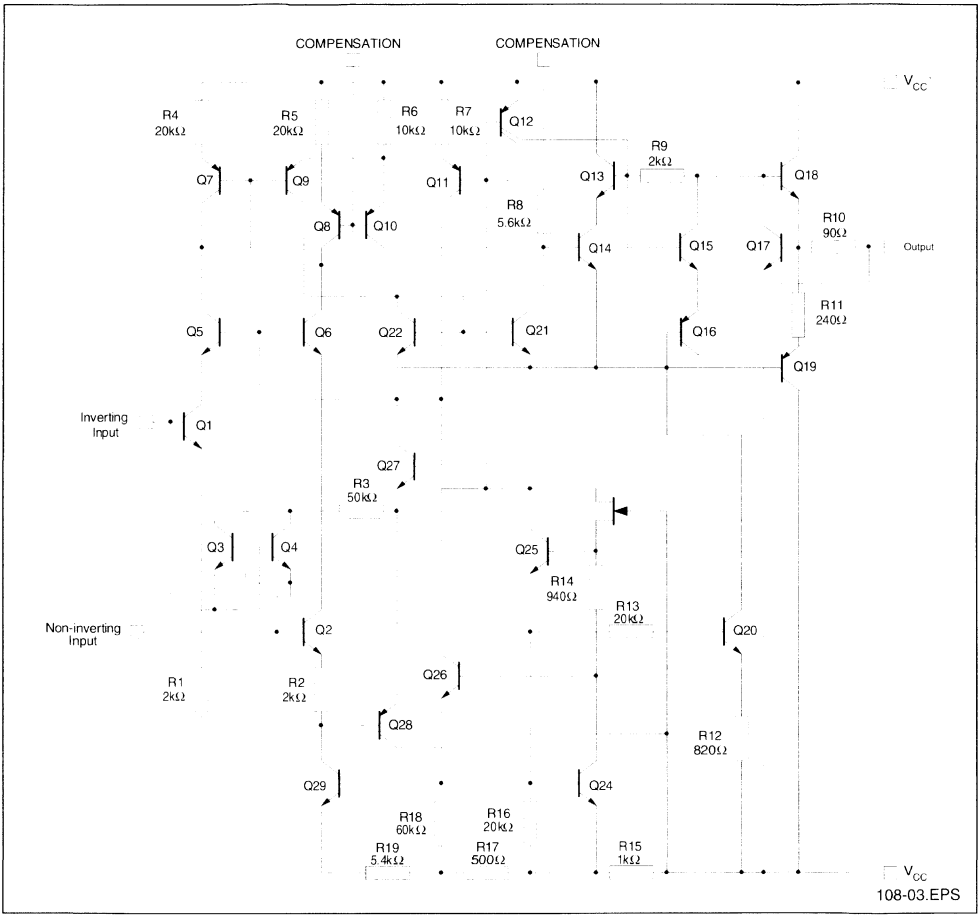
DIP8/CERDIP8
SO8



108-02.EPS

1 - Frequency compensation
2 - Inverting input
3 - Non-inverting input
4 - V_{CC}^-
5 - N.C.
6 - Output
7 - V_{CC}^+
8 - Frequency Compensation

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	LM108,A	LM208,A	LM308,A	Unit
V_{CC}	Supply Voltage	±22	±22	±22	V
V_i	Input Voltage - (note 2)	±15	±15	±15	V
I_{id}	Differential Input Current - (note 1)	±10	±10	±10	
P_{tot}	Power Dissipation		500		mW
	Output Short-circuit Duration		Infinite		
T_{oper}	Operating Free-air Temperature Range	−55 to +125	−40 to +105	0 to +70	°C
T_{stg}	Storage Temperature Range	−65 to +150	−65 to +150	−65 to +150	°C

108-02 TBL

Notes : 1. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS

$\pm 5V \leq V_{CC} \leq \pm 20V$, $C_1 = 30pF$, $T_{amb} = 25°C$ (unless otherwise specified)

Symbol	Parameter	LM108A - LM208A LM308A			Unit
		Min.	Typ.	Max.	
V_{io}	Input Offset Voltage ($R_S \leq 10k\Omega$) $T_{amb} = 25°C$ $T_{min.} \leq T_{amb} \leq T_{max.}$ LM108A - LM208A		0.3	0.5 0.75 1	mV
I_{ib}	Input Bias Current $T_{amb} = 25°C$ LM108A - LM208A LM308A $T_{min.} \leq T_{amb} \leq T_{max.}$ LM108A - LM208A LM308A		0.6	2 4 3 7	nA
I_{io}	Input Offset Current $T_{amb} = 25°C$ $T_{min.} \leq T_{amb} \leq T_{max.}$		0.05	0.2 0.4	nA
A_{vd}	Large Signal Voltage Gain ($V_{cc} = \pm 15V$, $V_O = \pm 10V$, $R_L = 10k\Omega$) $T_{amb} = 25°C$ $T_{min.} \leq T_{amb} \leq T_{max.}$	80 60	300		V/mV
SVR	Supply Voltage Rejection Ratio ($R_S \leq 10k\Omega$) $T_{amb} = 25°C$ $T_{min.} \leq T_{amb} \leq T_{max.}$	96 96	110		dB
I_{CC}	Supply Current no Load $T_{amb} = 25°C$ $T_{min.} \leq T_{amb} \leq T_{max.}$		0.3	0.6 0.6	mA
V_{icm}	Input Common Mode Voltage Range ($V_{CC} = \pm 15V$) $T_{amb} = 25°C$ $T_{min.} \leq T_{amb} \leq T_{max.}$	± 14 ± 14			V
CMR	Common Mode Rejection Ratio ($R_S \leq 10k\Omega$) $T_{amb} = 25°C$ $T_{min.} \leq T_{amb} \leq T_{max.}$	96 96	110		dB
I_{os}	Output Short-circuit Current ($V_{CC} = \pm 15V$)	3	10	20	mA
$\pm V_{opp}$	Output Voltage Swing ($V_{CC} = \pm 15V$, $R_L = 10k\Omega$) $T_{amb} = 25°C$ $T_{min.} \leq T_{amb} \leq T_{max.}$	13 13	14		V
SR	Slew Rate ($V_{CC} = \pm 15V$, $V_i = \pm 10V$, $R_L = 10k\Omega$, $C_L = 100pF$, $T_{amb} = 25°C$, unity gain)		0.15		V/µs
t_r	Rise Time ($V_{CC} = \pm 15V$, $V_i = \pm 20mV$, $R_L = 10k\Omega$, $C_L = 100pF$, unity gain)		0.7		µs
K_{ov}	Overshoot ($V_{CC} = \pm 15V$, $V_i = 20$ mV, $R_L = 10k\Omega$, $C_L = 100pF$, unity gain)		10		%
R_i	Input Resistance ($V_{CC} = \pm 15V$)	30	70		MΩ
GBP	Gain Bandwidth Product ($V_{CC} = \pm 15V$, $V_i = 10mV$, $R_L = 10k\Omega$, $C_L = 100pF$, f = 100kHz)	0.3	0.8		MHz
THD	Total Harmonic Distortion ($V_{CC} = \pm 15V$, f = 1kHz, $A_V = 20dB$, $R_L = 10k\Omega$, $V_O = 2V_{PP}$, $C_L = 100pF$)		0.12		%
e_n	Equivalent Input Noise Voltage ($V_{CC} = \pm 15V$, f = 1kHz, $R_s = 100\Omega$)		20		$\frac{nV}{\sqrt{Hz}}$
DV_{io}	Input Offset Voltage Drift $T_{min.} \leq T_{amb} \leq T_{max.}$		1	5	µV/°C
DI_{io}	Input Offset Current Drift $T_{min.} \leq T_{amb} \leq 25°C$		0.5	2.5	pA/°C

108-03.TBL

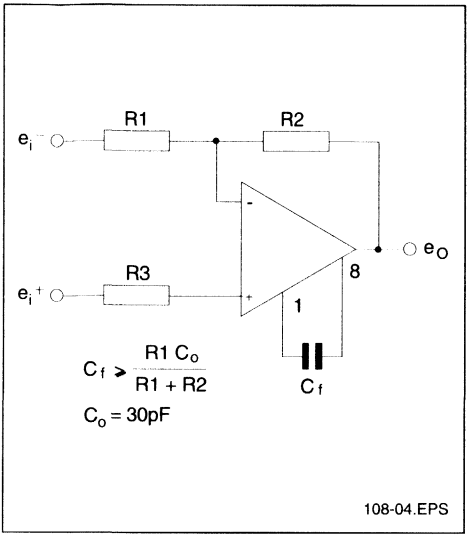
ELECTRICAL CHARACTERISTICS

$\pm 5V \leq V_{CC} \leq \pm 20V$, $C_1 = 30pF$, $T_{amb} = 25°C$ (unless otherwise specified)

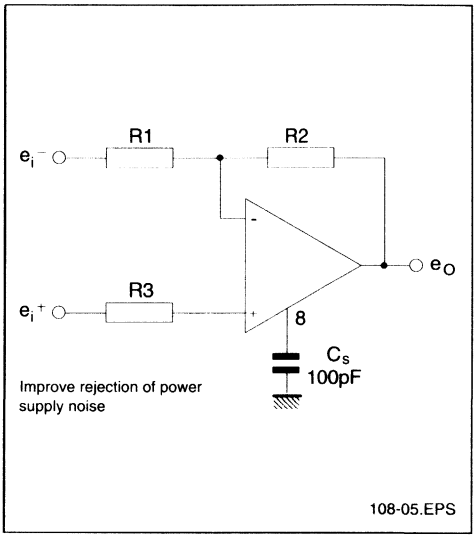
Symbol	Parameter	LM108 - LM208			LM308			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage ($R_S \leq 10k\Omega$) $T_{amb} = 25°C$ $T_{min.} \leq T_{amb} \leq T_{max.}$		0.7	2 3		2	7.5 10	mV
I_{ib}	Input Bias Current $T_{amb} = 25°C$ $T_{min.} \leq T_{amb} \leq T_{max.}$		0.6	2 3		0.6	7 10	nA
I_{io}	Input Offset Current $T_{amb} = 25°C$ $T_{min.} \leq T_{amb} \leq T_{max.}$		0.05	0.2 0.4		0.05	1 1.5	nA
A_{vd}	Large Signal Voltage Gain ($V_{cc} = \pm 15V$, $V_O = \pm 10V$, $R_L = 10k\Omega$) $T_{amb} = 25°C$ $T_{min.} \leq T_{amb} \leq T_{max.}$	50 25	300		25 15	300		V/mV
SVR	Supply Voltage Rejection Ratio ($R_S \leq 10k\Omega$) $T_{amb} = 25°C$ $T_{min.} \leq T_{amb} \leq T_{max.}$	80 80	96		80 80	96		dB
I_{CC}	Supply Current no Load $T_{amb} = 25°C$ $T_{min.} \leq T_{amb} \leq T_{max.}$		0.3	0.6 0.6		0.3	0.8 0.8	mA
V_{icm}	Input Common Mode Voltage Range ($V_{CC} = \pm 15V$) $T_{amb} = 25°C$ $T_{min.} \leq T_{amb} \leq T_{max.}$	±13.5 ±13.5			±14 ±14			V
CMR	Common Mode Rejection Ratio ($R_S \leq 10k\Omega$) $T_{amb} = 25°C$ $T_{min.} \leq T_{amb} \leq T_{max.}$	80 80	100		80 80	100		dB
I_{os}	Output Short-circuit Current ($V_{CC} = \pm 15V$)	3	10	20	3	10	20	mA
$\pm V_{opp}$	Output Voltage Swing ($V_{CC} = \pm 15V$, $R_L = 10k\Omega$) $T_{amb} = 25°C$ $T_{min.} \leq T_{amb} \leq T_{max.}$	13 13	14		13 13	14		V
SR	Slew Rate ($V_{CC} = \pm 15V$, $V_i = \pm 10V$, $R_L = 10k\Omega$, $C_L = 100pF$, $T_{amb} = 25°C$, unity gain)		0.15			0.15		V/µs
t_r	Rise Time ($V_{CC} = \pm 15V$, $V_i = \pm 20mV$, $R_L = 10k\Omega$, $C_L = 100pF$, unity gain)		0.7			0.7		µs
K_{ov}	Overshoot ($V_{CC} = \pm 15V$, $V_i = 20$ mV, $R_L = 10k\Omega$, $C_L = 100pF$, unity gain)		10			10		%
R_i	Input Resistance ($V_{CC} = \pm 15V$)	30	70		30	70		MΩ
GBP	Gain Bandwidth Product ($V_{CC} = \pm 15V$, $V_i = 10mV$, $R_L = 10k\Omega$, $C_L = 100pF$, f = 100kHz)	0.3	0.8		0.3	0.8		MHz
THD	Total Harmonic Distortion ($V_{CC} = \pm 15V$, f = 1kHz, $A_V = 20dB$, $R_L = 10k\Omega$, $V_O = 2V_{PP}$, $C_L = 100pF$)		0.12			0.12		%
e_n	Equivalent Input Noise Voltage ($V_{CC} = \pm 15V$, f = 1kHz, $R_s = 100\Omega$)		20			20		$\frac{nV}{\sqrt{Hz}}$
DV_{io}	Input Offset Voltage Drift $T_{min.} \leq T_{amb} \leq T_{max.}$		3	15		6	30	µV/°C
DI_{io}	Input Offset Current Drift $T_{min.} \leq T_{amb} \leq 25°C$		0.5	2.5		2	10	pA/°C

BASIC DIAGRAMS

STANDARD COMPENSATION CIRCUIT

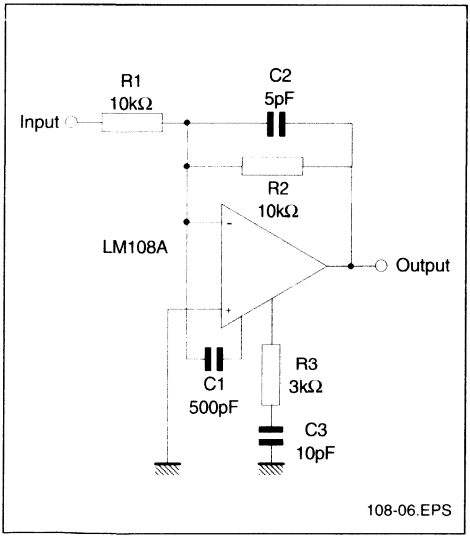


ALTERNATIVE FREQUENCY COMPENSATION

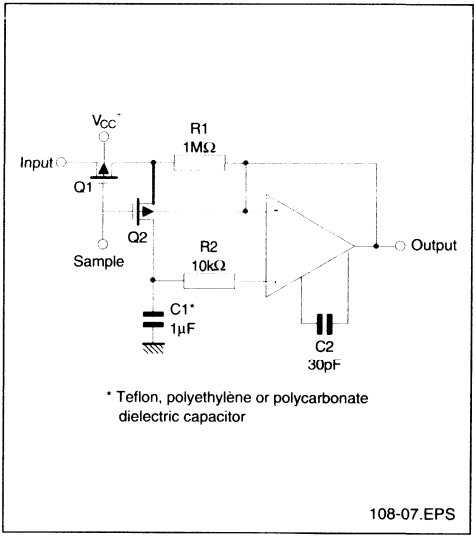


TYPICAL APPLICATIONS

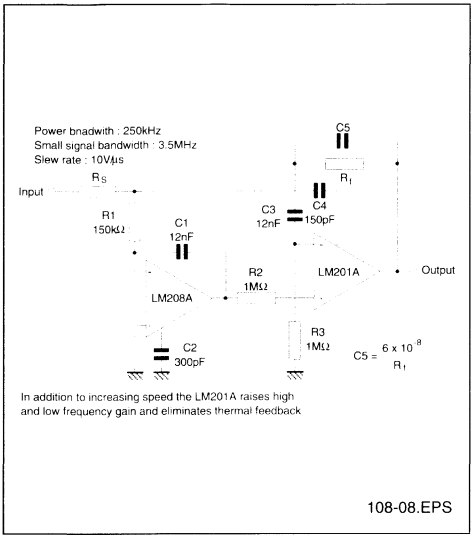
STANDARD FEEDFORWARD



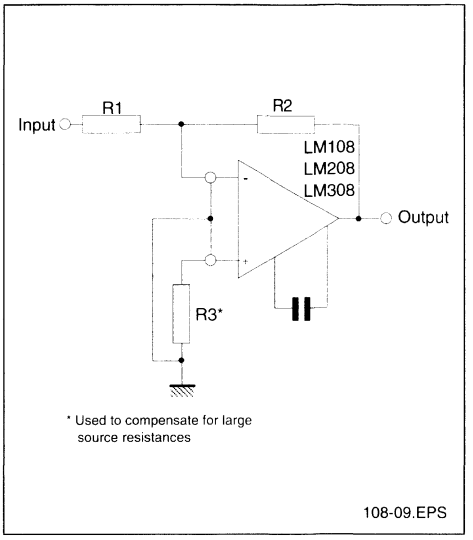
SAMPLE AND HOLD



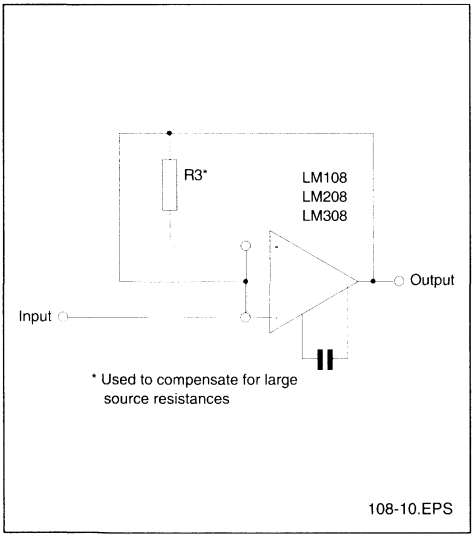
FAST SUMMING AMPLIFIER



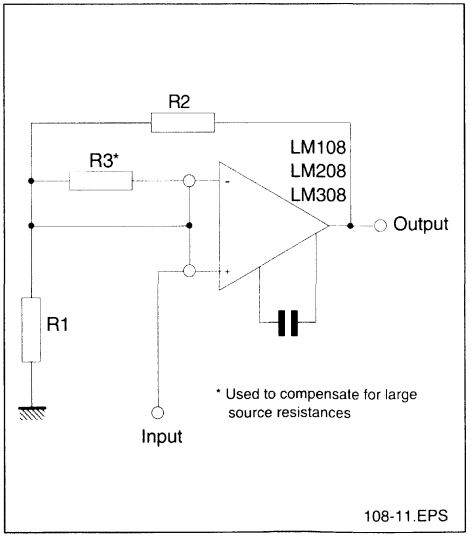
INVERTING AMPLIFIER



FOLLOWING AMPLIFIER



NON-INVERTING AMPLIFIER

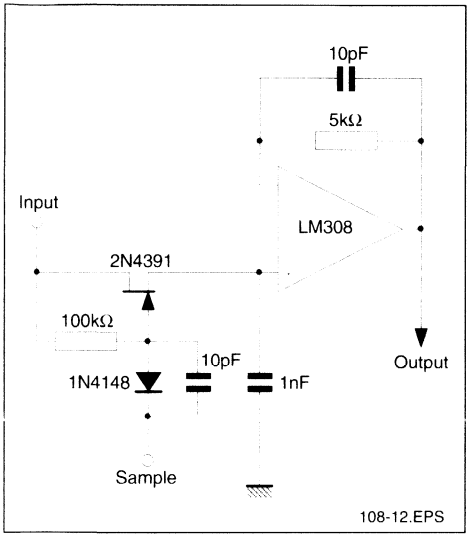


INPUT GUARDING

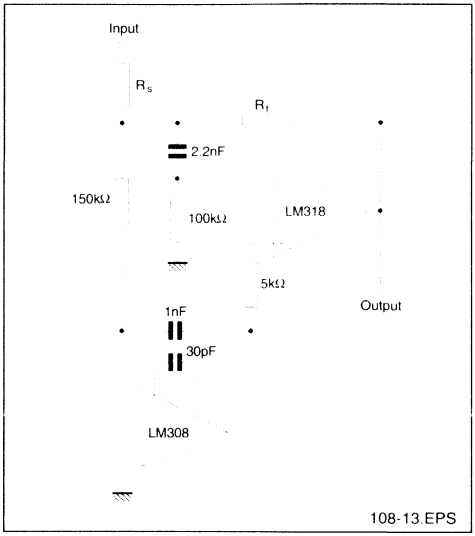
Leakage currents are on the verge of causing trouble at +125°C. The standard pin configuration of most IC op amps has the input pins adjacent to pins which are the supply potentials. Therefore, it is advisable to employ guarding to reduce the voltage difference between the inputs and adjacent metal runs. A ten-lead pin circle is used, and the leads of the IC are formed so that the holes adjacent to the inputs are vacant when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low impedance point that is at the same potential as the inputs.

TYPICAL APPLICATION DIAGRAMS

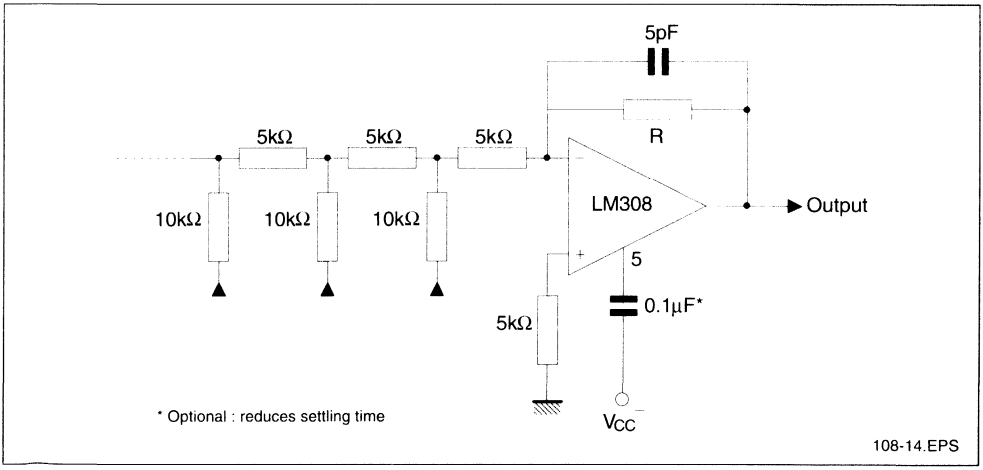
FAST SAMPLE AND HOLD



FAST SUMMING AMPLIFIER WITH LOW INPUT CURRENT



D/A CONVERTER USING LADDER NETWORK

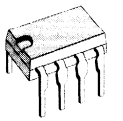


SGS-THOMSON MICROELECTRONICS

LM111 - LM211 LM311

VOLTAGE COMPARATORS

- MAXIMUM INPUT CURRENT : 150nA
- MAXIMUM OFFSET CURRENT : 20nA
- DIFFERENTIAL INPUT VOLTAGE RANGE : ±30V
- POWER CONSUMPTION : 135mW AT ±15V
- SUPPLY VOLTAGE : +5V TO ±15V
- OUTPUT CURRENT : 50mA



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

J
CERDIP 8
(Cerdip Package)

H
TO99
(Metal Can)

DESCRIPTION

The LM111, LM211 and LM311 are voltage comparators that have low input currents.

They are also designed to operate over a wide range of supply voltages : from standard ±15V operational amplifier supplies down to the single +5V supply used for IC logic.

Their output is compatible with RTL-DTL and TTL as well as MOS circuits and can switch voltages up to +50V at output currents as high as 50mA.

ORDER CODES

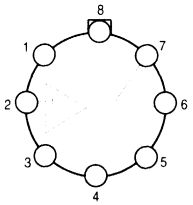
Part Number	Temperature Range	Package			
		H	N	J	D
LM111	–55, 125°C	•	•	•	•
LM211	–40, 105°C	•	•	•	•
LM311	0, 70°C	•	•	•	•

Examples : LM111H, LM111J

111-01.TBL

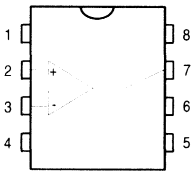
PIN CONNECTIONS (top views)

TO99



111-01.EPS

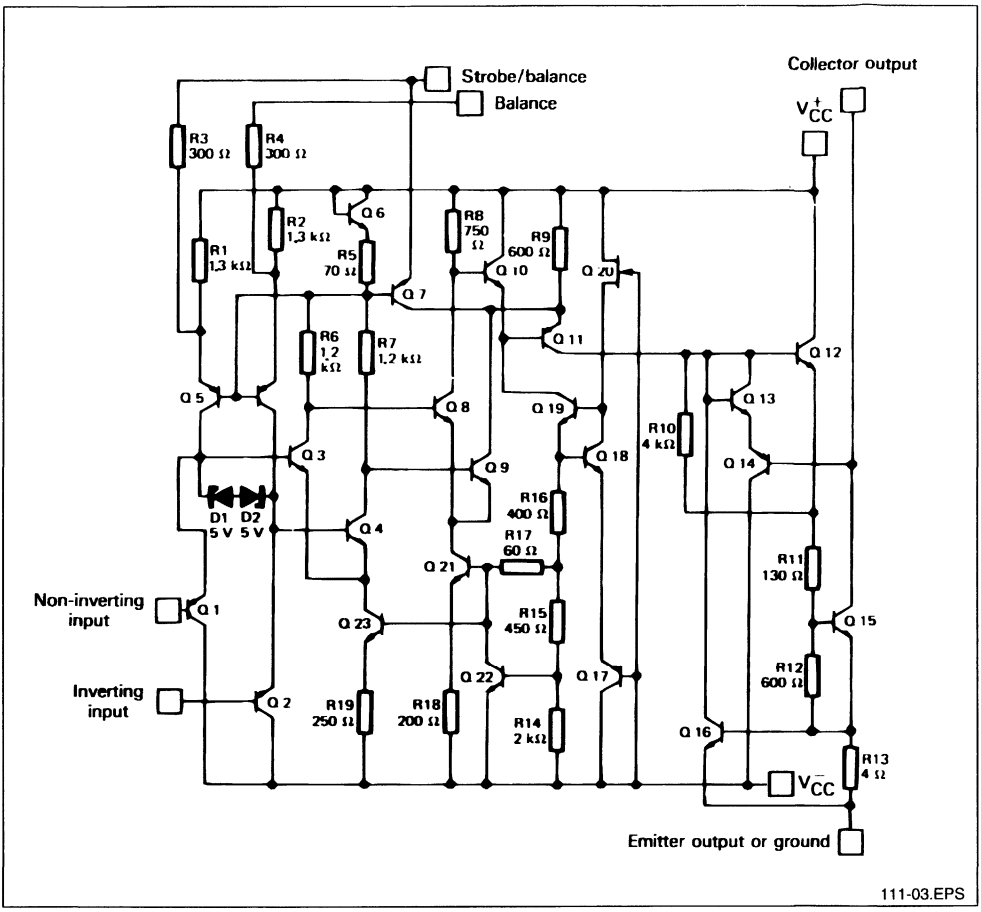
DIP8/CERDIP8
SO8



111-02.EPS

1 - Ground
2 - Non-inverting input
3 - Inverting input
4 - V_{CC}^-
5 - Balance
6 - Strobe/balance
7 - Output
8 - V_{CC}^+

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	LM111	LM211	LM311	Unit
V_{CC}	Supply Voltage	36	36	36	V
V_{id}	Differential Input Voltage	±30	±30	±30	V
V_i	Input Voltage – (note 1)	±15	±15	±15	V
P_{tot}	Power Dissipation		500		mW
T_{oper}	Operating Free-air Temperature Range	–55 to +125	–40 to +105	0 to +70	°C
T_{stg}	Storage Temperature Range	–65 to +150	–65 to +150	–65 to +150	°C
$V_{(1-4)}$	Ground to Negative Supply Voltage	30	30	30	V
$V_{(7-4)}$	Output to Negative Supply Voltage	50	50	40	V

111-02.TBL

Output short-circuit duration : 10s
Voltage at strobe pin : $V_{CC}^+ - 5V$

Maximum junction temperature
LM111 : +150°C
LM211 : +150°C
LM311 : +150°C

Note : 1. This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

ELECTRICAL CHARACTERISTICS

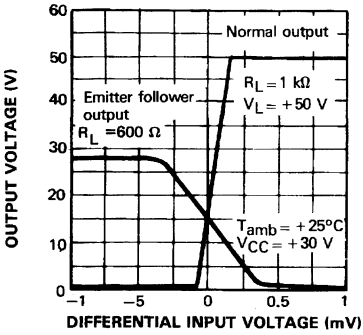
V_{CC} = ±15V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	LM111 - LM211			LM311			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage ($R_S \leq 50k\Omega$) – (note 1)							mV
	T_{amb} = +25°C		0.7	3		2	7.5	
	$T_{min.} \leq T_{amb} \leq T_{max.}$			4			10	
I_{io}	Input Offset Current – (note 1)							nA
	T_{amb} = +25°C		4	10		6	50	
	$T_{min.} \leq T_{amb} \leq T_{max.}$			20			70	
I_{ib}	Input Bias Current – (note 1)							nA
	T_{amb} = +25°C		60	100		100	250	
	$T_{min.} \leq T_{amb} \leq T_{max.}$			150			300	
A_{vd}	Large Signal Voltage Gain	40	200		40	200		V/mV
	Supply Currents							mA
I_{CC}^+	Positive		5.1	6		5.1	7.5	
I_{CC}^-	Negative		4.1	5		4.1	5	
V_{icm}	Input Common Mode Voltage Range							V
	$T_{min.} \leq T_{amb} \leq T_{max.}$	-14.5	+13.8	+13		+13.8	+13	
			-14.7		-14.5	-14.7		
V_{OL}	Low Level Output Voltage							V
	T_{amb} = +25°C, I_O = 50mA $V_i \leq$ -5mV		0.75	1.5				
	$V_i \leq$ -10mV					0.75	1.5	
	$T_{min.} \leq T_{amb} \leq T_{max.}$							
	$V_{CC}^+ \geq$ +4.5 V, V_{CC}^- = 0							
	I_{sink} = 8mA $V_i \leq$ -6mV		0.23	0.4				
	$V_i \leq$ -10mV					0.23	0.4	
I_{OH}	High Level Output Current							
	T_{amb} = +25°C $V_i \geq$ + 5mV, V_O = +35V		0.2	10				nA
	$V_i \geq$ +10mV, V_O = +5V					0.2	50	nA
	$T_{min.} \leq T_{amb} \leq T_{max.}$ $V_i \geq$ + 5mV, V_O = +35V		0.1	0.5				µA
I_{strobe}	Strobe Current		3			3		mA
t_{re}	Response Time – (note 2)		200			200		ns

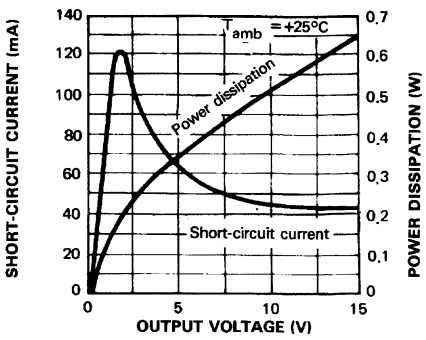
111-03.TBL

Notes : 1. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single +5V supply up to +15V supplies.
The offset voltages and offset currents given are the maximum values required to drive the output down to +1V or up to +14V with a 1mA load current. Thus, these parameters define an error band and take into account the worst-case of voltage gain and input impedance.
2. The response time specified (see definitions) is for a 100mV input step with 5mV overdrive.

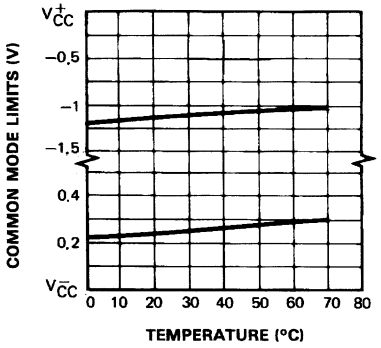
TRANSFER CHARACTERISTICS



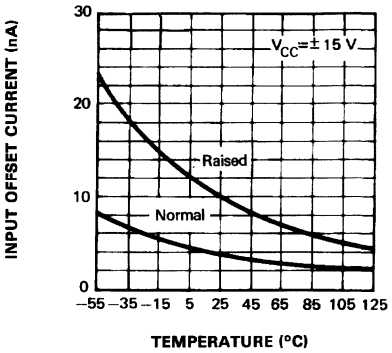
OUTPUT LIMITING CHARACTERISTICS



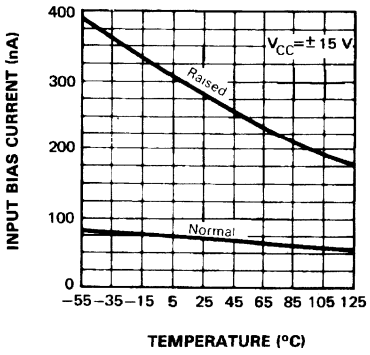
COMMON MODE LIMITS



INPUT OFFSET CURRENT

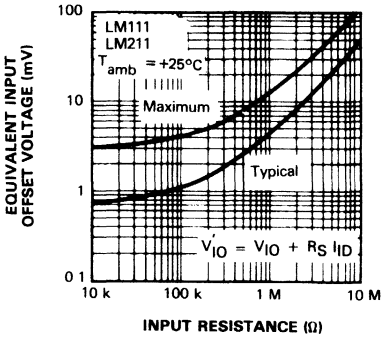


INPUT BIAS CURRENT

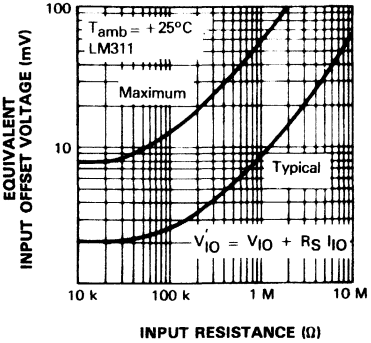


111-04.EPS

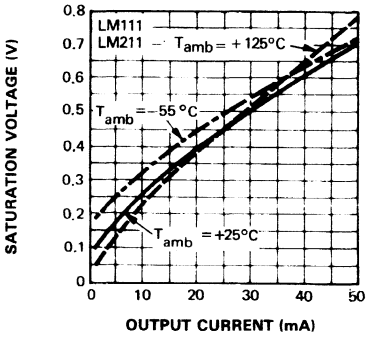
EQUIVALENT INPUT OFFSET ERROR



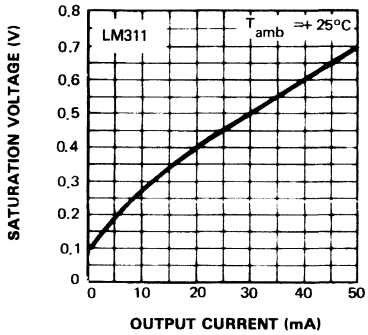
EQUIVALENT INPUT OFFSET ERROR



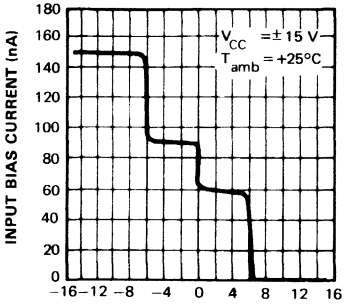
LOW LEVEL OUTPUT SATURATION VOLTAGE



LOW LEVEL OUTPUT SATURATION VOLTAGE

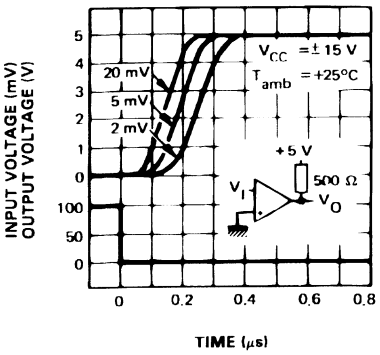


INPUT CHARACTERISTICS

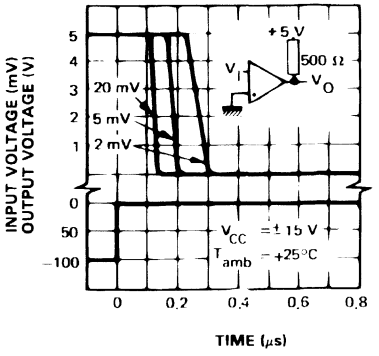


111-05.EPS

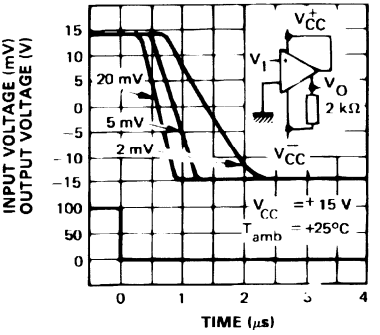
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



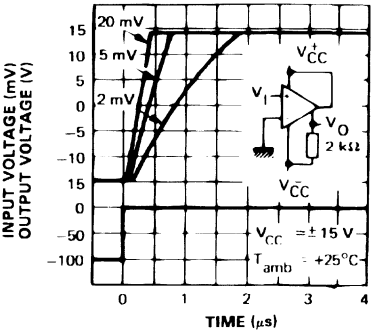
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



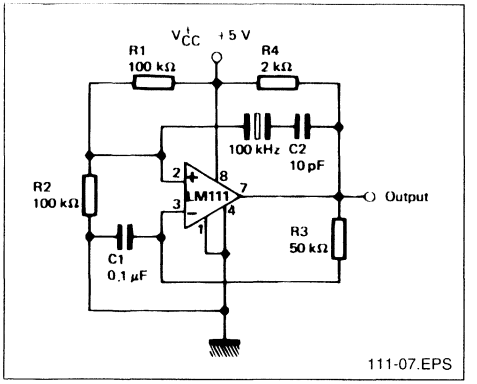
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



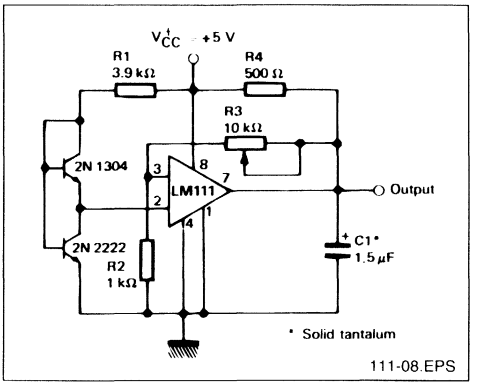
111-06.EPS

TYPICAL APPLICATIONS

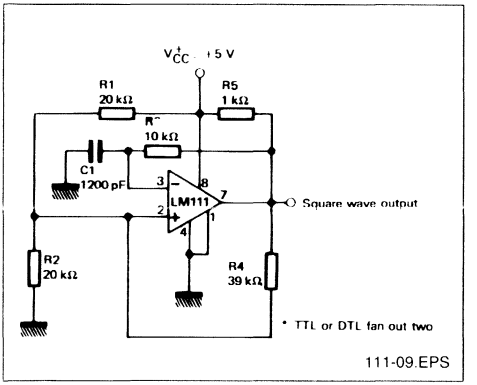
CRYSTAL OSCILLATOR



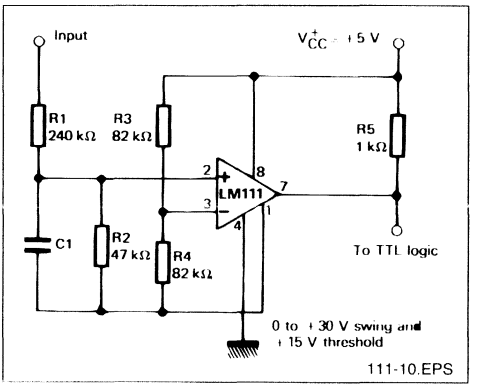
LOW VOLTAGE ADJUSTABLE REFERENCE SUPPLY



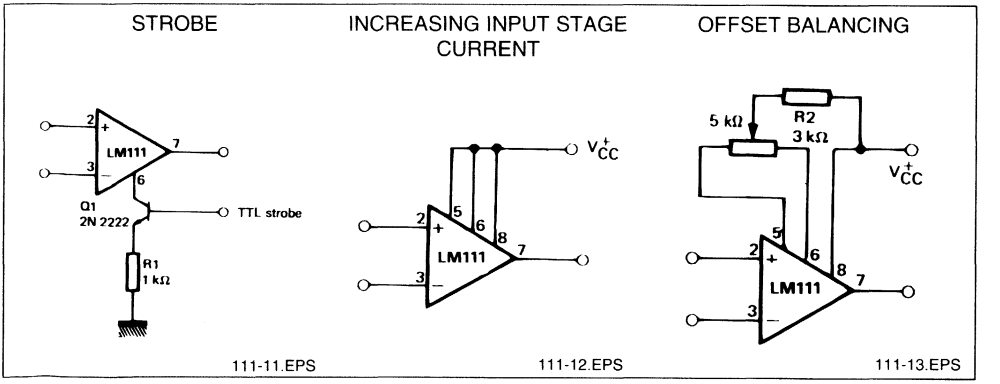
100KHz FREE RUNNING MULTIVIBRATOR



TTL INTERFACE WITH HIGH LEVEL LOGIC



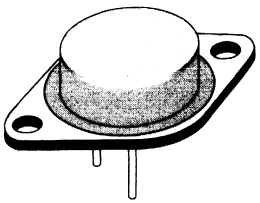
AUXILIARY CIRCUITS



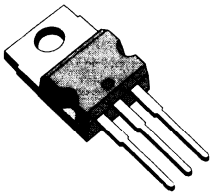
1.2V TO 37V ADJUSTABLE VOLTAGE REGULATOR

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST/1)

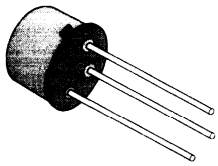
- OUTPUT VOLTAGE RANGE : 1.2 TO 37V
- OUTPUT CURRENT IN EXCESS OF 1.5A (0.5A for TO-39)
- 0.1% LINE AND LOAD REGULATION
- FLOATING OPERATION FOR HIGH VOLTAGES
- COMPLETE SERIES OF PROTECTIONS : CURRENT LIMITING, THERMAL SHUTDOWN AND SOA CONTROL



TO-3



TO-220



TO-39

DESCRIPTION

The LM117/LM217/LM317 are monolithic integrated circuit in TO-220 and TO-3 packages intended for use as positive adjustable voltage regulators.

They are designed to supply more than 1.5A of load current with an output voltage adjustable over a 1.2 to 37V range.

The nominal output voltage is selected by means of only a resistive divider, making the device exceptionally easy to use and eliminating the stocking of many fixed regulators.

ABSOLUTE MAXIMUM RATING

Symbol	Parameter		Value	Unit
V_{i-o}	Input-output Differential Voltage		40	V
I_O	Output Current		Intenrally Limited	
T_{op}	Operating Junction Temperature for:	LM117	-55 to 150	°C
		LM217	-25 to 150	°C
		LM317	0 to 125	°C
P_{tot}	Power Dissipation		Internally Limited	

THERMAL DATA

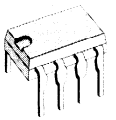
			TO-3	TO-220	ISOWATT220	TO-39	
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	4	3	4	15	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	35	50	60	160	°C/W

SGS-THOMSON MICROELECTRONICS

LM118-LM218 LM318

SINGLE OPERATIONAL AMPLIFIERS

- INPUT OFFSET VOLTAGE : 4 mV max. LM118 – LM218 10 mV max. LM318
- INPUT BIAS CURRENT : 250nA max.
- INPUT OFFSET CURRENT : 50nA max.
- SLEW RATE OF 150 V/µs AS INVERTING AMPLIFIER



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

J
CERDIP8
(Cerdip Package)

H
TO99
(Metal Can)

DESCRIPTION

The LM118, LM218 and LM318 are precision high speed operational amplifiers designed for applications requiring wide bandwidth and high slew rate. They feature internal frequency compensation and a factor of ten increase in speed over general purpose devices.

Although, no external frequency compensation components are needed for operation, feedforward compensation may be used to further increase the speed. For inverting applications, feedforward compensation will boost the slew rate to over 150 V/µs and almost double the bandwidth. However, for non-inverting or differential applications feedforward cannot be used.

The high speed and fast settling time of these op amps make them useful in A/D converters, oscillators, active filters, sample and hold circuits, or general purpose amplifiers.

ORDER CODES

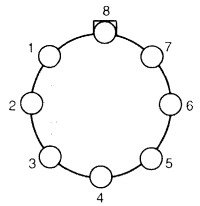
Part Number	Temperature Range	Package			
		H	N	J	D
LM118	–55, + 125°C	•	•	•	•
LM218	–40, + 105°C	•	•	•	•
LM318	0, + 70°C	•	•	•	•

Examples : LM118J, LM218H

118-01.TBL

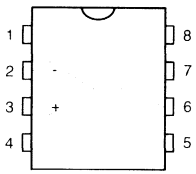
PIN CONNECTIONS (top views)

TO99



118-01.EPS

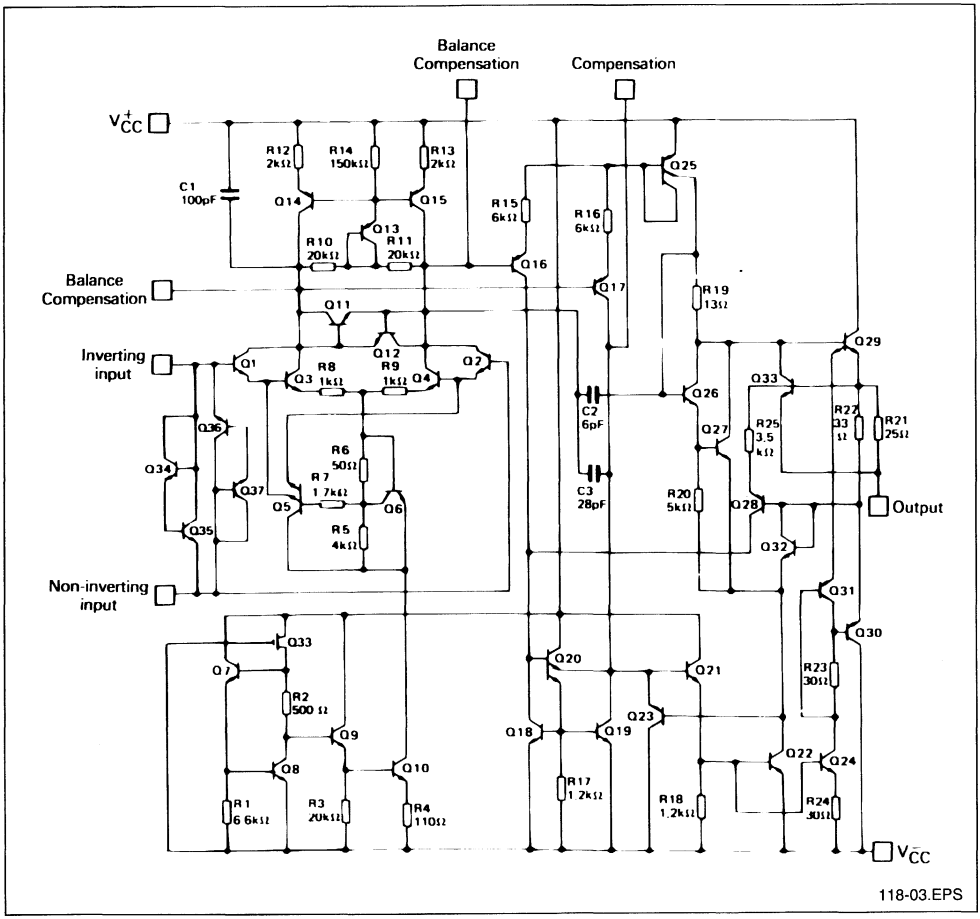
DIP8/CERDIP8
SO8



118-02.EPS

1 - Balance/Compensation 1
2 - Inverting input
3 - Non-inverting input
4 - V_{CC}^-
5 - Balance/Compensation 3
6 - Output
7 - V_{CC}^+
8 - Compensation 2

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	LM118	LM218	LM318	Unit
V_{CC}	Supply Voltage	±20	±20	±20	V
V_i	Input Voltage - (note 1)	±15	±15	±15	V
I_{id}	Differential Input Current - (note 2)	±10	±10	±10	mA
	Output Short-circuit Duration	Infinite			
P_{tot}	Power Dissipation LM318D All other Versions	500	500	300 500	mW
T_{oper}	Operating Free-air Temperature Range	−55 to +125	−40 to +105	0 to +70	°C
T_{stg}	Storage Temperature Range	−65 to +150	−65 to +150	−65 to +150	°C

Notes : 1. For supply voltage less than ±15V, the absolute maximum input voltage is equal to the supply voltage
2. The inputs are shunted with shunt diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

ELECTRICAL CHARACTERISTICS

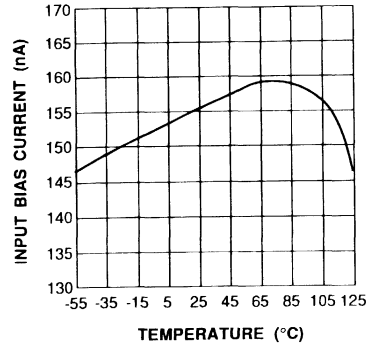
$\pm 5V \leq V_{CC} \leq \pm 20V$, $C_1 = 30pF$, $T_{amb} = 25^oC$(unless otherwise specified)

Symbol	Parameter	LM118 - LM218			LM318			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage ($R_S \leq 10k\Omega$) $T_{amb} = 25^oC$ $T_{min.} \leq T_{amb} \leq T_{max.}$		2	4 6		2	10 15	mV
I_{ib}	Input Bias Current $T_{amb} = 25^oC$ $T_{min.} \leq T_{amb} \leq T_{max.}$		160	250 500		160	500 750	nA
I_{io}	Input Offset Current $T_{amb} = 25^oC$ $T_{min} \leq T_{amb} \leq T_{max}$		6	50 100		6	200 300	nA
A_{vd}	Large Signal Voltage Gain ($V_{CC} = \pm 15V$, $V_O = \pm 10V$, $R_L = 2k\Omega$) $T_{amb} = 25^oC$ $T_{min.} \leq T_{amb} \leq T_{max.}$	50 25	200		25 20	200		V/mV
SVR	Supply Voltage Rejection Ratio ($R_S \leq 10k\Omega$) $T_{amb} = 25^oC$ $T_{min.} \leq T_{amb} \leq T_{max.}$	70 70	97		65 65	97		dB
I_{CC}	Supply Current, no Load $T_{amb} = 25^oC$ $T_{min} \leq T_{amb} \leq T_{max}$		5	8 15		5	10 15	mA
V_i	Input Voltage Range ($V_{CC} = \pm 15V$) $T_{amb} = 25^oC$ $T_{min.} \leq T_{amb} \leq T_{max.}$	-11.5 - 11.5		11.5 11.5	-11.5 - 11.5		11.5 11.5	V
CMR	Common Mode rejection Ratio ($R_S \leq 10k\Omega$) $T_{amb} = 25^oC$ $T_{min.} \leq T_{amb} \leq T_{max.}$	80 80	105		70 70	105		dB
I_{os}	Output Short-circuit Current ($V_{CC} = \pm 15V$) $T_{amb} = 25^oC$	10	30	60	10	30	60	mA
$\pm V_{OPP}$	Output Voltage Swing ($V_{CC} = \pm 15V$, $R_L = 2k\Omega$) $T_{amb} = 25^oC$ $T_{min.} \leq T_{amb} \leq T_{max.}$	±12 ±12	±13		±12 ±12	±13		V
SR	Slew Rate ($V_{CC} = \pm 15V$, $V_i = \pm 10V$, $R_L = 2k\Omega$, $C_L = 100pF$, $T_{amb} = 25^oC$, unity gain) - (note 3)	50	70		50	70		V/µs
R_i	Input Impedance	1	3		1	3		MΩ
GBP	Gain Bandwidth Product ($V_{CC} = \pm 15V$, $V_i = 10mV$, $R_L = 2k\Omega$, $C_L = 100pF$, f = 100kHz)		15			15		MHz
THD	Total Harmonic Distortion ($V_{CC} = \pm 15V$, f = 1kHz, $A_V = 20dB$, $R_L = 2k\Omega$, $V_O = 2V_{PP}$, $C_L = 100$ pF)		0.008			0.008		%
e_n	Equivalent Input Noise Voltage ($V_{CC} = \pm 15V$, f = 1kHz, $R_s = 100\Omega$)		17			17		$\frac{nV}{\sqrt{Hz}}$

118-03.TBL

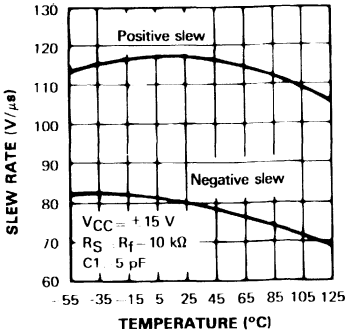
Note : 3. May be improved up to 150V/µs in inverting amplifier configuration (see basic diagrams).

IIB (nA) **INPUT BIAS CURRENT**



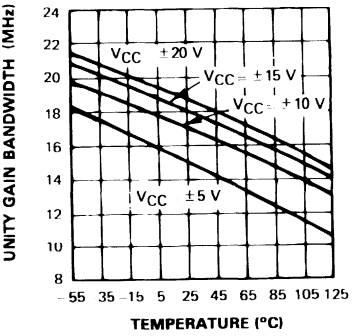
118-04.EPS

VOLTAGE FOLLOWER SLEW RATE (Note 5)



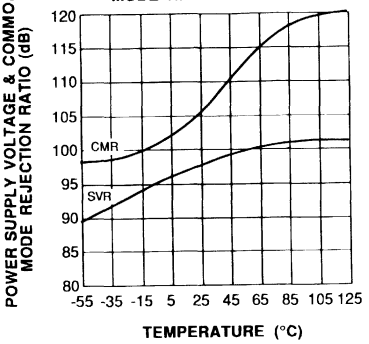
118-05.EPS

UNITY GAIN BANDWIDTH (GAIN : 1) (Note 5)



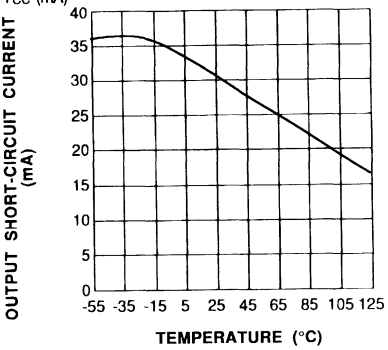
118-06.EPS

POWER SUPPLY VOLTAGE & COMMON MODE REJECTION RATIO



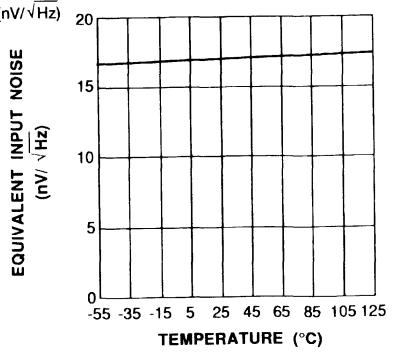
118-07.EPS

ICC (mA) **OUTPUT SHORT-CIRCUIT CURRENT**



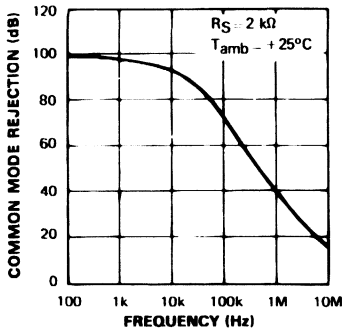
118-08.EPS

NOISE (nV/√Hz) **EQUIVALENT INPUT NOISE**



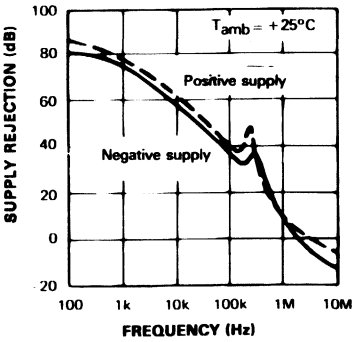
118-09.EPS

COMMON MODE REJECTION



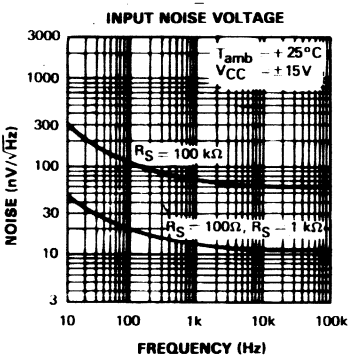
118-10.EPS

POWER SUPPLY REJECTION



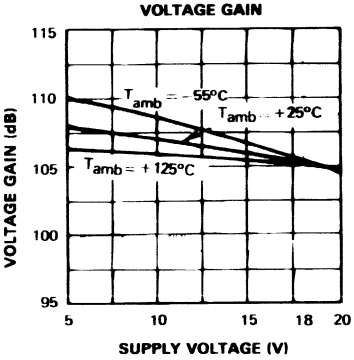
118-11.EPS

INPUT NOISE VOLTAGE



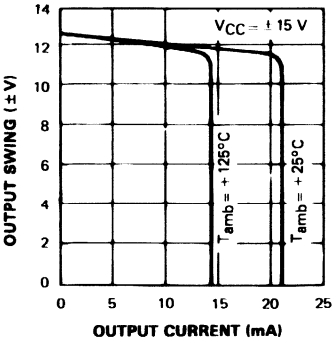
118-12.EPS

VOLTAGE GAIN



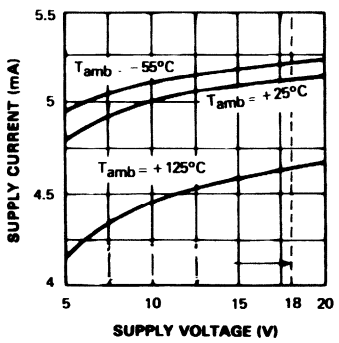
118-13.EPS

CURRENT LIMITING



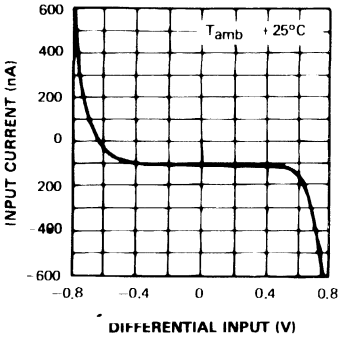
118-14.EPS

SUPPLY CURRENT



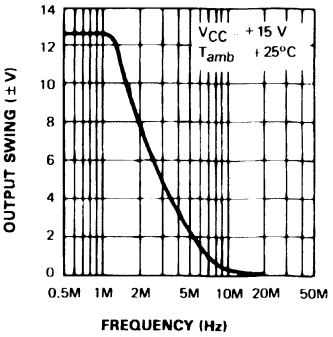
118-15.EPS

INPUT CURRENT



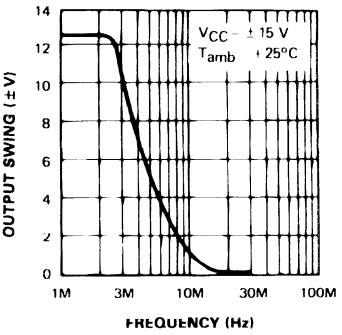
118-16.EPS

LARGE SIGNAL FREQUENCY RESPONSE



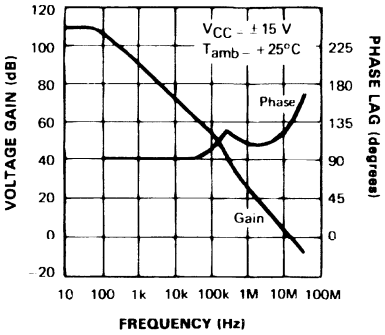
118-17.EPS

LARGE SIGNAL FREQUENCY RESPONSE*



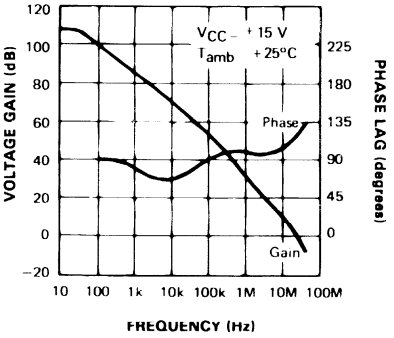
118-18.EPS

OPEN LOOP FREQUENCY RESPONSE



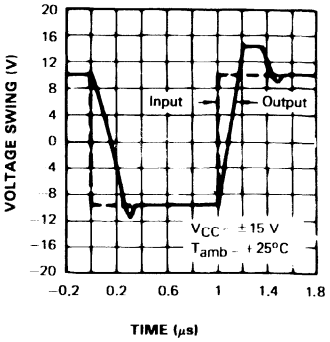
118-19.EPS

OPEN LOOP FREQUENCY RESPONSE*

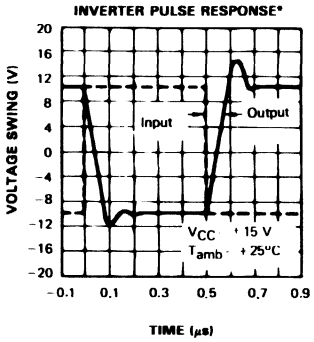


118-20.EPS

VOLTAGE FOLLOWER PULSE RESPONSE

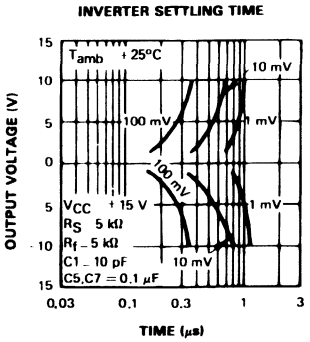


118-21.EPS



* With feedforward compensation

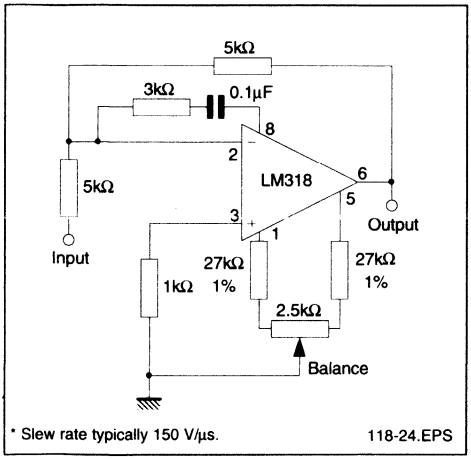
118-22.EPS



118-23.EPS

BASIC DIAGRAMS

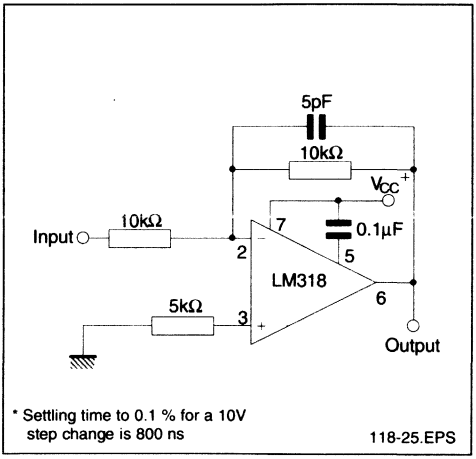
FEEDFORWARD COMPENSATION FOR GREATER INVERTING SLEW RATE*



* Slew rate typically 150 V/μs.

118-24.EPS

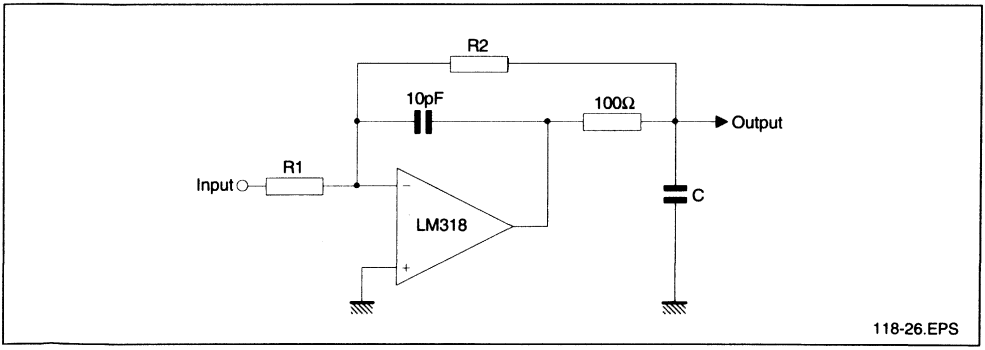
COMPENSATION FOR MINIMUM SETTLING TIME*



* Settling time to 0.1 % for a 10V step change is 800 ns

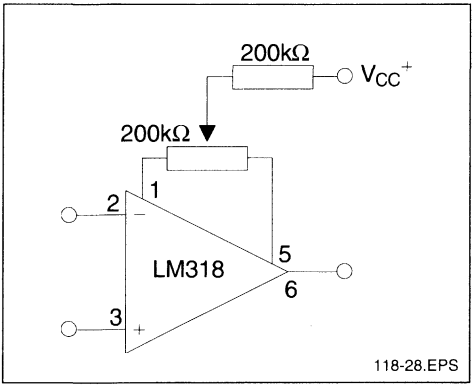
118-25.EPS

ISOLATING LARGE CAPACITIVE LOADS

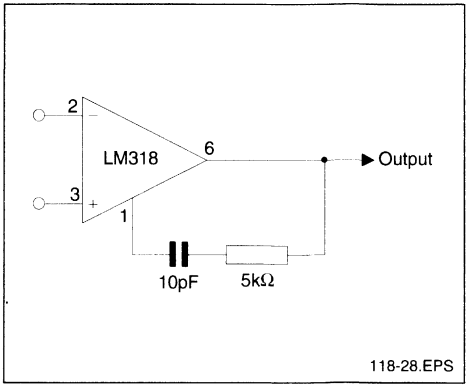


118-26.EPS

OFFSET BALANCING

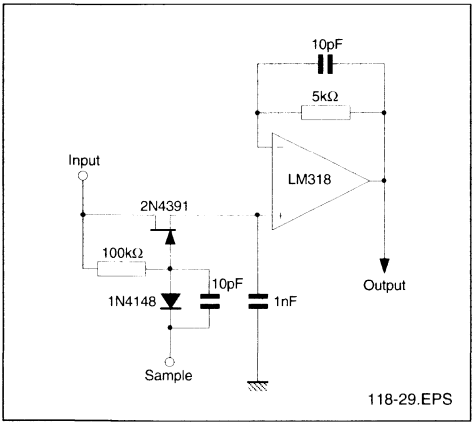


OVERCOMPENSATION

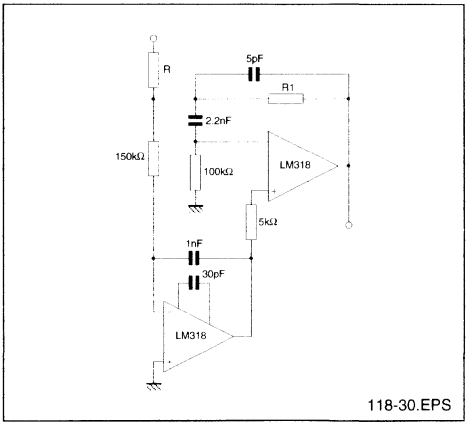


TYPICAL APPLICATION DIAGRAM

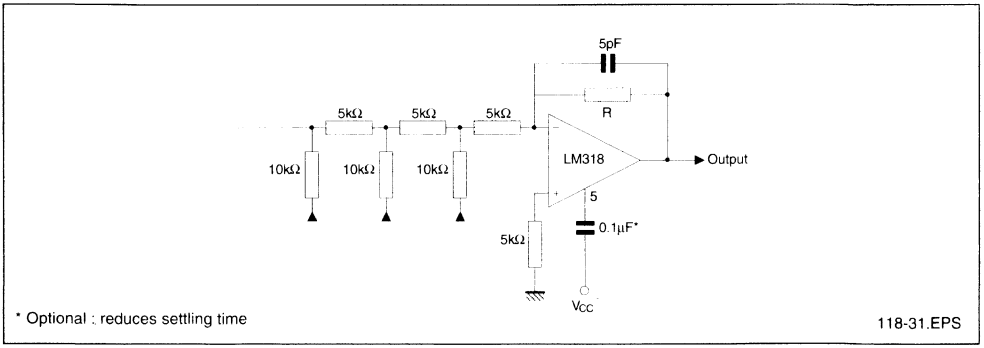
FAST SAMPLE AND HOLD



FAST SUMMING AMPLIFIER WITH LOW INPUT CURRENT



D/A CONVERTER USING LADDER NETWORK

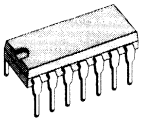


SGS-THOMSON MICROELECTRONICS

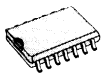
LM119 - LM219 LM319

HIGH SPEED DUAL COMPARATORS

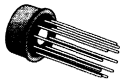
- TWO INDEPENDENT COMPARATORS
- OPERATES FROM A SINGLE +5V SUPPLY
- TYPICALLY 80ns RESPONSE TIME AT ±15V
- MINIMUM FAN-OUT OF 2 EACH SIDE
- MAXIMUM INPUT CURRENT OF 1μA OVER OPERATING TEMPERATURE RANGE
- INPUTS AND OUTPUTS CAN BE ISOLATED FROM SYSTEM GROUND
- HIGH COMMON-MODE SLEW RATE



N
DIP4
(Plastic Package)
J
CERDIP14
(Cerdip Package)



D
SO14
(Plastic Micropackage)



H
TO100
(Metal Can)

DESCRIPTION

These products are precision high speed dual comparators designed to operate over a wide range of supply voltages down to a single 5V logic supply and ground and have low input currents and high gains.

The open collector of the output stage makes compatible with TTL as well as capable of driving lamps and relays at currents up to 25mA.

Although designed primarily for applications requiring operation from digital logic supplies, are fully specified for power supplies up to ±15V.

They feature faster response than the LM111 at the expense of higher power dissipation. However, the high speed, wide operating voltage range and low package count make the much more versatile.

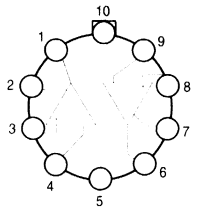
ORDER CODES

Part Number	Temperature Range	Package			
		H	N	J	D
LM119	–55, +125°C	•	•	•	•
LM219	–40, +105°C	•	•	•	•
LM319	0, +70°C	•	•	•	•
Examples : LM119H, LM219N					

119-01.TBL

PIN CONNECTIONS (top views)

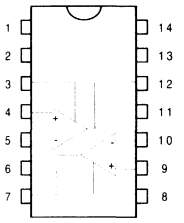
TO100



119-01.EPS

1 - Output 1
2 - Ground 1
3 - Non-inverting input 1
4 - Inverting inpu t1
5 - V_{CC}^-
6 - Output 2
7 - Ground 2
8 - Non-inverting input 2
9 - Inverting input 2
10 - V_{CC}^+

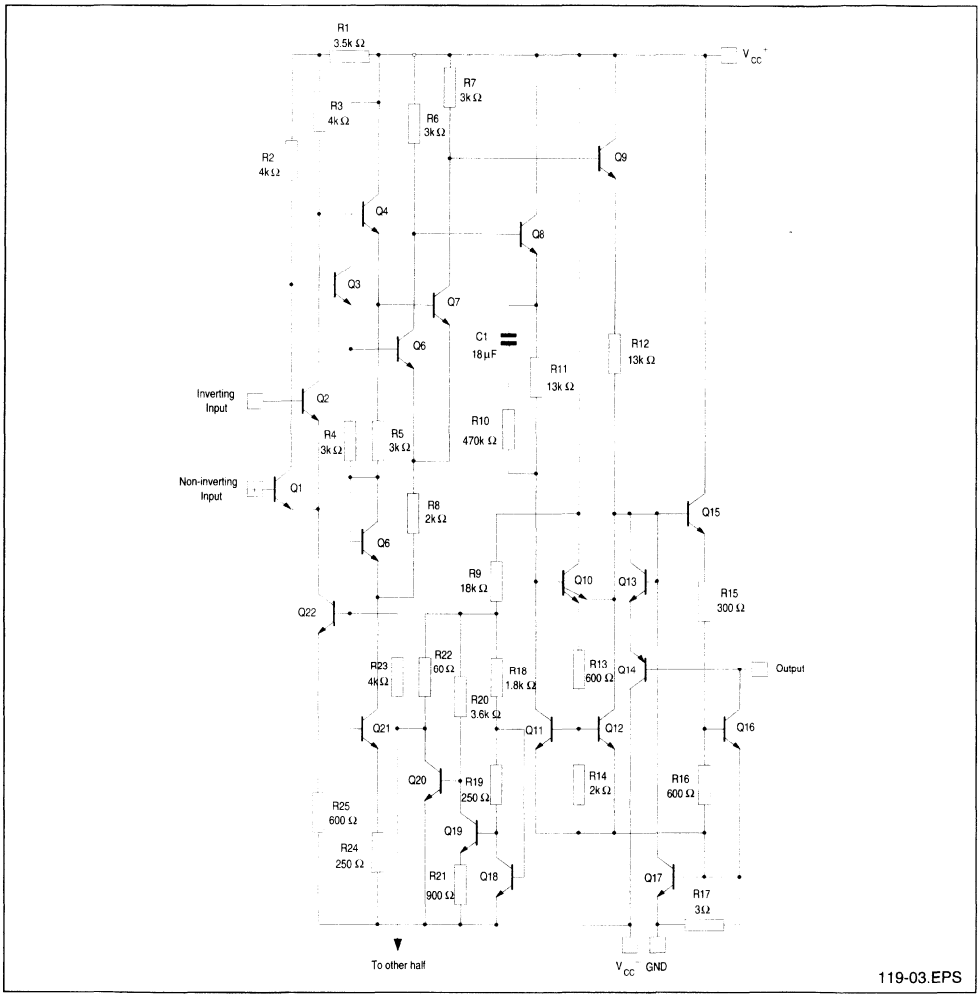
DIP14/CERDIP14
SO14



119-02.EPS

1 - N.C.
2 - N.C.
3 - Ground 1
4 - Non-inverting input 1
5 - Inverting input 1
6 - V_{CC}^-
7 - Output 2
8 - Ground 2
9 - Non-inverting input 2
10 - Inverting input 2
11 - V_{CC}^+
12 - Output 1
13 - N.C.
14 - N.C.

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	LM119	LM219	LM319	Unit
$V_O - V_{CC}^-$	Output to Negative Supply Voltage	36	36	36	V
V_{CC}^-	Negative Supply Voltage	25	25	25	V
V_{CC}^+	Positive Supply Voltage	18	18	18	V
V_{id}	Differential Input Voltage	±5	±5	±5	V
V_i	Input Voltage – (note 1)	±15	±15	±15	V
P_{tot}	Power Dissipation	500	500	500	mW
T_{oper}	Operating Free-air Temperature Range	–55 to +125	–40 to +105	0 to +70	°C
T_{stg}	Storage Temperature Range	–65 to +150	–65 to +150	–65 to +150	°C

119-03.TBL

ELECTRICAL CHARACTERISTICS

V_{CC} = ±15V, T_{amb} = 25°C(unless otherwise specified)

Symbol	Parameter	LM119 - LM219			LM319			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage ($R_S \leq 5k\Omega$) – (note 2) T_{amb} = +25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		0.7	4 7		2	8 10	mV
I_{io}	Input Offset Current – (note 2) T_{amb} = +25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		30	75 100		80	200 300	nA
I_{ib}	Input Bias Current – (note 2) T_{amb} = +25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		150	500 1000		250	1000 1200	nA
A_{vd}	Large Signal Voltage Gain	10	40		8	40		V/mV
I_{CC}^+	Positive Supply Current V_{CC} = ±15V V_{CC}^+ = +5V, V_{CC}^- = 0V		8 4.3	11.5		8 4.3	12.5	mA
I_{CC}^-	Negative Supply Current		3	4.5		3	5	mA
V_{icm}	Input Common Mode Voltage Range V_{CC} = ±15V V_{CC}^+ = +5V, V_{CC}^- = 0V	±12 1	±13	 3	±12 1	±13	 3	V
V_{id}	Differential Input Voltage			±5			±5	V
V_{OL}	Low Level Output Voltage T_{amb} = +25°C, I_O = 25mA $V_i \leq -5mV$ $V_i \leq -10mV$ $T_{min.} \leq T_{amb} \leq T_{max.}$ $V_{CC}^+ \geq +4.5V$, V_{CC}^- = 0V, $I_{O(sink)} < 3.2mA$ $V_i \leq -6mV$ $V_i \leq -10mV$		 0.75 0.23	 1.5 0.4		 0.75 0.3	 1.5 0.4	V
I_{OH}	High Level Output Current (V_O = +35V) T_{amb} = +25°C $V_i \geq$ 5mV $V_i \geq$ 10mV $T_{min.} \leq T_{amb} \leq T_{max.}$ $V_i \geq$ 5mV		0.2 1	2 10		 0.2 	 10 	µA
t_{re}	Response Time – (note 3)		80			80		ns

119-03.TBL

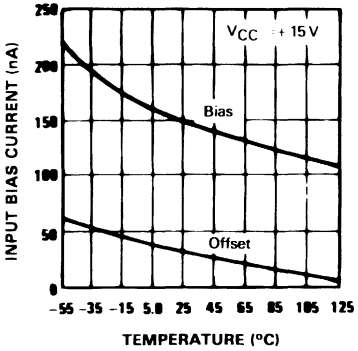
Notes : 1. For supply voltages less than ±15V the absolute maximum input voltage is equal to the supply voltage.

2. These specifications apply for V_{CC} = ±15V, unless otherwise stated. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single +5V supply up to ±15V supplies. The offset voltages and offset current given are the maximum values required to drive the output down to 1V or up to +14V with a 1mA load current.
Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

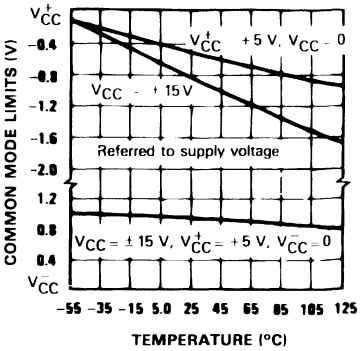
3. The response time specified is for a 100mV input step with 5mV overdrive.

LM119-LM219

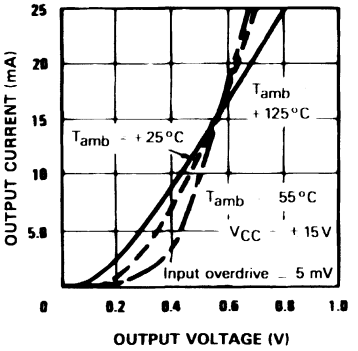
INPUT BIAS CURRENTS



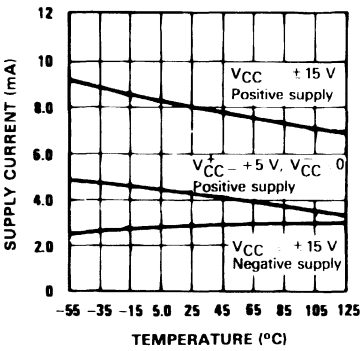
COMMON MODE LIMITS



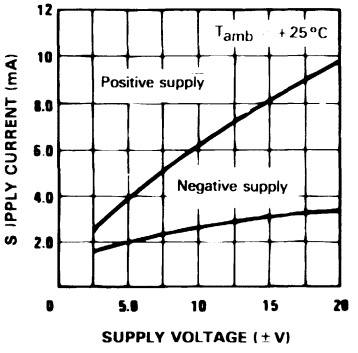
OUTPUT SATURATION VOLTAGE



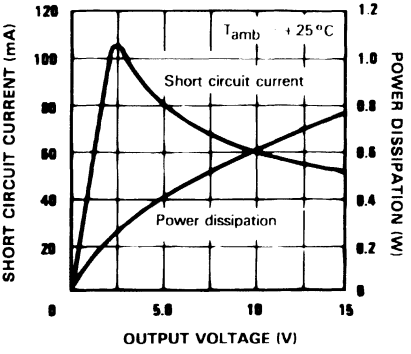
SUPPLY CURRENT



SUPPLY CURRENT



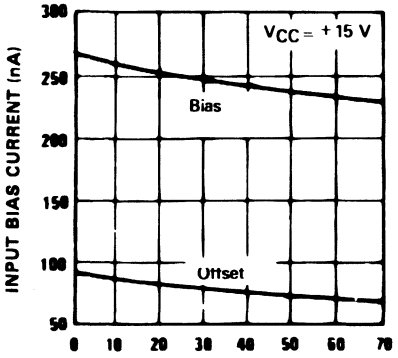
OUTPUT LIMITING CHARACTERISTICS



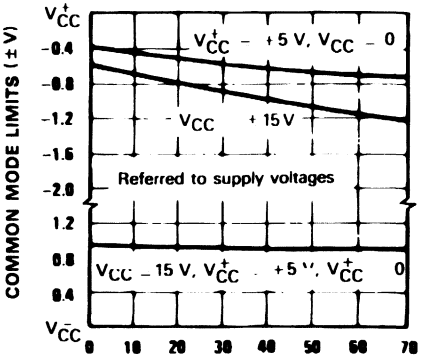
119-04.EPS

LM319

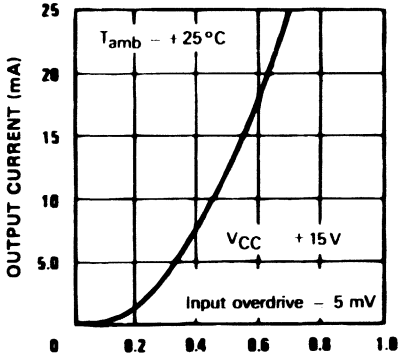
INPUT BIAS CURRENTS



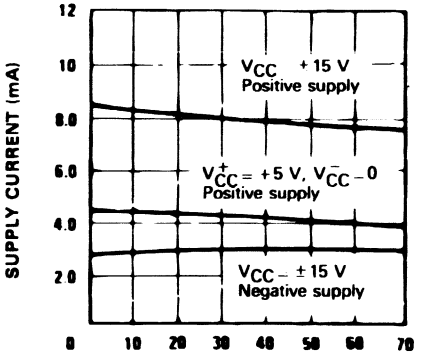
COMMON MODE LIMITS



OUTPUT SATURATION VOLTAGE

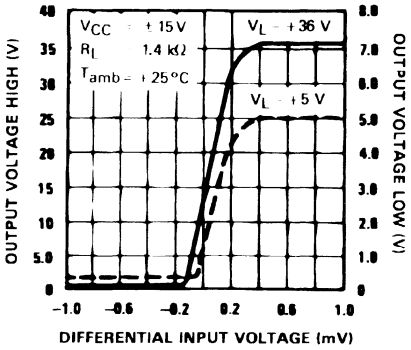


SUPPLY CURRENT

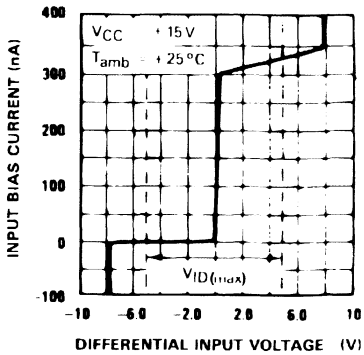


119-05.EPS

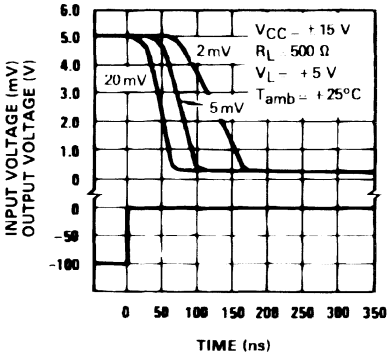
TRANSFER FUNCTION



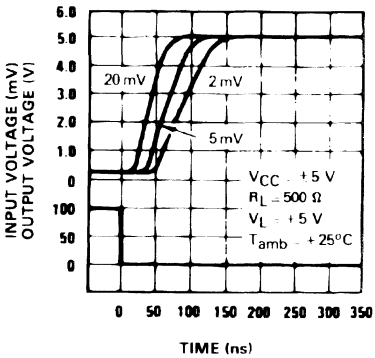
INPUT CHARACTERISTICS



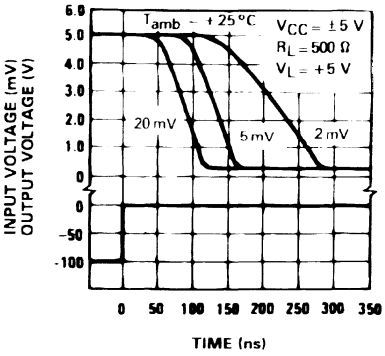
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



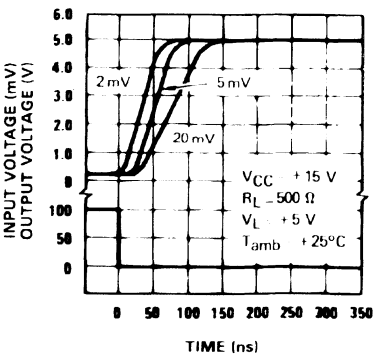
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



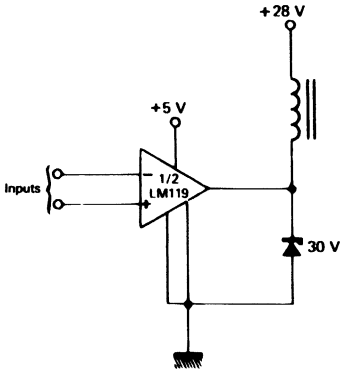
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



119-06.EPS

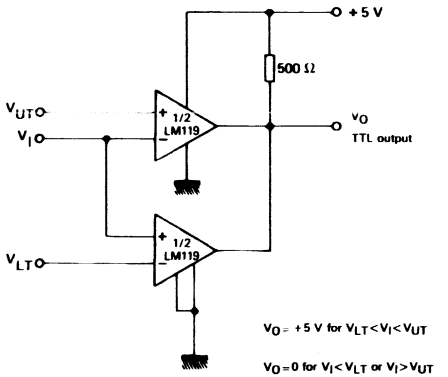
TYPICAL APPLICATION DIAGRAMS

RELAY DRIVER



119-07.EPS

WINDOW DETECTOR

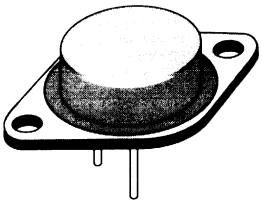


119-08.EPS

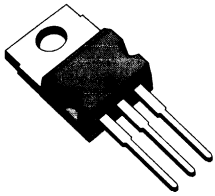
THREE-TERMINAL 3A-5V POSITIVE VOLTAGE REGULATORS

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST/1)

- OUTPUT CURRENT : 3A
- INTERNAL CURRENT AND THERMAL LIMITING
- TYPICAL OUPUT IMPEDANCE : 0.01Ω
- MINIMUM INPUT VOLTAGE : 7.5V
- POWER DISSIPATION : 30W



TO-3



TO-220

DESCRIPTION

The LM123, LM223, LM323 are three-terminal positive voltage regulators with a preset 5V output and a load driving capability of 3A. New circuit design and processing techniques are used to provide the high output current without sacrificing the regulation characteristics of lower current devices.

The 3A regulator is virtually blowout proof.

Current limiting, power limiting and thermal shutdown provide the same high level of reliability obtained with these techniques in the LM209, 1A regulator.

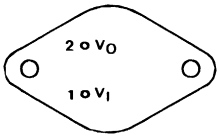
An overall worst case specification for the combined effects of input voltage, load current, ambient temperature, and power dissipation ensure that the LM123, LM223, LM323 will perform satisfactorily as a system element.

ORDER CODES

Part Number	Temperature Range	Package	
		K	T
LM123	-55 °C to 150 °C	•	
LM223	-25 °C to 150 °C	•	
LM323	0 °C to 125 °C	•	•

PIN CONNECTION

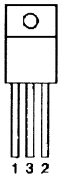
TO-3
(bottom view)



Case is ground

1 - Input
2 - Output

TO-220
(front view)

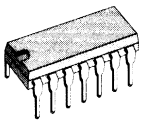


1 - Input
2 - Output
3 - GND

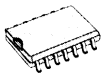
LM124/A - LM224/A LM324/A - LM2902

LOW POWER QUAD OPERATIONAL AMPLIFIERS

- LARGE VOLTAGE GAIN : 100dB
- VERY LOW SUPPLY CURRENT/AMPLI : 375µA
- LOW INPUT BIAS CURRENT : 20nA
- LOW INPUT OFFSET VOLTAGE : 2mV
- LOW INPUT OFFSET CURRENT : 2nA
- WIDE POWER SUPPLY RANGE :
  SINGLE SUPPLY : +3V TO +30V
  DUAL SUPPLIES : ±1.5V TO ±15V



N
DIP14
(Plastic Package)
J
CERDIP14
(Cerdip Package)



D
SO14
(Plastic Micropackage)

DESCRIPTION

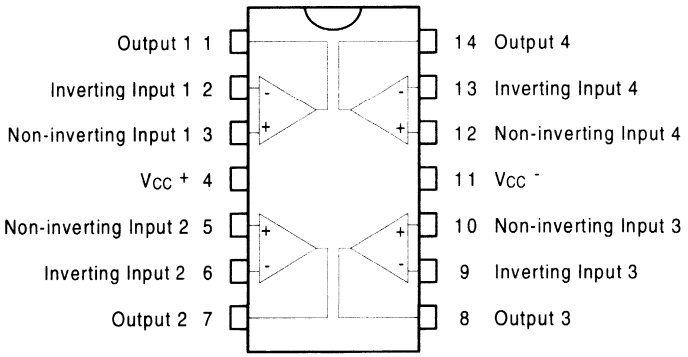
These circuits consist of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically for automotive and industrial control systems. They operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

ORDER CODES

Part Number	Temperature Range	Package		
		N	J	D
LM124/A	– 55°C, +125°C	•	•	•
LM224/A	–40°C, +105°C	•	•	•
LM324/A	0°C, +70°C	•	•	•
LM2902	–40°C, +105°C	•	•	•
Examples : LM124J, LM224N				

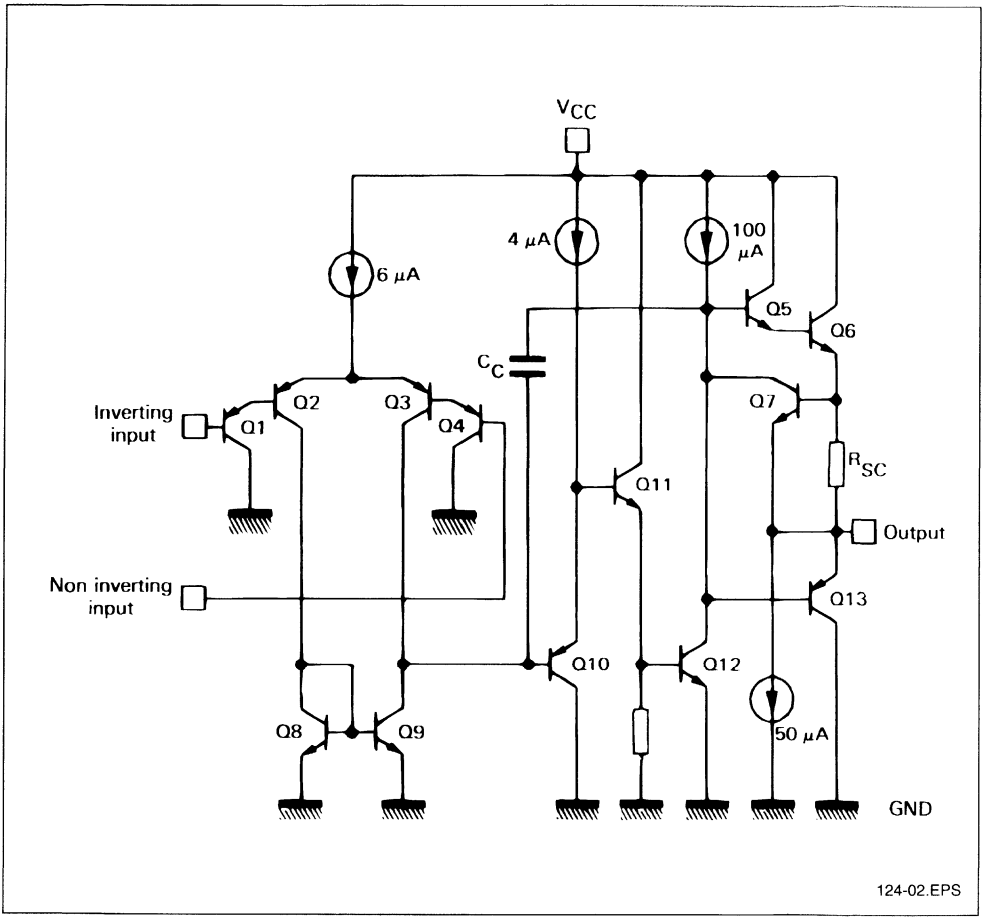
124-01.TBL

PIN CONNECTIONS (top view)



124-01.EPS

SCHEMATIC DIAGRAM (1/4 LM124)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	LM124,A	LM224,A 2902	LM324,A	Unit
V_{cc}	Supply Voltage		±16 or 32		V
V_i	Input Voltage		–0.3 to +32		V
V_{id}	Differential Input Voltage	+32	+32	+32	V
P_{tot}	Power Dissipation N, J Suffix D Suffix	500 -	500 400	500 400	mW
-	Output Short-circuit Duration - (note 1)		Infinite		
I_{in}	Input Current – (note 6)	50	50	50	mA
T_{oper}	Operating Free Air Temperature Range	–55 to +125	–40 to +105	0 to +70	°C
T_{stg}	Storage Temperature Range	–65 to 150	–65 to 150	–65 to 150	°C

ELECTRICAL CHARACTERISTICS

V_{CC}^+ = +5V, V_{CC}^- = Ground, V_O = 1.4V, T_{amb} = +25°C
(unless otherwise specified)

Symbol	Parameter	LM124A - LM224A LM324A			LM124 - LM224 LM324 - LM2902			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage (note 3) T_{amb} = +25°C LM324, LM2902 $T_{min.} \le T_{amb} \le T_{max.}$ LM324, LM2902		2	3 5		2	5 7 7 9	mV
I_{io}	Input Offset Current T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$		2	20 40		2	30 40	nA
I_{ib}	Input Bias Current (note 2) T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$		20	100 200		20	150 200	nA
A_{vd}	Large Signal Voltage Gain (V_{CC}^+ = +15V, R_L = 2kΩ, V_O = 1.4V to 11.4V) T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$	50 25	100		50 25	100		V/mV
SVR	Supply Voltage Rejection Ratio ($R_S \le 10k\Omega$) (V_{CC}^+ = 5V to 30V) T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$	65 65	110		65 65	110		dB
I_{CC}	Supply Current, all Amp, no load T_{amb} = +25°C V_{CC} = +5V V_{CC} = +30V $T_{min.} \le T_{amb} \le T_{max.}$ V_{CC} = +5V V_{CC} = +30V		0.7 1.5 0.8 1.5	1.2 3 1.2 3		0.7 1.5 0.8 1.5	1.2 3 1.2 3	mA
V_{icm}	Input Common Mode Voltage Range (V_{CC} = +30V) - (note 4) T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$	0 0		V_{CC} -1.5 V_{CC} -2	0 0		V_{CC} -1.5 V_{CC} -2	V
CMR	Common-mode Rejection Ratio ($R_S \le 10k\Omega$) T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max}$	70 60	80		70 60	80		dB
I_o	Output Short-circuit Current (V_{id} = +1V) V_{CC} = +15V, V_o = +2V	20	40	60	20	40	60	mA
I_{sink}	Output Sink Current (V_{id} = -1V) V_{CC} = +15V, V_o = +2V V_{CC} = +15V, V_o = +0.2V	10 12	20 50		10 12	20 50		mA µA

124-03.TBL

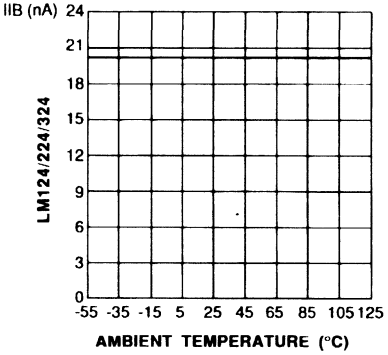
ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	LM124A - LM224A LM324A			LM124 - LM224 LM324 - LM 2902			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OH}	High Level Output Voltage (V_{CC} = +30V)							V
	T_{amb} = +25°C R_L = 2kΩ	26	27		26	27		
	$T_{min.} \le T_{amb} \le T_{max.}$	26			26			
	T_{amb} = +25°C R_L = 10kΩ	27	28		27	28		
	$T_{min.} \le T_{amb} \le T_{max.}$	27			27			
	(V_{CC} = +5V, R_L = 2kΩ)							
	T_{amb} = +25°C	3.5			3.5			
	$T_{min.} \le T_{amb} \le T_{max.}$	3			3			
V_{OL}	Low Level Output Voltage (R_L = 10kΩ)							mV
	T_{amb} = +25°C		5	20		5	20	
	$T_{min.} \le T_{amb} \le T_{max.}$			20			20	
SR	Slew Rate (V_{CC} = 15V, V_I = 0.5 to 3V, R_L = 2kΩ, C_L = 100pF, T_{amb} = +25°C, unity gain)	0.2	0.4		0.2	0.4		V/µs
GBP	Gain Bandwidth Product (V_{CC} = 30V f = 100kHz, T_{amb} = +25°C, V_{in} = 10mV R_L = 2kΩ, C_L = 100pF)	0.7	1.3		0.7	1.3		MHz
THD	Total Harmonic Distortion (f = 1kHz, A_V = 20dB, R_L = 2kΩ, V_O = $2V_{pp}$ C_L = 100pF, T_{amb} = +25°C, V_{CC} = 30V)		0.015			0.015		%
e_n	Equivalent Input Noise Voltage (f = 1kHz, R_s = 100Ω, V_{CC} = 30V)		40			40		$\frac{nV}{\sqrt{Hz}}$
DV_{io}	Input Offset Voltage Drift		7	30		7	30	µV/°C
DI_{IO}	Input Offset Current Drift		10	200		10	200	pA/°C
V_{O1}/V_{O2}	Channel Separation (note 5) 1kHz ≤ f ≤ 20kHz		120			120		dB

Notes :

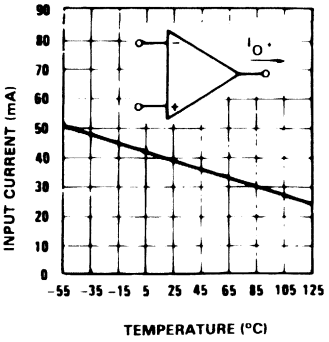
1. Short-circuits from the output to V_{CC} can cause excessive heating if V_{CC} > 15V. The maximum output current is approximately 40mA independent of the magnitude of V_{CC}. Destructive dissipation can result from simultaneous short-circuit on all amplifiers.
2. The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. V_o = 1.4V, R_s = 0Ω, 5V < V_{CC}^+ < 30V, 0 < V_{ic} < V_{CC}^+ - 1.5V
4. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V_{CC}^+ - 1.5V, but either or both inputs can go to +32V without damage.
5. Due to the proximity of external components insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequences.
6. This input current only exists when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward biased and thereby acting as input diodes clamps. In addition to this diode action, there is also NPN parasitic action on the IC chip. this transistor action can cause the output voltages of the Op-amps to go to the V_{CC} voltage level (or to ground for a large overdrive) for the time duration than an input is driven negative.
   This is not destructive and normal output will set up again for input voltage higher than -0.3V.

INPUT BIAS CURRENT vs AMBIENT TEMPERATURE



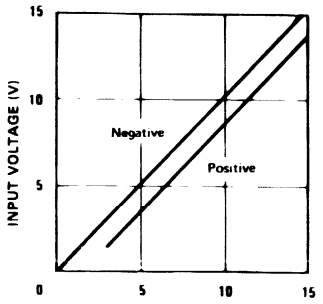
124-03.EPS

CURRENT LIMITING (Note 8)



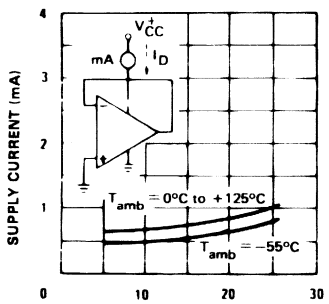
124-04.EPS

INPUT VOLTAGE RANGE



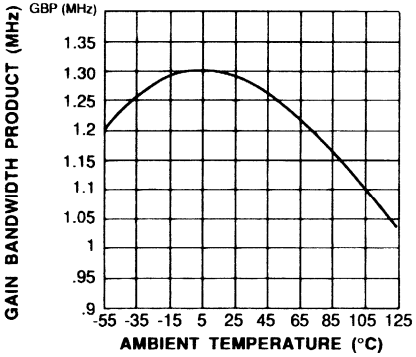
124-05.EPS

SUPPLY CURRENT



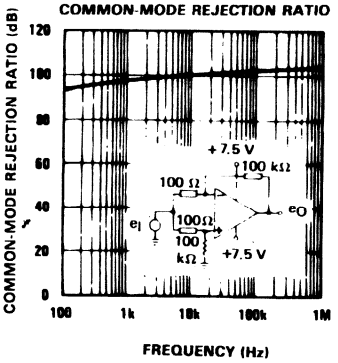
124-06.EPS

GAIN BANDWIDTH PRODUCT



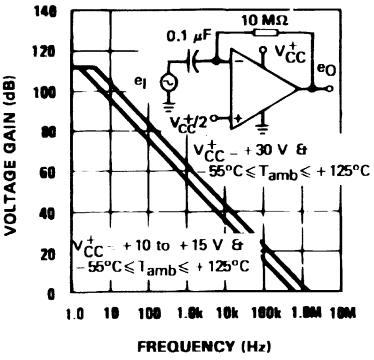
124-07.EPS

COMMON-MODE REJECTION RATIO

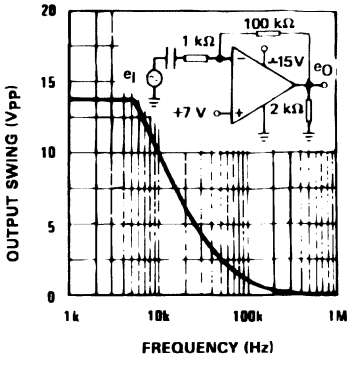


124-08.EPS

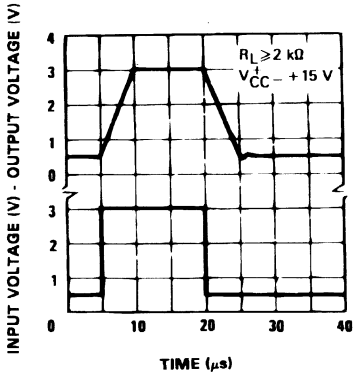
OPEN LOOP FREQUENCY RESPONSE



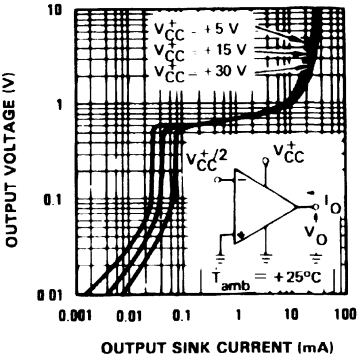
LARGE SIGNAL FREQUENCY RESPONSE



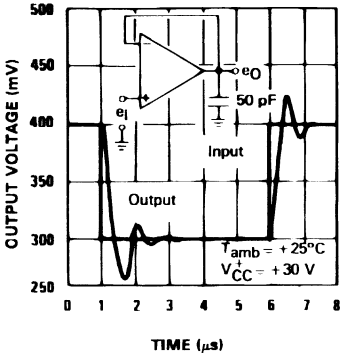
VOLTAGE FOLLOWER PULSE RESPONSE



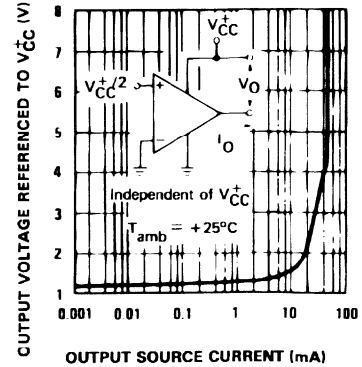
OUTPUT CHARACTERISTICS (CURRENT SINKING)



VOLTAGE FOLLOWER PULSE RESPONSE (SMALL SIGNAL)

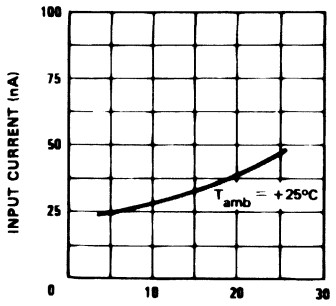


OUTPUT CHARACTERISTICS (CURRENT SOURCING)



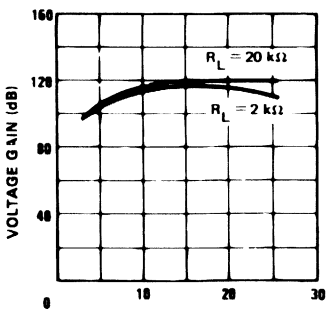
124-09.EPS

INPUT CURRENT



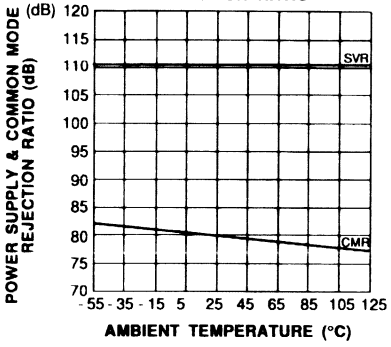
124-10.EPS

VOLTAGE GAIN



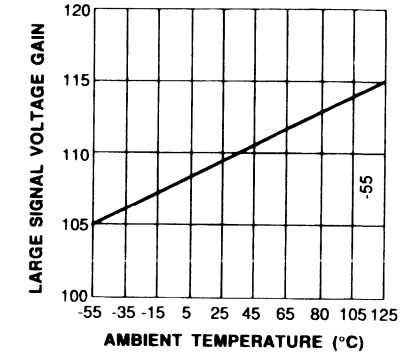
124-11.EPS

POWER SUPPLY & COMMON MODE REJECTION RATIO



124-12.EPS

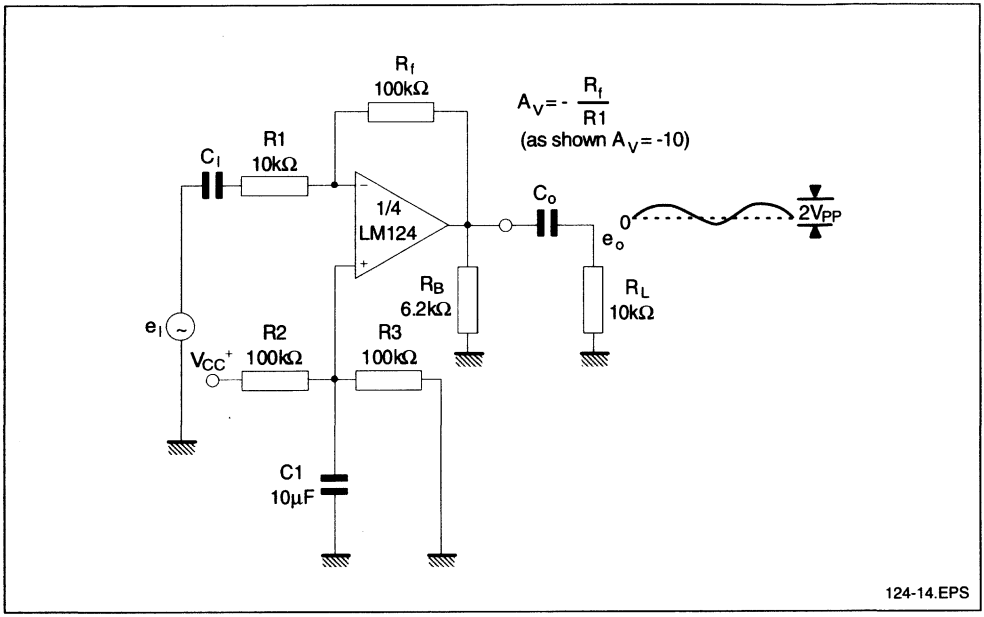
LARGE SIGNAL VOLTAGE GAIN



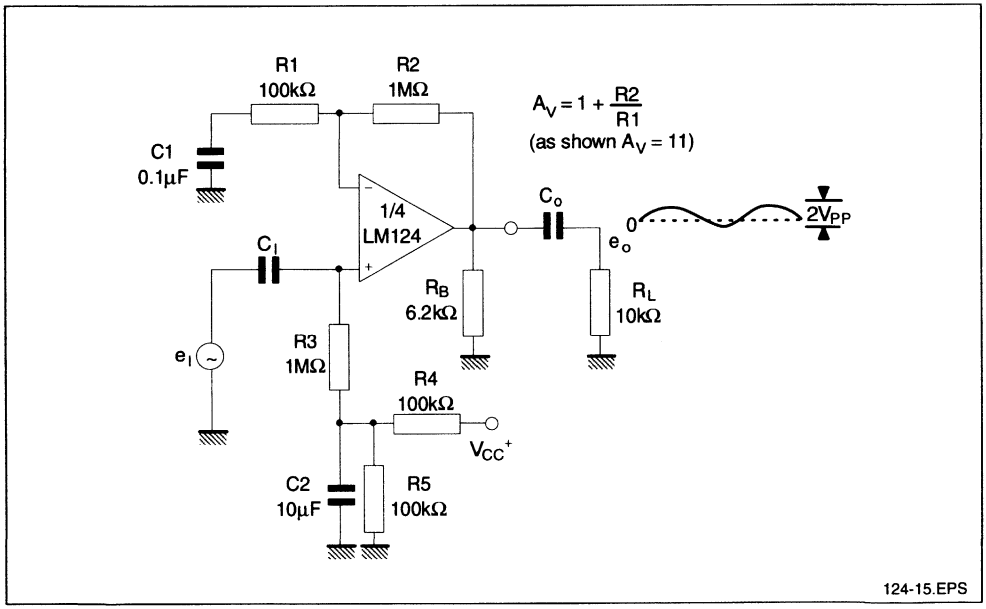
124-13.EPS

TYPICAL SINGLE - SUPPLY APPLICATIONS

AC COUPLED INVERTING AMPLIFIER

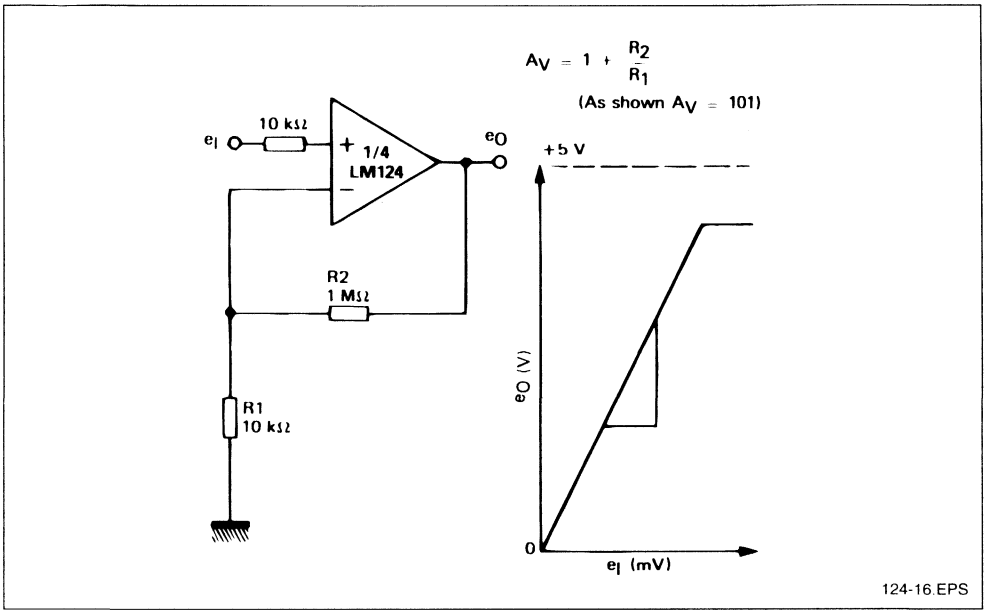


AC COUPLED NON-INVERTING AMPLIFIER

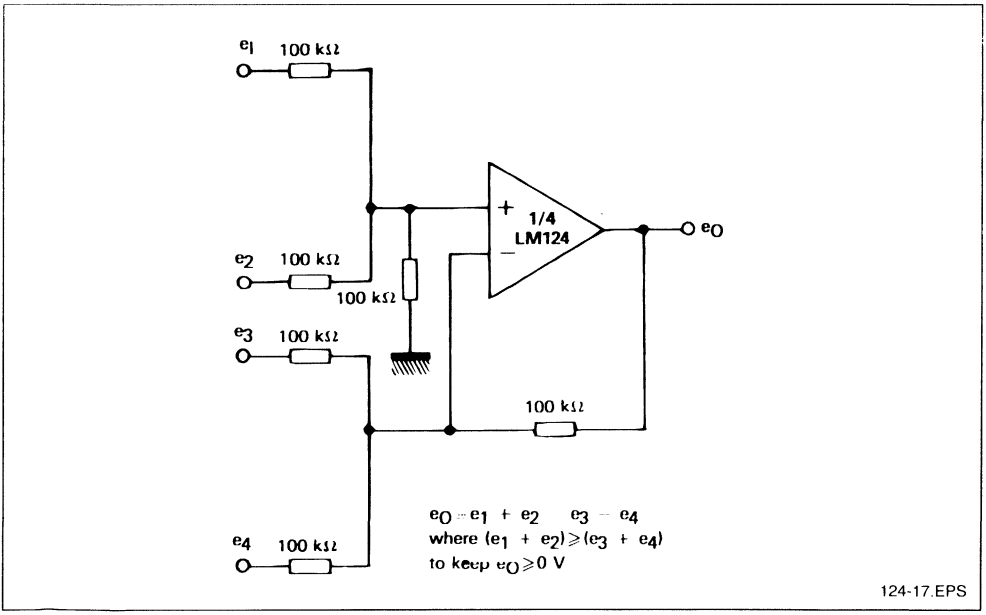


TYPICAL SINGLE - SUPPLY APPLICATIONS (continued)

NON-INVERTING DC GAIN

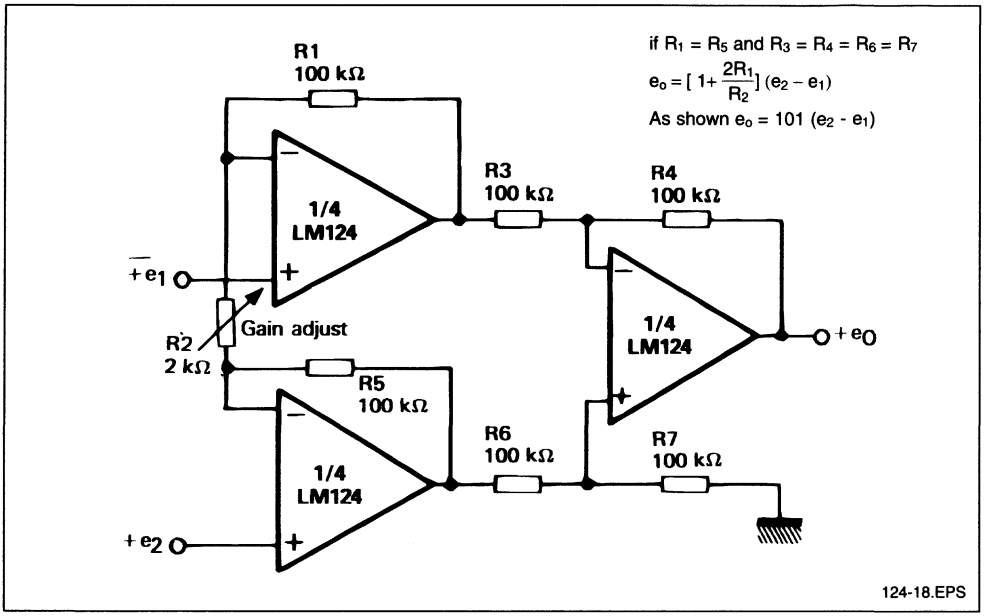


DC SUMMING AMPLIFIER

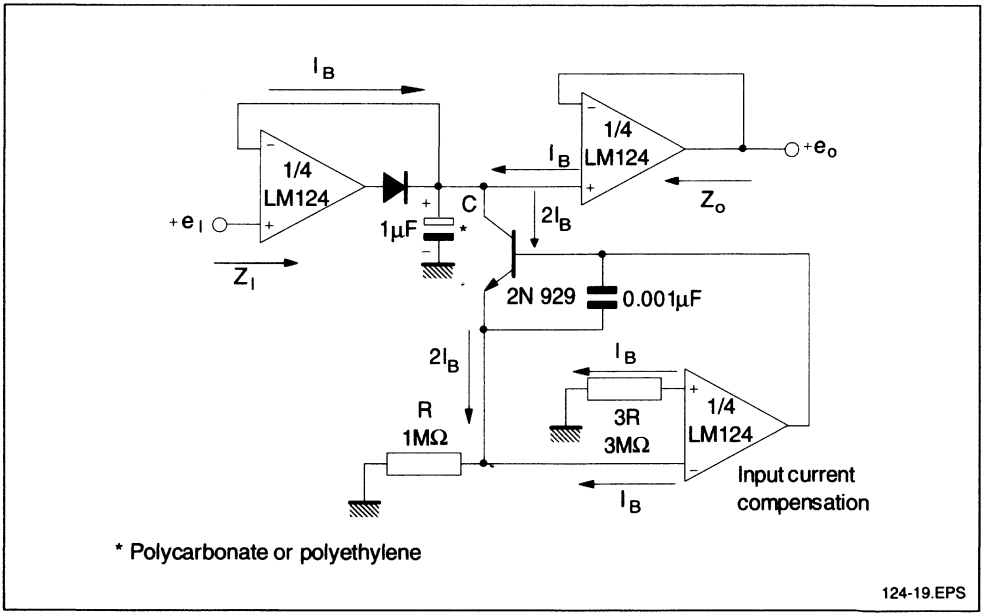


TYPICAL SINGLE - SUPPLY APPLICATIONS (continued)

HIGH INPUT Z ADJUSTABLE GAIN DC INSTRUMENTATION AMPLIFIER

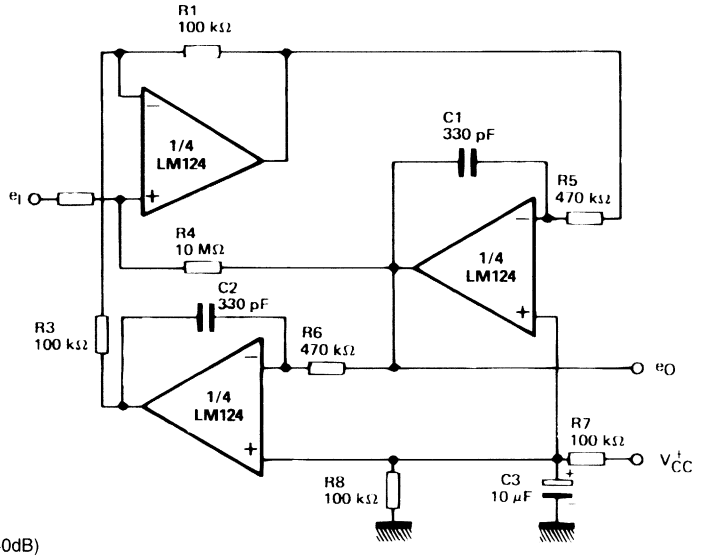


LOW DRIFT PEAK DETECTOR



TYPICAL SINGLE - SUPPLY APPLICATIONS (continued)

ACTIVE BANDPASS FILTER



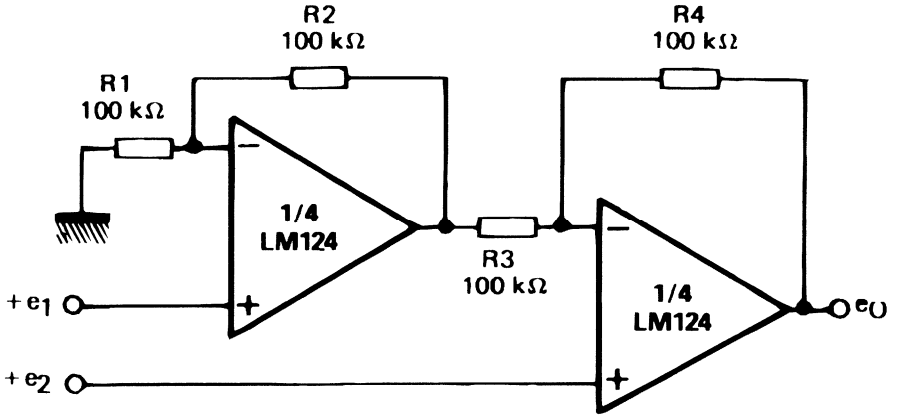
F_O = 1kHz
Q = 50
A_V = 100 (40dB)

124-20.EPS

HIG INPUT Z, DC DIFFERENTIAL AMPLIFIER

For $\frac{R_1}{R_2} = \frac{R_4}{R_3}$ (CMRR depends on this resistor ratio match) $e_o = (1+\frac{R_4}{R_3})(e_2 - e_1)$

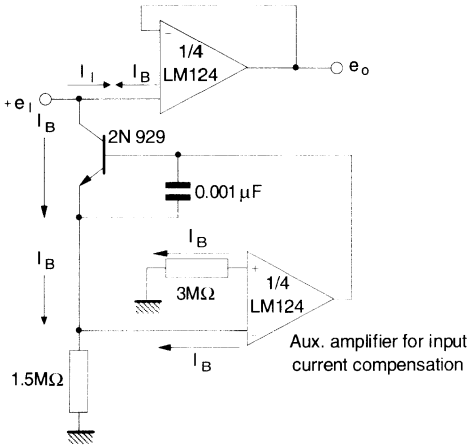
As shown $e_o = (e_2 - e_1)$



124-21.EPS

TYPICAL SINGLE - SUPPLY APPLICATIONS (continued)

USING SYMMETRICAL AMPLIFIERS TO REDUCE INPUT CURRENT (GENERAL CONCEPT)



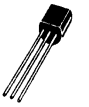
124-22.EPS

SGS-THOMSON MICROELECTRONICS

LM134-LM234 LM334

THREE TERMINAL ADJUSTABLE CURRENT SOURCES

- OPERATES from 1V to 40V
- 0.02% V CURRENT REGULATION
- PROGRAMMABLE from 1µA to 10mA
- ±3% INITIAL ACCURACY



Z
TO92
(Plastic Package)

D
SO8
(Plastic Micropackage)

DESCRIPTION

The LM134/LM234/LM334 are 3-terminal adjustable current sources characterized by :

- an operating current range of 10000 : 1
- an excellent current regulation
- a wide dynamic voltage range of 1V to 40V

The current is determined by an external resistor without requiring other external components.

Reverse voltages of up to 20V will only draw a current of several microamperes. This enables the circuit to operate as a rectifier and as a source of current in a.c. applications.

For the LM134/LM234/LM334, the voltage on the control pin is 64mV at +25°C and is directly proportional to the absolute temperature (°K). The simplest external resistor connection generates a current with ≈ 0.33%/°C temperature dependence. Zero drift can be obtained by adding an additional resistor and a diode to the external circuit.

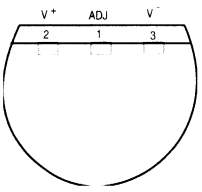
ORDER CODES

Part Number	Temperature Range	Package	
		Z	D
LM134	–55°C, +125°C	•	•
LM234	–25°C, +100°C	•	•
LM334	0°C, +70°C	•	•
Example : LM134Z			

134-01.TBL

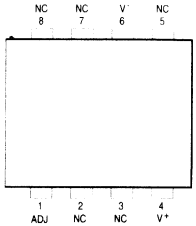
PIN CONNECTIONS

TO92
(Bottom view)



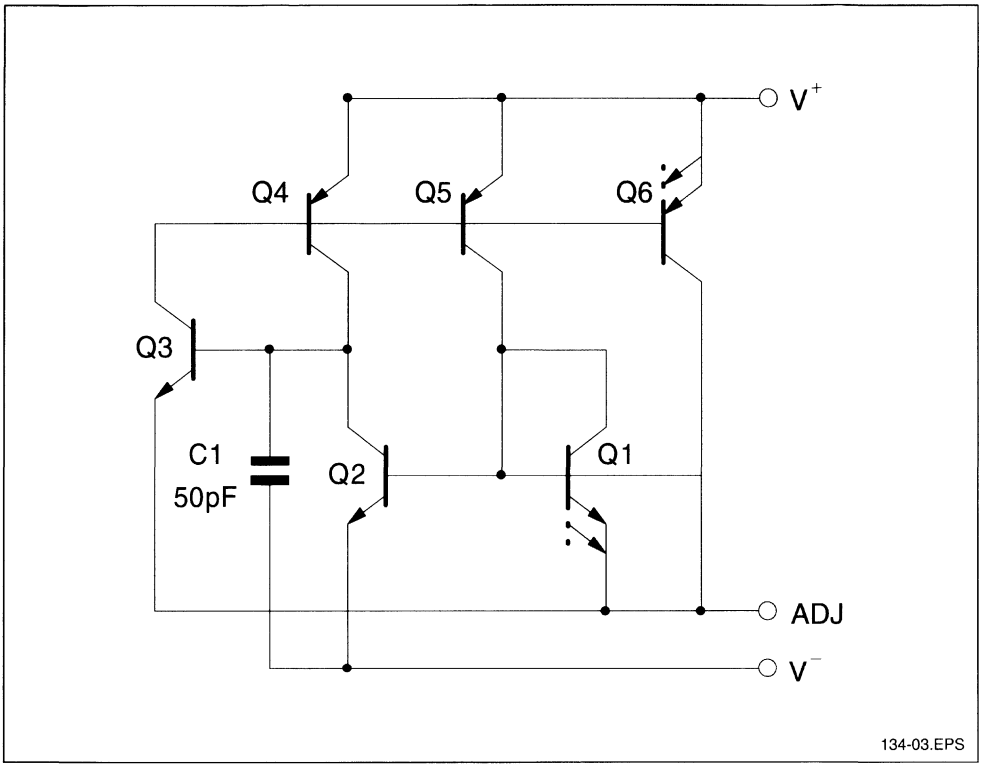
134-01.EPS

SO8
(Top view)



134-02.EPS

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATING

Symbol	Parameter		LM134 - LM234	LM334	Unit
	Voltage V^+ to V^- Forward Reverse		 40 20	 30 20	V
V_{ADJ}	ADJ Pin to V^- Voltage		5	5	V
I_{SET}	Set Current		10	10	mA
P_{tot}	Power Dissipation		400	400	mW
T_{stg}	Storage Temperature Range		−65 to +150		°C
T_{oper}	Operating Free-air Temperature Range	LM134 LM234 LM334	−55 to +125 −25 to +100 0 to +70		°C

ELECTRICAL CHARACTERISTICS

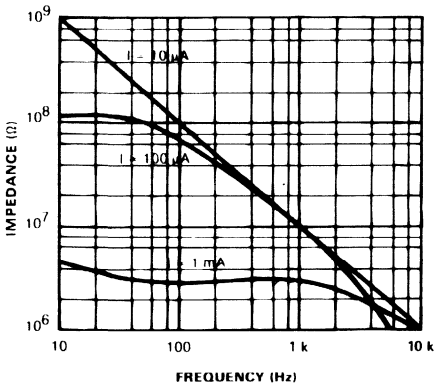
T_j = +25°C with pulse testing so that junction temperature does not change during testing (unless otherwise specified)

Parameter	LM134 - LM234			LM334			Unit
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Set Current Error (V^+ = +2.5V) - (note 1)							%
10µA ≤ I_{SET} ≤ 1mA			3			6	
1mA ≤ I_{SET} ≤ 5mA			5			8	
2µA ≤ I_{SET} ≤ 10µA			8			12	
Ratio of Set Current to V^- Current							
10µA ≤ I_{SET} ≤ 1mA	14	18	23	14	18	26	
1mA ≤ I_{SET} ≤ 5mA		14			14		
2µA ≤ I_{SET} ≤ 10µA		14			14		
Minimum Operating Voltage							V
2µA ≤ I_{SET} ≤ 100µA		0.8			0.8		
100µA ≤ I_{SET} ≤ 1mA		0.9			0.9		
1mA ≤ I_{SET} ≤ 5mA		1			1		
Average change in set current with input voltage							% / V
2µA ≤ I_{SET} ≤ 1mA							
+1.5V ≤ V^+ ≤ +5V		0.02	0.05		0.02	0.1	
+5V ≤ V^+ ≤ +40V		0.01	0.03		0.01	0.05	
1mA ≤ I_{SET} ≤ 5mA							
+1.5V ≤ V^+ + ≤ +5V		0.03			0.03		
+5V ≤ V^+ ≤ +40V		0.02			0.02		
Temperature Dependence of set current - (note 2)							
25µA ≤ I_{SET} ≤ 1mA	0.96 T	T	1.04 T	0.96 T	T	1.04 T	
Effective Shunt Capacitance		15			15		pF

134-03.TBL

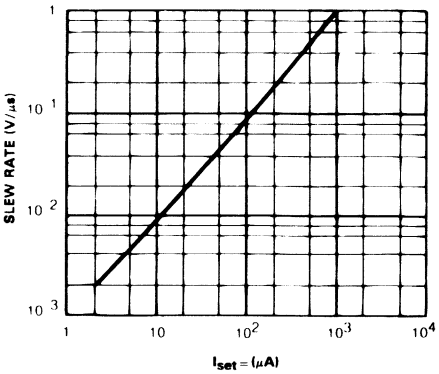
Notes : 1. Set current is the current flowing into theV^+ pin. It is determined by the following formula Iset = 67.7mV/R_{set} (T_j = +25°C).
Set current error is expressed as a percent deviation from this amount.
2. I_{set} is directly proportional to absolute temperature (°K). I_{set} at any temperature can be calculated from I_{set} = I_O (T/T_O) where I_O is Iset measured at T_O (°K).

OUTPUT IMPEDANCE



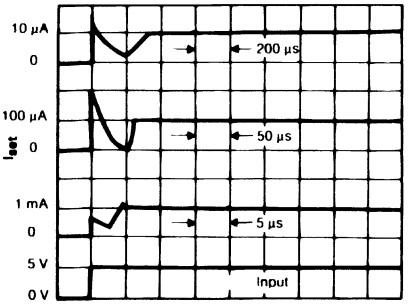
134-04.EPS

MAXIMUM SLEW RATE FOR LINEAR OPERATION



134-05.EPS

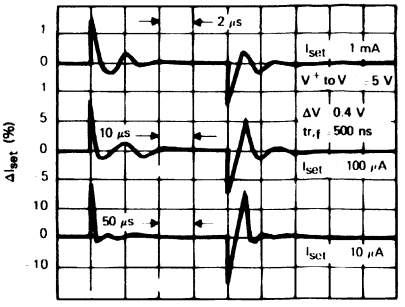
START UP



TIME (SCALE CHANGES AT EACH CURRENT LEVEL).

134-06.EPS

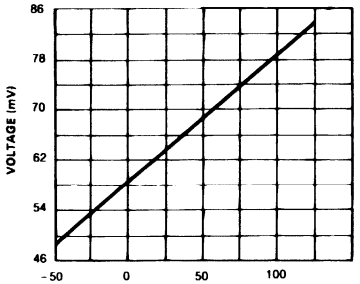
TRANSIENT RESPONSE



TIME (SCALE CHANGES AT EACH CURRENT LEVEL).

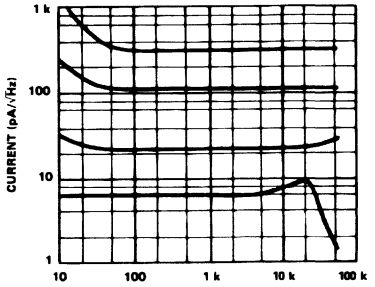
134-07.EPS

VOLTAGE ACROSS R_{set}



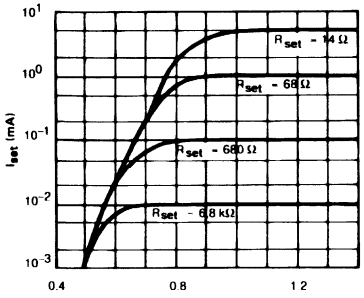
134-08.EPS

CURRENT NOISE



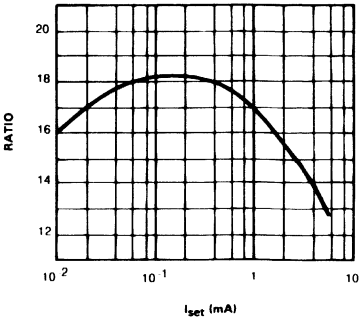
134-09.EPS

TURN-ON VOLTAGE



134-10.EPS

RATIO OF I_{set} to V CURRENT



135-11.EPS

APPLICATION HINT

SLEW RATE

At slew rates above a threshold (see curve) the LM134, LM234, LM334 can have a non-linear current characteristic. The slew rate at which this takes place is directly proportional to I_{set}. At I_{set} = 10µA, dv/dt max. = 0.01V/µS ; at I_{set} = 1mA, dv/dt max. = 1V/µS. Slew rates of more than 1V/µS do not damage the circuit nor do they produce high currents.

THERMAL EFFECTS

Internal heating can have a significant effect on current regulation for an I_{set} above 100µA. For example, each increase of 1V in the voltage across the LM134 at I_{set} = 1mA will increase the junction temperature by ≈ 0.4°C (in still air). The output current (I_{set}) has a temperature coefficient of about 0.33%/°C. Thus the change in current due to the increase in temperature will be (0.4) (0.33) = 0.132%. This is a degradation of 10 : 1 in regulation versus the true electrical effects. Thermal effects should be taken into account when d.c. regulation is critical and I_{set} is higher than 100µA. The dissipation of the connections of CB-97 package can reduce this thermal effect by a coefficient of more than 3.

SHUNT CAPACITANCE

In certain applications, the 15pF value for the shunt capacitance should be reduced :

- because of loading problems,
- because of limitation of the output impedance of the current source in a.c. applications. This reduction of the capacitance can be easily carried out by adding a FET as indicated in the typical applications. The value of this capacitance can be reduced by at least 3pF and regulation can be improved by an order of magnitude without any modification of the d.c. characteristics (except for the minimum input voltage).

NOISE

The current noise produced by LM134, LM234, LM334 is about 4 times that of a transistor. If the LM134, LM234, LM334 is utilized as an active load for a transistor amplifier, the noise at the input will increase by about 12dB. In most cases this is acceptable, and a single amplifier can be built with a voltage gain higher than 2000.

LEAD RESISTANCE

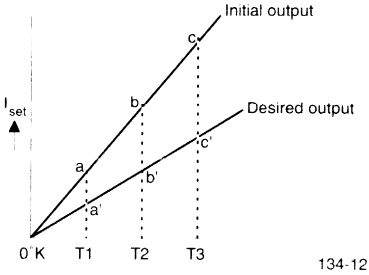
The sense voltage which determines the current of the LM134, LM234, LM334, is less than 100mV. At this level, the effects of the thermocouple and the connection resistance should be reduced by locating the current setting resistor close to the device. Do not use sockets for the ICs. A contact resistance of 0.7Ω is sufficient to decrease the output current by 1% at the 1mA level.

SENSING TEMPERATURE

The LM134, LM234, LM334 are excellent remote controlled temperature sensors because their operation as sources of current preserves their accuracy even in the case of long connecting wires. The output current is directly proportional to the absolute temperature in degrees Kelvin according to the following equation.

$$I_{set} = \frac{(227\mu V/^{\circ}K)\,(T)}{R_{set}}$$

The calibration of the LM134, LM234, LM334 is simplified by the fact that most of the initial accuracy is due to gain limitation (slope error) and not an offset. Gain adjustment is a one point trim because the output of the device extrapolates to zero at 0°K.



134-12.EPS

This particularity of the LM134, LM234, LM334 is illustrated in the above diagram. Line abc represents the sensor current before adjustment and line a'b'c' represents the desired output. An adjustment of the gain provided at T2 will move the output from b to b' and will correct the slope at the same time so that the output at T1 and T3 will be correct. This gain adjustment can be carried out by means of R_{set} or the load resistor utilized in the circuit. After adjustment, the slope error should be less than 1%. A low temperature coefficient for R_{set} is necessary to keep this accuracy. A 33ppm/°C temperature drift of R_{set} will give an error of 1% on the slope because the resistance follows the same temperature variations as the LM134, LM234, LM334. Three wires are required to isolate R_{set} from the LM134, LM234, LM334. Since this solution is not recommended. Metal-film resistors with a drift less than 20ppm/°C are now available. Wirewound resistors can be utilized when very high stability is required.

TYPICAL APPLICATIONS

Figure 1 : Basic 2-terminal Current Source

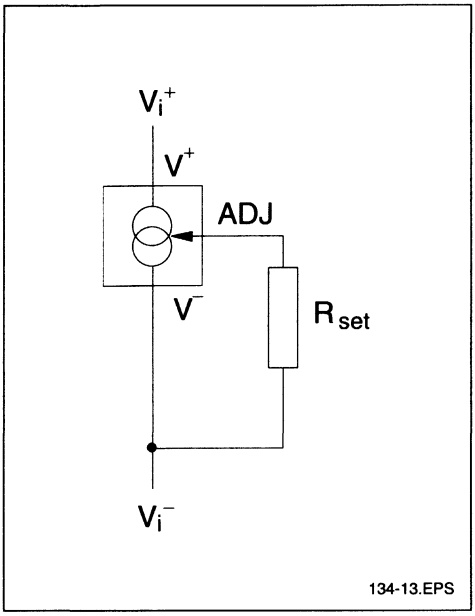


Figure 2 : Alternate Trimming Technique

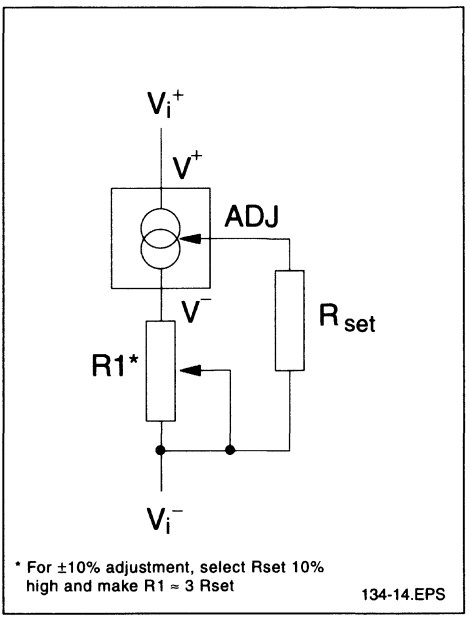


Figure 3 : Terminating Remote Sensor for Voltage Output

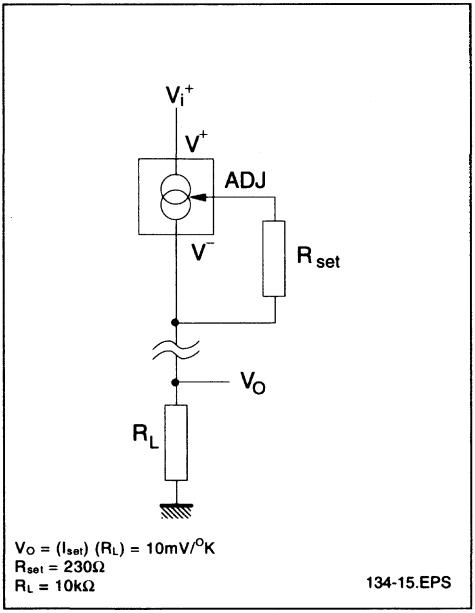


Figure 4 : Zero Temperature Coefficient Current Source

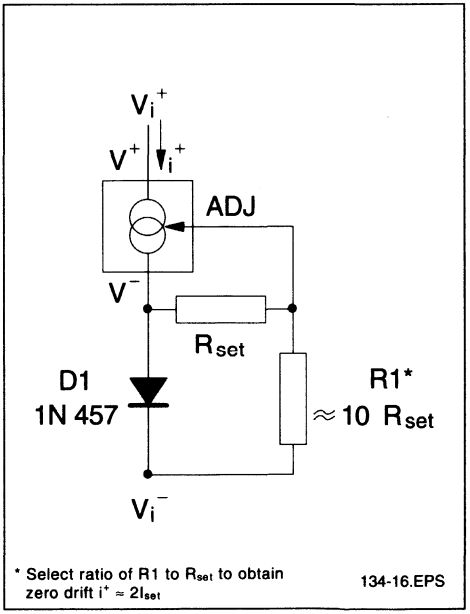
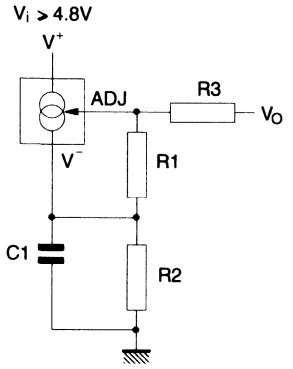


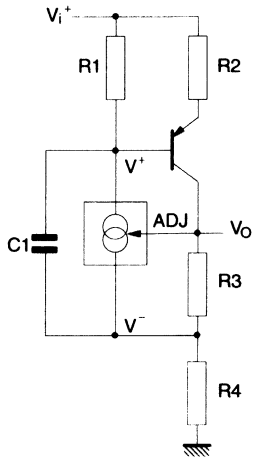
Figure 5 : Low Output Impedance Thermometer



$R1 = 230\Omega$, 1%
$R2 = 10k\Omega$, 1%
$R3 = 600\Omega$
$V_O = 10mV/^oK$
$Z_O \leq 100\Omega$
134-17.EPS

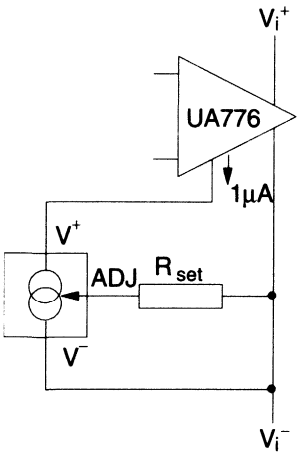
Output impedance of the LM134, LM234, LM334 at the "ADJ" pin is approximately $\frac{-R_o\Omega}{16}$ where R_o is the equivalent external resistance connected to the V^- pin. This negative resistance can be reduced by a factor of 5 or more by inserting an equivalent resistor in series with the output

Figure 6 : Low Output Impedance Thermometer



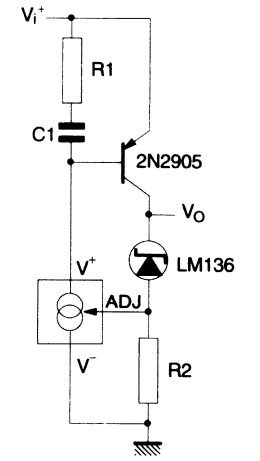
$R1 = 15k\Omega$
$R2 = 300\Omega$
$R3 = 100\Omega$
$R4 = 4.5k\Omega$
$C1 = 2.2nF$
$V_O = 10mV/^oK$
$Z_O \leq 2\Omega$
134-18.EPS

Figure 7 : Micropower Bias



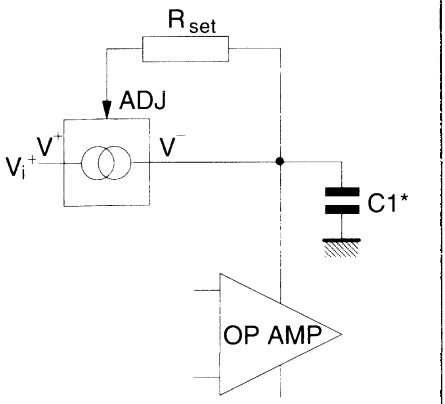
$R_{set} = 68k\Omega$
134-19.EPS

Figure 8 : Low Input Voltage Reference Driver



$R1 = 1.5k\Omega$
$R2 = 120\Omega$
$C1 = 0.1\mu F$
$I_O \leq 3mA$
$V_i^+ \geq Vref + 200mV$
$V_O = V_Z + 64mV$ (+25°C)
134-20.EPS

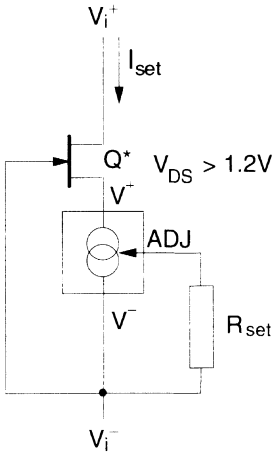
Figure 9 : In-line Current Limiter



* Use minimum value required to ensure stability of protected circuit

134-21.EPS

Figure 10 : Fet Cascading for Low Capacitance



* Select Q to ensure at least 1V across the LM134, LM234, LM334.
$V_P\ (1 - I_{set}/I_{DSS}) \geq 1.2V$

134-22.EPS

LM135
LM235 - LM335/A

PRECISION TEMPERATURE SENSORS

- DIRECTLY CALIBRATED IN °K
- 1°C INITIAL ACCURACY
- OPERATES FROM 400µA TO 5mA
- LESS THAN 1Ω DYNAMIC IMPEDANCE

Z
TO92
(Plastic Package

D
SO8
(Plastic Micropackage)

DESCRIPTION

The LM135, LM235, LM335 are precision temperature sensors which can be easily calibrated. They operate as a 2-terminal Zener and the breakdown voltage is directly proportional to the absolute temperature at 10mV/°K. The circuit has a dynamic impedance of less than 1Ω and operates within a range of current from 400µA to 5mA without alteration of its characteristics. Calibrated at +25°C, the LM135, LM235, LM335 have a typical error of less than 1°C over a 100°C temperature range. Unlike other sensors, the LM135, LM235, LM335 have a linear output.

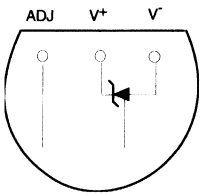
ORDER CODES

Part number	Temperature Range	Package	
		Z	D
LM135	–55°C, +150°C	•	•
LM235	–40°C, +125°C	•	•
LM335/A	–40°C, +100°C	•	•

135-01.TBL

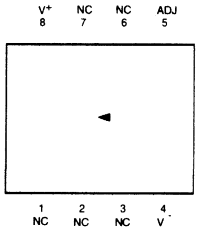
PIN CONNECTIONS

TO92
(Bottom view)



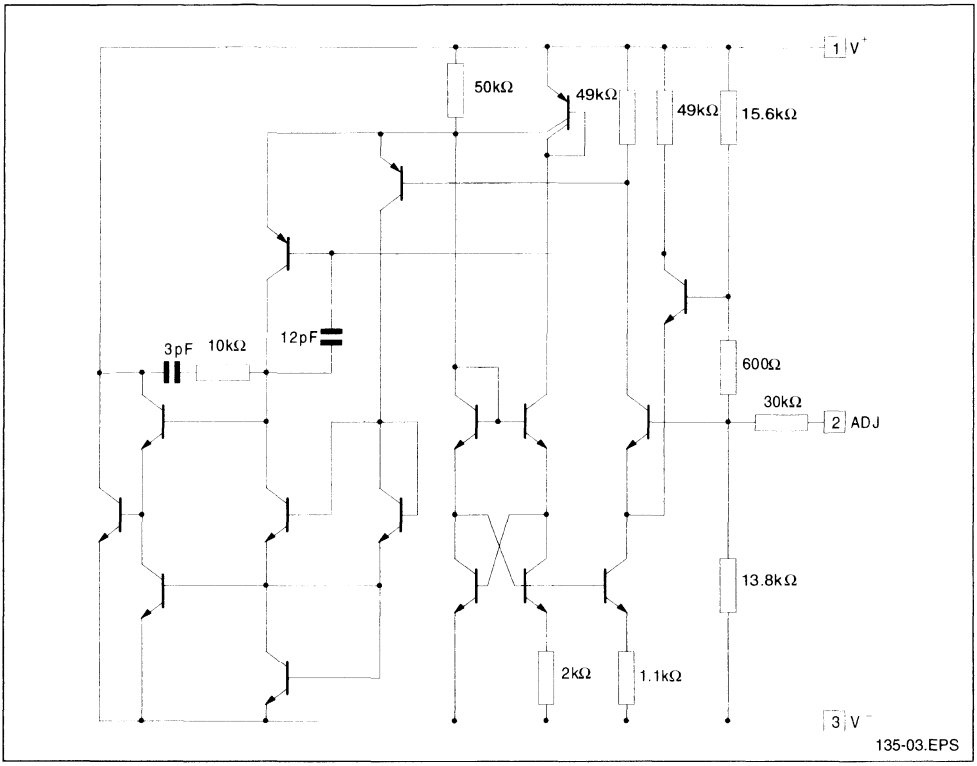
135-01.EPS

SO8
(Top view)



135-02.EPS

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	LM135	LM235	LM335,A	Unit
	Current				mA
I_R	Reverse	15	15	15	
I_F	Forward	10	10	10	
T_{oper}	Operating Free-air Temperature Range - (note 1)				°C
	Continuous	−55 to +150	−40 to +125	−40 to +100	
	Intermittent	+150 to +200	+125 to +150	+100 to +125	
T_{stg}	Storage Temperature Range	−65 to +150	−65 to +150	−65 to +150	°C

Note : 1. $T_j \leq 150°C$

TEMPERATURE ACCURACY

Parameter		LM135 - LM235 LM335A			LM335			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Operating Output Voltage T_{case} = +25°C, I_R = 1mA		2.95	2.98	3.01	2.92	2.98	3.04	V
Uncalibrated Temperature Error (I_R = 1mA) T_{case} = +25°C $T_{min.} \leq T_{case} \leq T_{max.}$			1 2	3 5		2 4	6 9	°C
Temperature Error with 25°C Calibration $T_{min.} \leq T_{case} \leq T_{max.}$, I_R = 1mA	LM135 - LM235 LM335 LM335A		0.5 0.5	1.5 1		 1 	 2 	°C
Calibrated Error at Extended Temperature $T_{case} = T_{max.}$ (intermittent)			2			2		°C
Non-linearity (I_R = 1mA)	LM135 - LM235 LM335 LM335A		0.3 0.3	1 1.5		 0.3 	 1.5 	°C

135-03.TBL

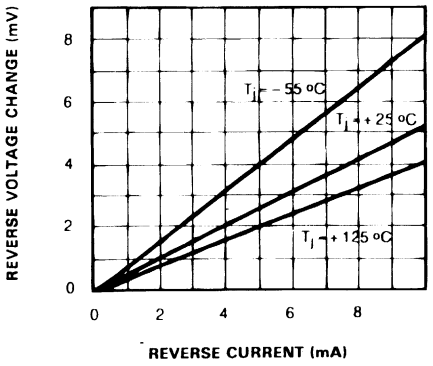
ELECTRICAL CHARACTERISTICS - (note 1)

Parameter		LM135 - LM235			LM335,A			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Operating output voltage change with current 400µA ≤ I_R ≤ 5mA at constant temperature			2.5	10		3	14	mV
Dynamic Impedance (I_R = 1mA)			0.5			0.6		Ω
Output Voltage Temperature Drift			+10			+10		mV/°C
Time Constant	Still Air Air 0.5m/s Stirred Oil		80 10 1			80 10 1		s
Time Stability (T_{case} = +125°C)			0.2			0.2		°C/kh

135-04.TBL

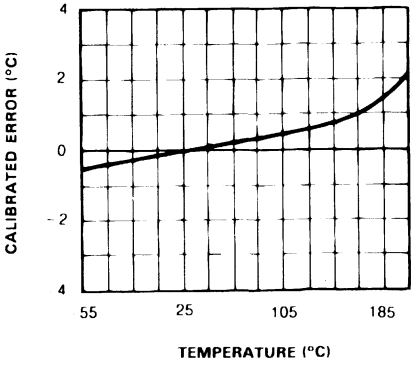
Note : 1. Accuracy measurements are made in a well-stirred oil bath. For other conditions, self heating must be considered.

REVERSE VOLTAGE CHANGE



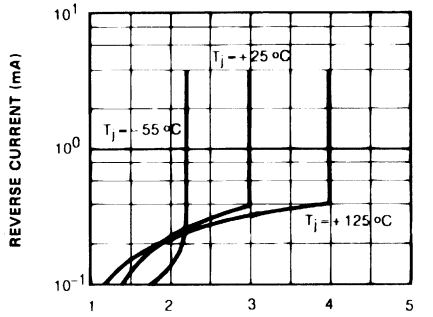
135-04.EPS

CALIBRATED ERROR



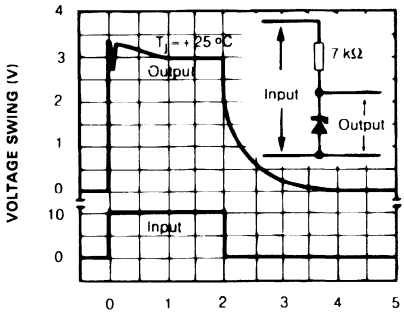
135-05.EPS

REVERSE CHARACTERISTICS



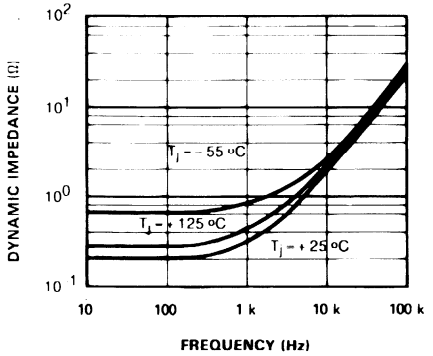
135-06.EPS

RESPONSE TIME



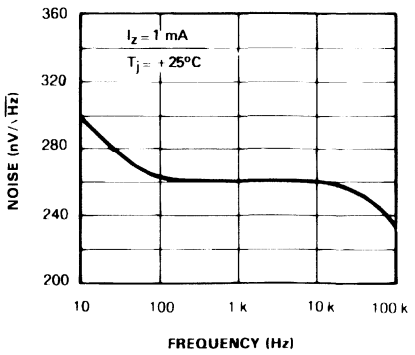
135-07.EPS

DYNAMIC IMPEDANCE



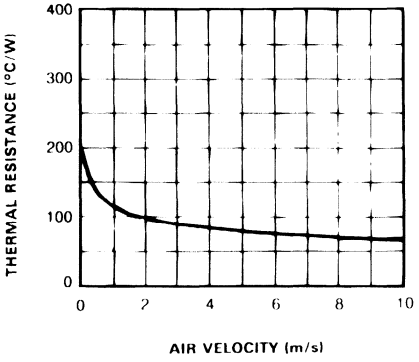
135-08.EPS

NOISE VOLTAGE



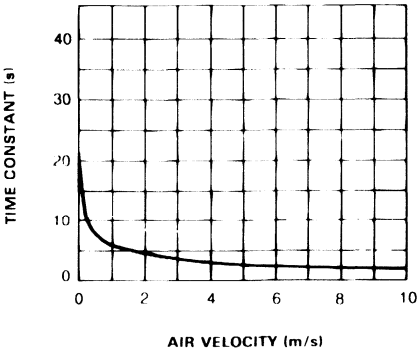
135-09.EPS

THERMAL RESISTANCE JUNCTION TO AIR



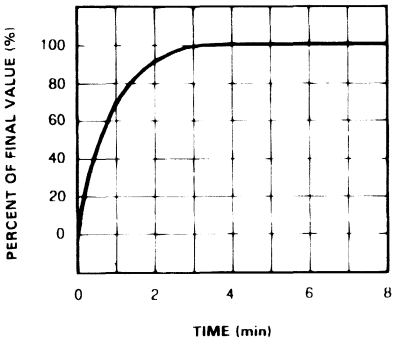
135-10.EPS

THERMAL TIME CONSTANT



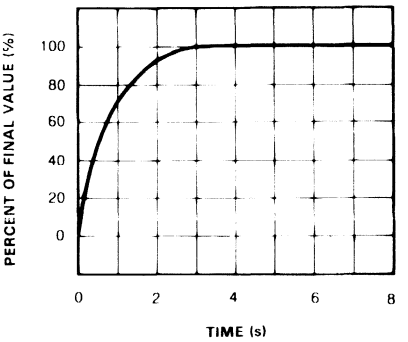
135-11.EPS

THERMAL RESPONSE IN STILL AIR



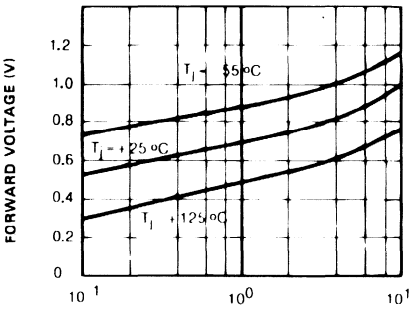
135-12.EPS

THERMAL RESPONSE IN STIRRED OIL BATH



135-13.EPS

FORWARD CHARACTERICS



135-14.EPS

APPLICATION HINTS

There is an easy method of calibrating the device for higher accuracies (see typical applications).

The single point calibration works because the output of the LM135, LM235, LM335 is proportional to the absolute temperature with the extrapolated output of sensor going to 0V at 0°K (–273.15°C). Errors in output voltage versus temperature are only slope. Thus a calibration of the slope at one temperature corrects errors at all temperatures.

The output of the circuit (calibrated or not) can be given by the equation : $V_{OT} = VO_{TO} \times \frac{T}{T_o}$

where T is the unknown temperature and T_O is the reference temperature (in °K).

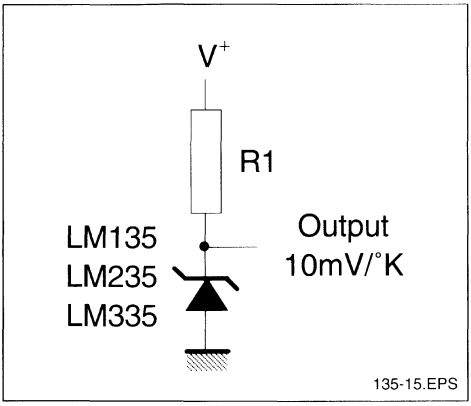
Nominally the output is calibrated at 10mV/°K.

Precautions should be taken to ensure good sensing accuracy. As in the case of all temperatures sensors, self heating can decrease accuracy. The LM135, LM235, LM335 should operate with a low current, but sufficient to drive the sensor and its calibration circuit to their maximum operating temperature.

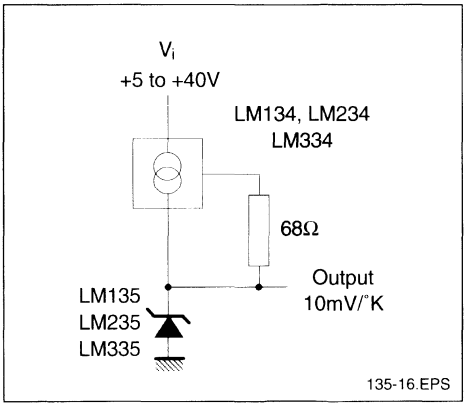
If the sensor is used in surroundings where the thermal resistane is constant, the errors due to self heating can be externally calibrated. This is possible if the circuit is biased with a temperature stable current. Heating will then be proportional to zener voltage and therefore temperature. In this way the error due to self heating is proportional to the absolute temperature as scale factor errors.

TYPICAL APPLICATIONS

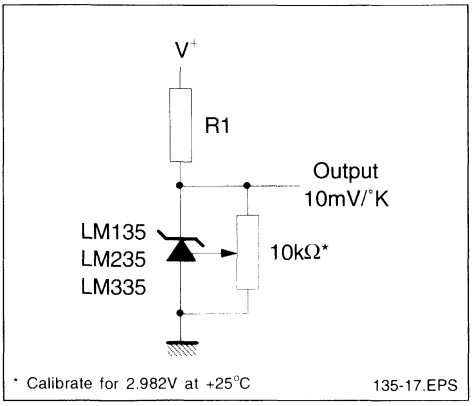
BASIC TEMPERATURE SENSOR



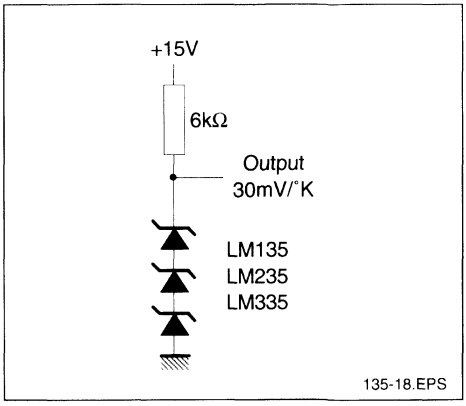
WIDE OPERATING SUPPLY



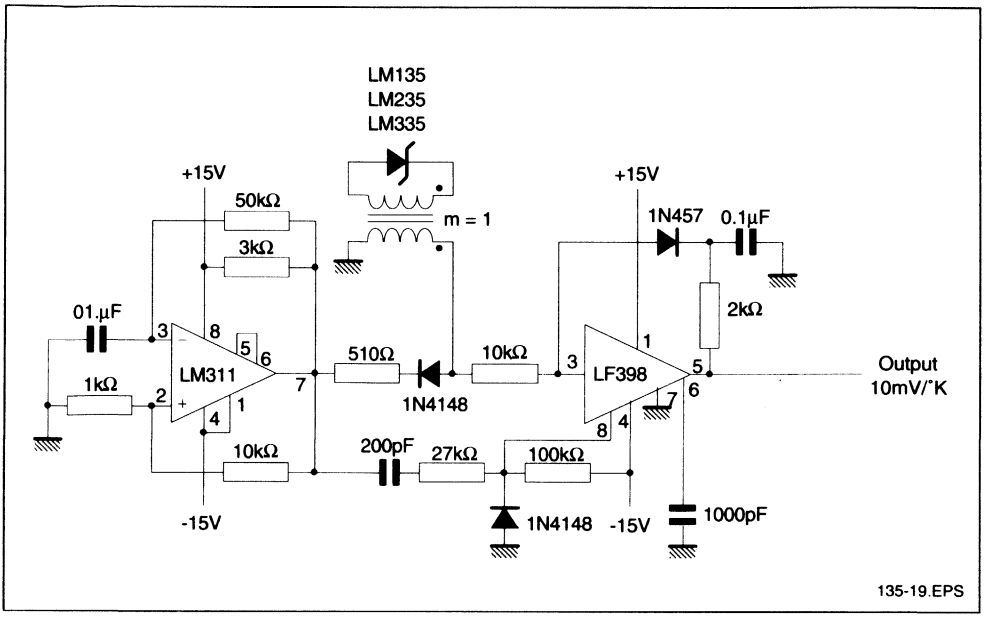
CALIBRATED SENSOR



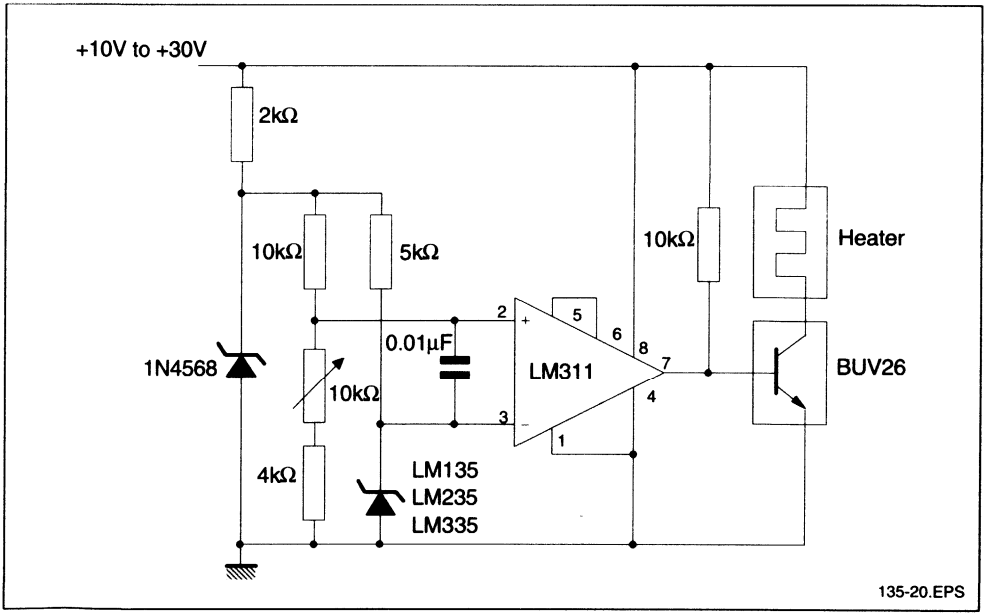
AVERAGE TEMPERATURE SENSING



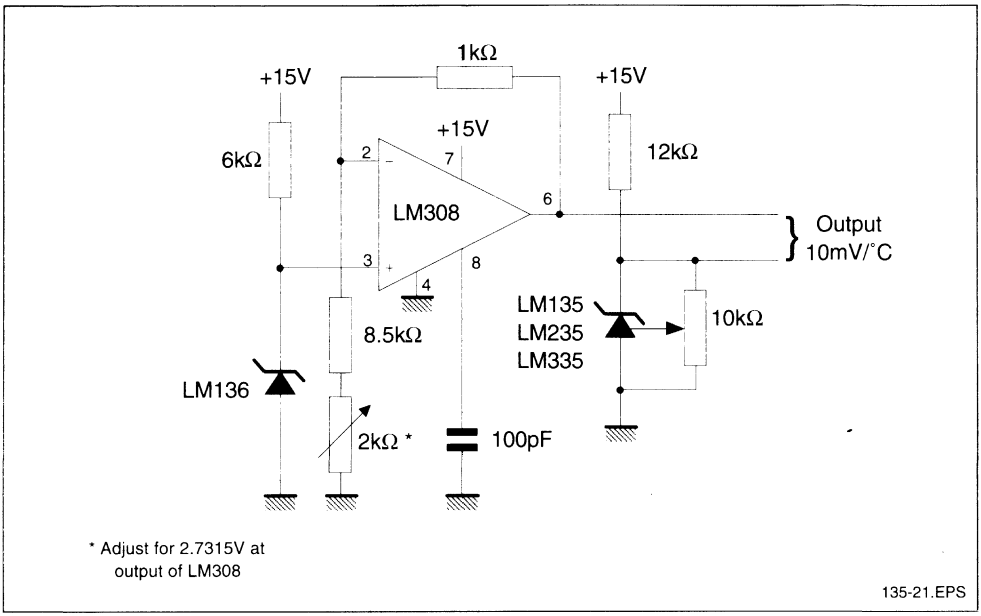
ISOLATED TEMPERATURE SENSOR



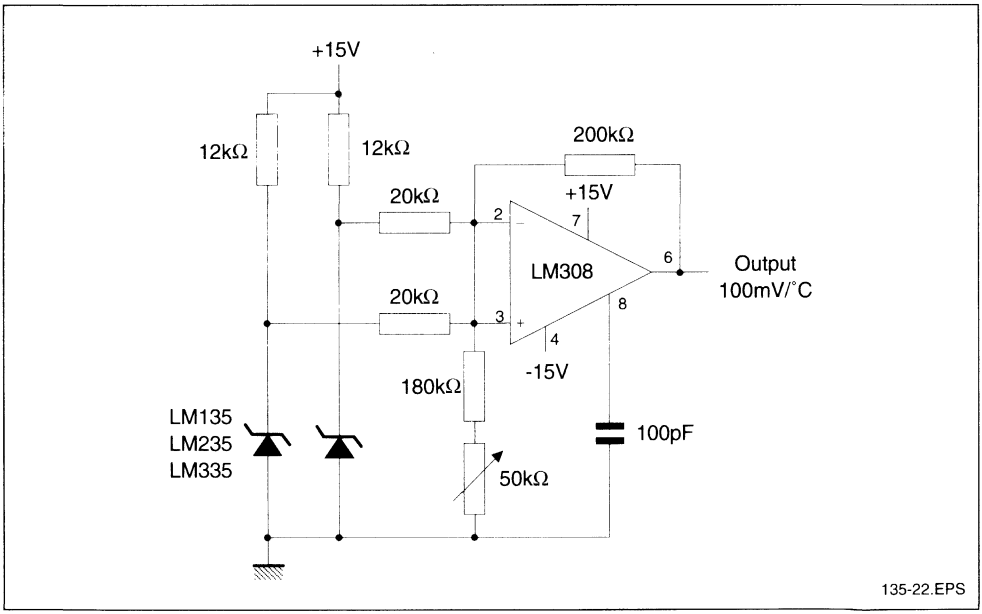
SIMPLE TEMPERATURE CONTROLLER



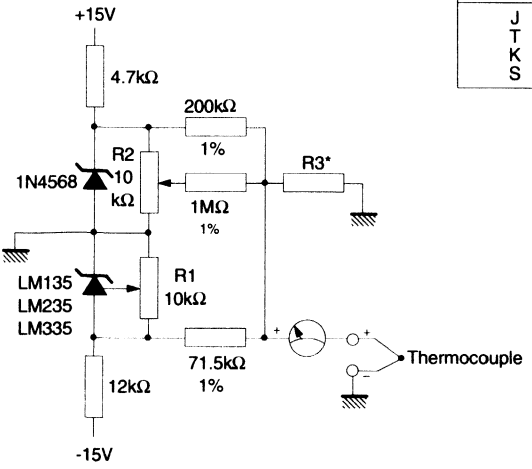
CENTIGRADE THERMOMETER



DIFFERENTIAL TEMPERATURE SENSOR



THERMOCOUPLE COLD JUNCTION COMPENSATION
(compensation for grounded thermocouple)



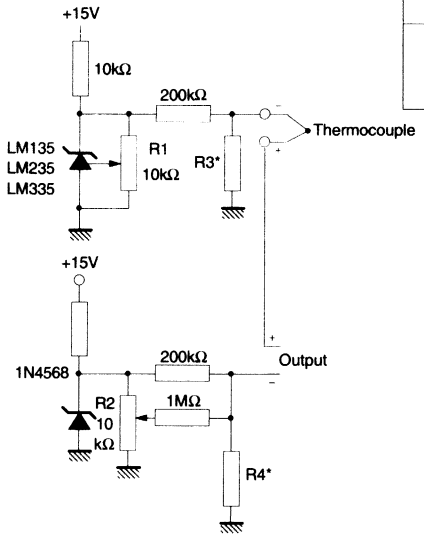
Thermo-couple	R3	Seebeck Coefficient
J	377Ω	52.3μV/°C
T	308Ω	42.8μV/°C
K	293Ω	40.8μV/°C
S	45.8Ω	6.4μV/°C

Adjustments : compensates for both sensor and resistor tolerances.
1. Short 1N4568.
2. Adjust R1 for SEEBECK coefficient times ambient temperature (in degrees K) across R3.
3. Short LM135 and adjust R2 for voltage across R3 corresponding to thermocouple type.
   J 14.32mV K 11.17mV
   T 11.79mV S 1.768mV

* Select R3 for proper thermocouple type

135-23.EPS

SINGLE POWER SUPPLY COLD JUNCTION COMPENSATION



Thermo-couple	R3	R4	Seebeck Coefficient
J	1.05kΩ	365Ω	52.3μV/°C
T	856Ω	315Ω	42.8μV/°C
K	816Ω	300Ω	40.8μV/°C
S	128Ω	46.3Ω	6.4μV/°C

Adjustments :
1. Adjust R1 for the voltage across R3 equal to the SEEBECK coefficient times ambient temperature in degrees Kelvin.
2. Adjust R2 for voltage across R4 corresponding to thermocouple.
   J 14.32mV K 11.17mV
   T 11.79mV S 1.768mV

* Select R3 and R4 for proper thermocouple

135-24.EPS

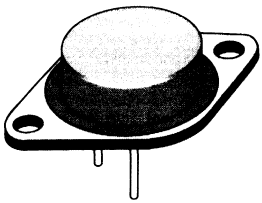
SGS-THOMSON MICROELECTRONICS

LM137/LM237 LM337

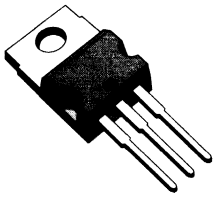
THREE-TERMINAL ADJUSTABLE NEGATIVE VOLTAGE REGULATORS

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST/1)

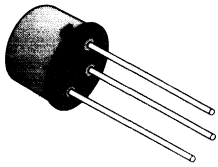
- OUTPUT VOLTAGE ADJUSTABLE DOWN TO V_{ref}
- 1.5A GUARANTEED OUTPUT CURRENT
- 0.3%/V TYPICAL LOAD REGULATION
- 0.01%/V TYPICAL LINE REGULATION
- CURRENT LIMIT CONSTANT WITH TEMPERATURE
- RIPPLE REJECTION : 77dB
- STANDARD 3-LEAD TRANSISTOR PACKAGES
- EXCELLENT THERMAL REGULATION: 0.002%/V
- 50ppm/°C TEMPERATURE COEFFICIENT



TO-3



TO-220



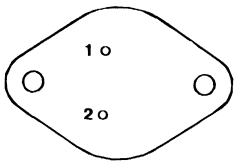
TO-39

DESCRIPTION

The LM137 series are adjustable 3-terminal negative voltage regulators capable of supplying in excess - 1.5A over a - 1.2 to - 37V output voltage range. They are exceptionally easy to use and require only two external resistors to set the output voltage. Further, both line and load regulation are better than standard fixed regulators. Also, LM137 regulators are supplied in standard transistor packages which are easily mounted and handled. In addition to higher performance than fixed regulators, the LM137 series offer full overload protection available only in integrated circuits. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

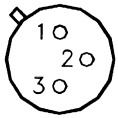
PIN CONNECTIONS

TO-3
(bottom view)



1 - Output
2 - Adj
Case is input

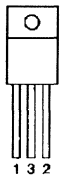
TO-39
(bottom view)



PC11220

1 - Adj
2 - Output
3 - input

TO-220
(front view)



1 - Adj
2 - Output
3 - Input

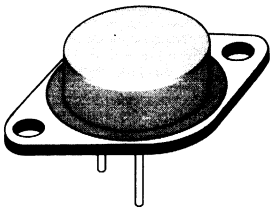
Heatsink surface connected to input

SGS-THOMSON MICROELECTRONICS

LM138/238 LM338

THREE-TERMINAL 5 A ADJUSTABLE VOLTAGE REGULATORS

- GUARANTEED 7A PEAK OUTPUT CURRENT
- GUARANTEED 5A OUTPUT CURRENT
- ADJUSTABLE OUTPUT DOWN TO 1.2V
- LINE REGULATION TYPICALLY 0.005% /V
- LOAD REGULATION TYPICALLY 0.1%
- GUARANTEED THERMAL REGULATION
- CURRENT LIMIT CONSTANT WITH TEMPERATURE
- STANDARD 3-LEAD TRANSISTOR PACKAGE



TO3
K SUFFIX
(Steel Can)

DESCRIPTION

The LM138/LM238/LM338 are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 5A over a 1.2V to 32V output range. They are exceptionally easy to use and require only 2 resistors to set the output voltage. Careful circuit design has resulted in outstanding load and line regulation comparable to many commercial power supplies. The LM138 family is supplied in a standard 3-lead transistor package.

A unique feature of the LM138 family is time-dependent current limiting. The current limit circuitry allows peak currents of up to 12A to be drawn from the regulator for short periods of time. This allows the LM138 to be used with heavy transient loads and speeds start-up under full-load conditions. Under sustained loading conditions, the current limit decreases to a safe value protecting the regulator. Also included on the chip are thermal overload protection and safe area protection for the power transistor. Overload protection remains functional even if the adjustment pin is accidentally disconnected.

Normally, no capacitors are needed unless the device is situated far from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejection ratios which are difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators or discrete designs, the LM238 is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to input differential is not exceeded.

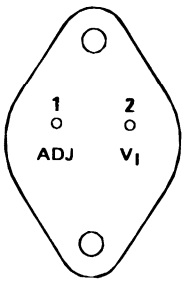
The LM138/LM238/LM338 are packaged in standard steel TO-3 transistor packages. The LM138 is rated for operation from -55 °C to 150 °C, the LM238 from – 25°C to + 150°C and the LM338 from 0°C to + 125°C.

ORDER CODE

PART NUMBER	TEMPERATURE RANGE	PACKAGE
		K
LM138	-55 °C to + 150 °C	•
LM238	-25 °C to + 150 °C	•
LM338	0 °C to + 125 °C	•

EXAMPLE: LM138K

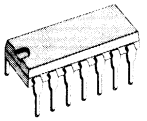
PIN CONNECTION
(bottom view)



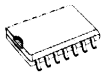
Case is output

LOW POWER QUAD VOLTAGE COMPARATORS

- WIDE SINGLE SUPPLY VOLTAGE RANGE OR DUAL SUPPLIES FOR ALL DEVICES : +2V TO +36V OR ±1V TO ±18V
- VERY LOW SUPPLY CURRENT (1.1mA) INDEPENDENT OF SUPPLY VOLTAGE (1.4mW/comparator at +5V)
- LOW INPUT BIAS CURRENT : 25nA TYP
- LOW INPUT OFFSET CURRENT : ±5nA TYP
- LOW INPUT OFFSET VOLTAGE : ±1mV TYP
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GROUND
- LOW OUTPUT SATURATION VOLTAGE : 250mV TYP. (I_O = 4mA)
- DIFFERENTIAL INPUT VOLTAGE RANGE EQUAL TO THE SUPPLY VOLTAGE
- TTL, DTL, ECL, MOS, CMOS COMPATIBLE OUTPUTS



N
DIP14
(Plastic Package)
J
CERDIP14
(Cerdip Package)



D
SO14
(Plastic Micropackage)

DESCRIPTION

These devices consist of four independent precision voltage comparators with an offset voltage specifications as low as 2mV max for LM339A, LM239A and LM139A. All these comparators were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible.

These comparators also have a unique characteristic in that the input common-mode voltage range includes ground even though operated from a single power supply voltage.

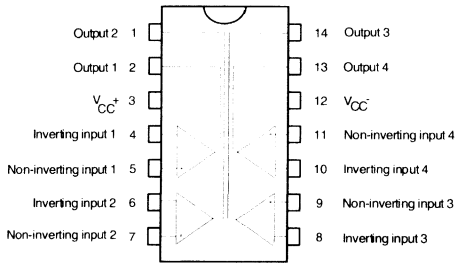
ORDER CODES

Part Number	Temperature Range	Package		
		N	J	D
LM139/A	−55, +125°C	•	•	•
LM239/A	−40, +105°C	•	•	•
LM339/A	0, +70°C	•	•	•
LM2901	−40, +105°C	•	•	•

Examples : LM139AN, LM2901D

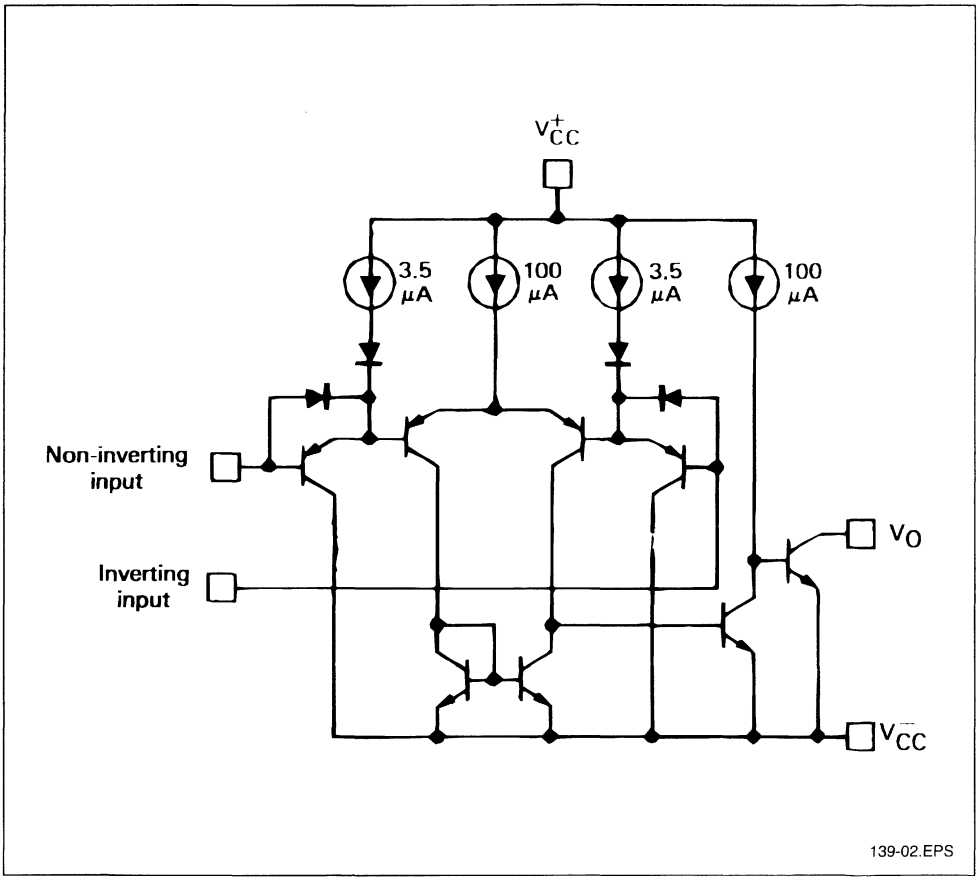
139-01.TBL

PIN CONNECTIONS (top view)



139-01.EPS

SCHEMATIC DIAGRAM (1/4 LM139)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	LM139,A LM239,A	LM339,A	LM2901	Unit
V_{CC}	Supply Voltage	±18 to 36	±18 to 36	±18 to 36	V
V_{id}	Differential Input Voltage	±36	±36	±36	V
V_i	Input Voltage	-0.3 to +36	-0.3 to +36	-0.3 to +36	V
	Output Short-circuit to Ground - (note 1)	Infinite			
P_{tot}	Power Dissipation	570	570	570	mW
T_{oper}	Operating Free-air Temperature Range LM239,A	-55, +125 -40, +105	0, +70	-40, +105	°C
T_{stg}	Storage Temperature Range	-65, +150	-65, +150	-65, +150	°C

139-02 TRI

Notes : 1. Short-circuit from the output to V_{CC}^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20mA, independent of the magnitude of V_{CC}^+.

ELECTRICAL CHARACTERISTICS

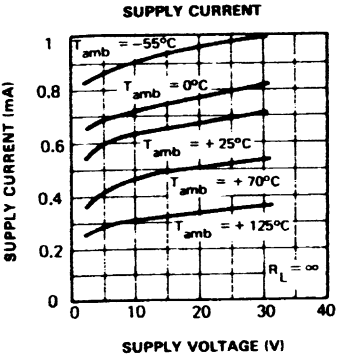
V_{CC}^+ = +5V, V_{CC}^- = GND, T_{amb} = 25°C (unless otherwise specified)

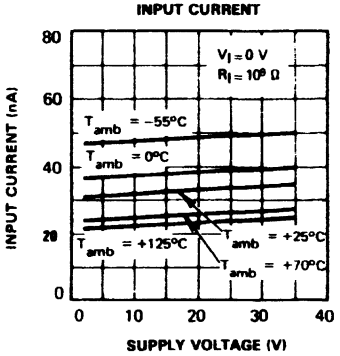
Symbol	Parameter	LM139A - LM239A LM339A			LM139 - LM239 LM339 - LM2901			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage – (note 2) T_{amb} = +25°C LM2901 $T_{min.} \le T_{amb} \le T_{max.}$ LM2901		1	2 4		1	5 7 9 15	mV
I_{io}	Input Offset Current T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$		3	25 100		5	50 150	nA
I_{ib}	Input Bias Current (I_I^+ or I_I^-) - (note 3) T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$		25	100 300		25	250 400	nA
A_{vd}	Large Signal Voltage Gain (V_{CC} = 15V, R_L =15kΩ, V_O = 1 to 11V) LM2901	50	200		50 25	200		V/mV
I_{CC}	Supply Current (all comparators) V_{CC} = +5V, no load V_{CC} = +30V, no load		1.1 1.3	2 2.5		1.1 1.3	2 2.5	mA
V_{icm}	Input Common Mode Voltage Range - (note 4) (V_{CC} = 30V) T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$	0 0		V_{CC}^+-1.5 V_{CC}^+ -2	0 0		V_{CC}^+-1.5 V_{CC}^+ -2	V
V_{id}	Differential Input Voltage - (note 6)			V_{CC}^+			V_{CC}^+	V
V_{OL}	Low Level Output Voltage (V_{id} = -1V, I_{sink} = 4mA) T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$		250	400 700		250	400 700	mV
I_{OH}	High Level Output Current (V_{id} = 1V) (V_{CC} = V_O = 30V) T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$		0.1	 1		0.1	 1	nA µA
I_{sink}	Output Sink Current (V_{id} = -1V, V_O = 1.5V)	6	16		6	16		mA
t_{re}	Response Time – (note 5) (R_L = 5.1kΩ connected to V_{CC}^+, $V_{(ref)}$ = +1.4V)		1.3			1.3		µs
t_{rel}	Large Signal Response Time (R_L = 5.1kΩ connected to V_{CC}^+, e_I = TTL, $V_{(ref)}$ = +1.4V)		300			300		ns

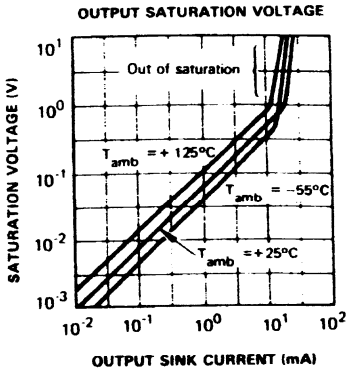
139-03.TBI

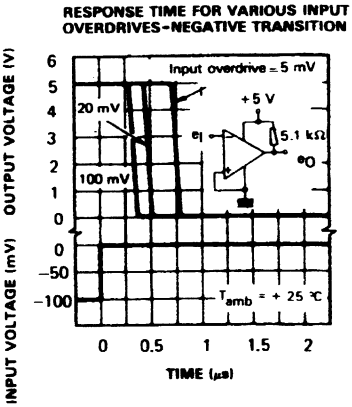
Notes :

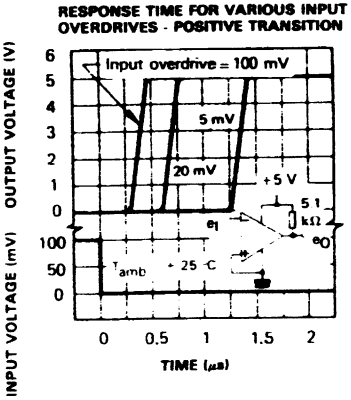
2. At output switch point, $V_O \approx$ 1.4V, R_S = 0 with V_{CC}^+ from 5Vto 30V, and over the full input common-mode range (0V to V_{CC}^+ –1.5V).
3. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading charge exists on the reference of input lines.
4. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V_{CC}^+ –1.5V, but either or both inputs can go to +30V without damage.
5. The response time specified is for a 100mV input step with 5mV overdrive. For larger overdrive signals 300ns can be obtained.
6. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than –0.3V (or 0.3V bellow the negative power supply, if used).


SUPPLY CURRENT
SUPPLY CURRENT (mA)
SUPPLY VOLTAGE (V)
T amb = −55°C
T amb = 0°C
T amb = + 25°C
T amb = + 70°C
T amb = + 125°C
R L = ∞
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40


INPUT CURRENT
INPUT CURRENT (nA)
SUPPLY VOLTAGE (V)
V I = 0 V
R I = 10⁹ Ω
T amb = −55°C
T amb = 0°C
T amb = +125°C
T amb = +25°C
T amb = +70°C
80
60
40
20
0
0
10
20
30
40


OUTPUT SATURATION VOLTAGE
SATURATION VOLTAGE (V)
OUTPUT SINK CURRENT (mA)
Out of saturation
T amb = + 125°C
T amb = −55°C
T amb = +25°C
10¹
10⁰
10⁻¹
10⁻²
10⁻³
10⁻²
10⁻¹
10⁰
10¹
10²

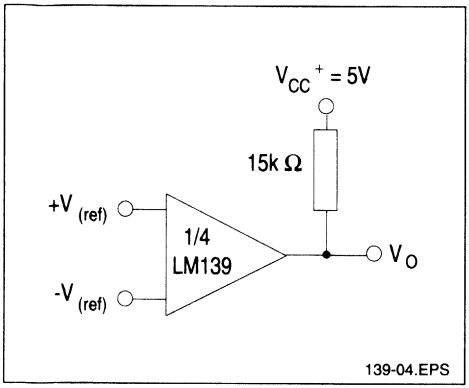

RESPONSE TIME FOR VARIOUS INPUT
OVERDRIVES-NEGATIVE TRANSITION
OUTPUT VOLTAGE (V)
INPUT VOLTAGE (mV)
TIME (µs)
Input overdrive = 5 mV
20 mV
100 mV
+5 V
5.1 kΩ
e I
e O
T amb = + 25 °C
6
5
4
3
2
1
0
0
−50
−100
0
0.5
1
1.5
2


RESPONSE TIME FOR VARIOUS INPUT
OVERDRIVES - POSITIVE TRANSITION
OUTPUT VOLTAGE (V)
INPUT VOLTAGE (mV)
TIME (µs)
Input overdrive = 100 mV
5 mV
20 mV
+5 V
5.1 kΩ
e I
e O
T amb = 25 °C
6
5
4
3
2
1
0
100
50
0
0
0.5
1
1.5
2

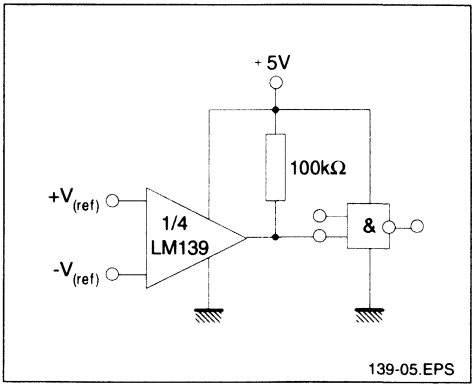
139-03.EPS

TYPICAL APPLICATIONS

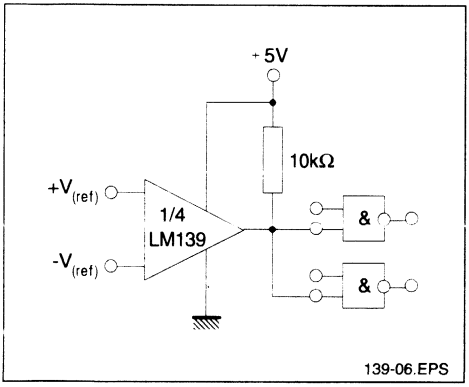
BASIC COMPARATOR



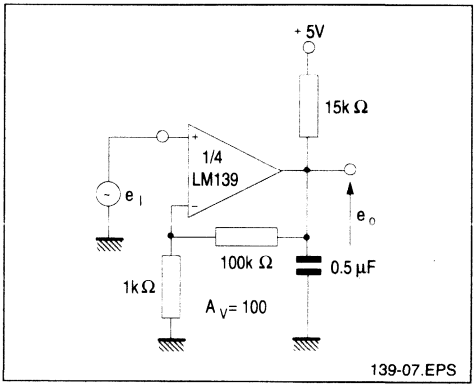
DRIVING CMOS



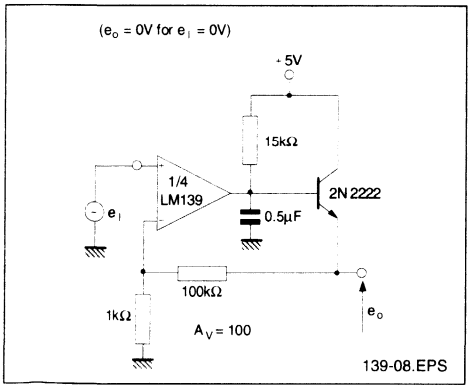
DRIVING TTL



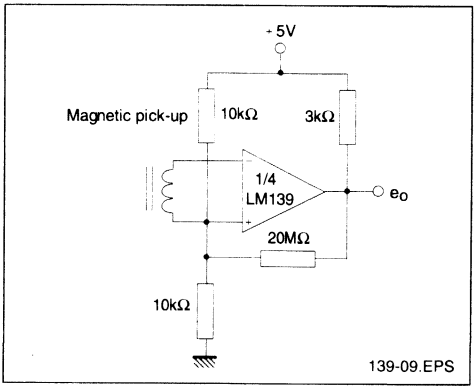
LOW FREQUENCY OP AMP



LOW FREQUENCY OP AMP

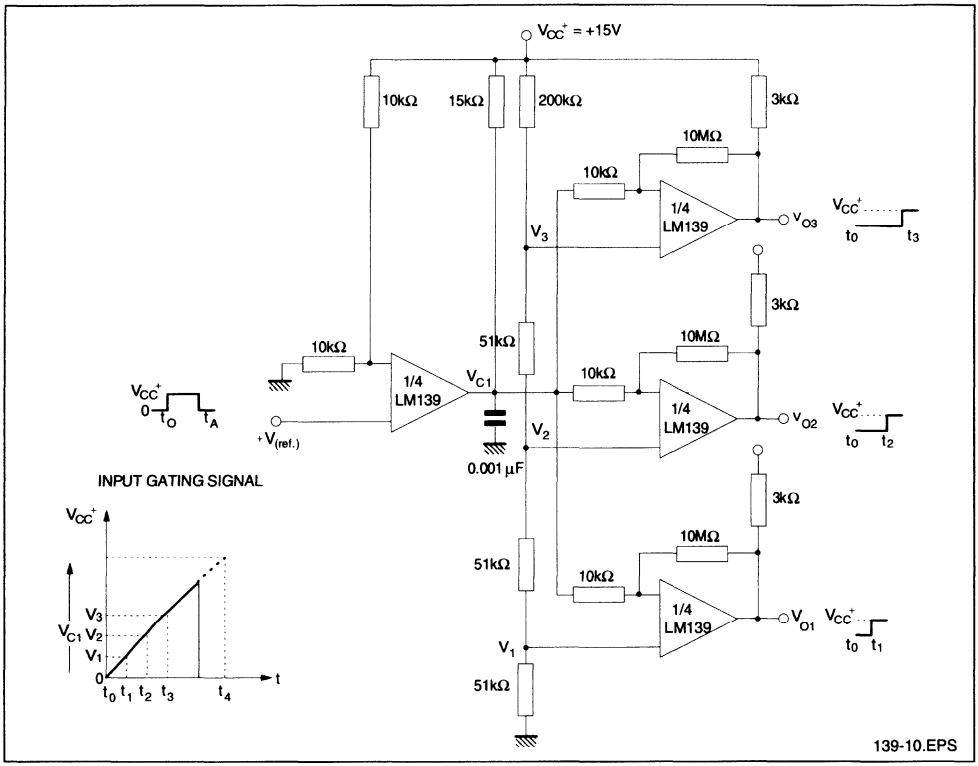


TRANSDUCER AMPLIFIER

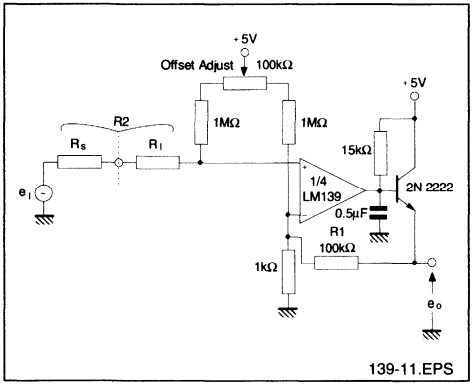


TYPICAL APPLICATIONS (continued)

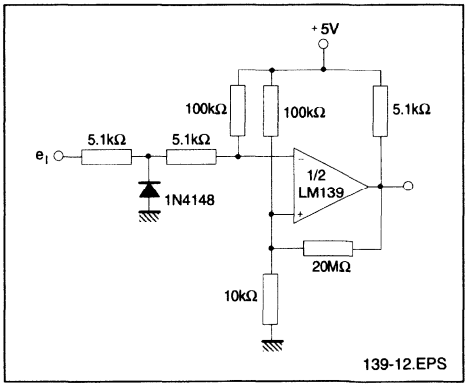
TIME DELAY GENERATOR



LOW FREQUENCY OP AMP WITH OFFSET ADJUST

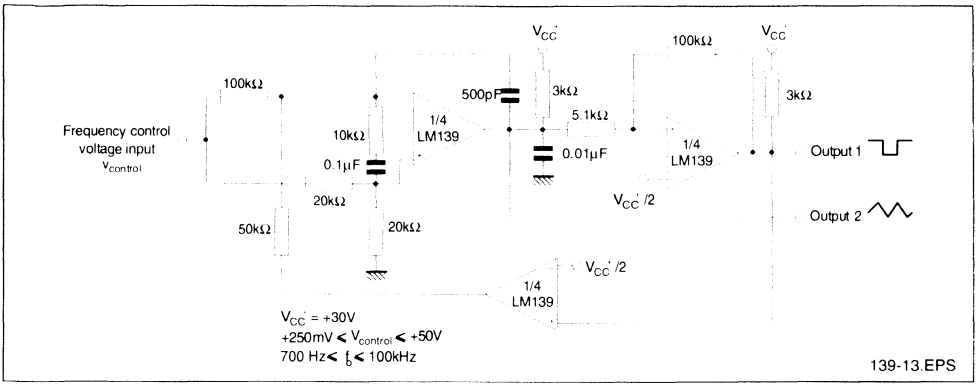


ZERO CROSSING DETECTOR (single power supply)

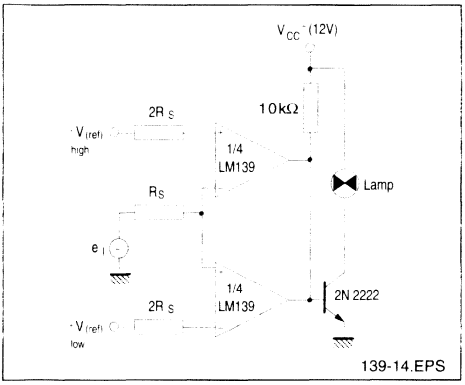


TYPICAL APPLICATIONS (continued)

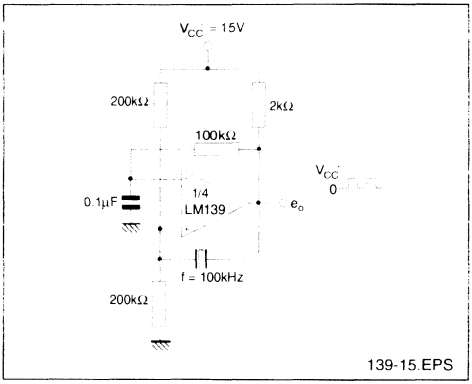
TWO-DECADE HIGH-FREQUENCY VCO



LIMIT COMPARATOR

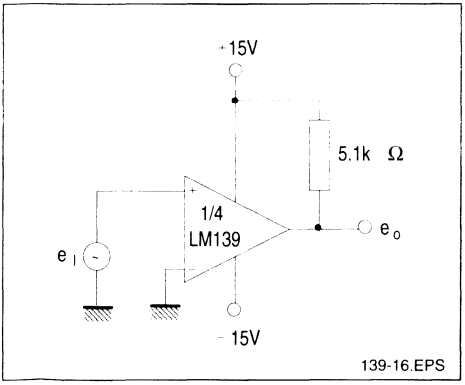


CRYSTAL CONTROLLED OSCILLATOR

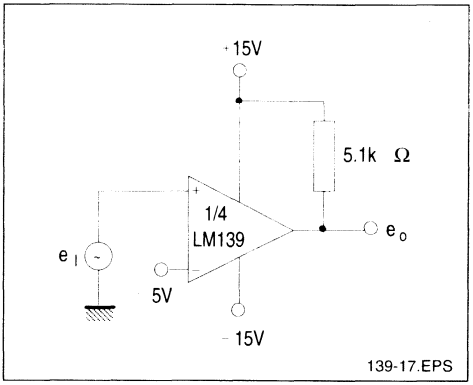


SPLIT-SUPPLY APPLICATIONS

ZERO CROSSING DETECTOR



COMPARATOR WITH A NEGATIVE REFERENCE

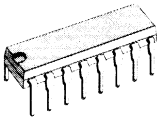


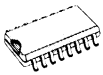
SGS-THOMSON MICROELECTRONICS

LM146
LM246 - LM346

PROGRAMMABLE QUAD BIPOLAR OPERATIONAL AMPLIFIERS

- PROGRAMMABLE ELECTRICAL CHARACTERISTICS
- BATTERY POWERED OPERATION
- LOW SUPPLY CURRENT (250µA/amplifier)
- GAIN-BANDWIDTH PRODUCT : 1MHz
- LARGE DC VOLTAGE GAIN : 120dB
- LOW NOISE VOLTAGE : 28nV/√Hz
- WIDE POWER SUPPLY RANGE : ±1.5V to ±22V
- CLASSE AB OUTPUT STAGE. NO CROSS-OVER DISTORTION
- OVERLOAD PROTECTION FOR INPUTS AND OUTPUTS





N
DIP16
(Plastic Package)
J
CERDIP16
(Cerdip Package)

D
SO16
(Plastic Micropackage)

ORDER CODES

Part Number	Temperature Range	Package		
		N	J	D
LM146	–55°C, +125°C	•	•	•
LM246	–40°C, +105°C	•	•	•
LM346	0°C, +70°C	•	•	•

Examples : LM146J, LM246N

146-01.TBL

DESCRIPTION

The LM346 consists of four independent, high gain, internally compensated, low power programmable amplifiers. Two external resistors (R_{set}) allow the user to program the gain-bandwith product, slew rate, supply current, input bias current, input offset current and input noise. For example the user can trade-off supply current for bandwidth or optimize noise figure for a given source resistance. In a similar way other amplifier characteristics can be tailored to the application.

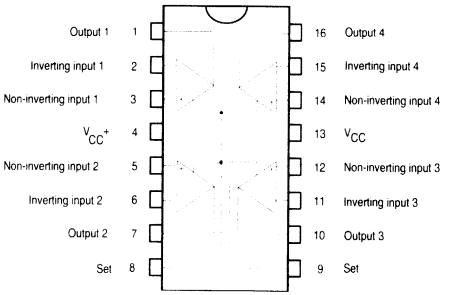
Except for the two programming pins at the end of the package the LM346 pin out is the same as the LM324 and LM348.

PROGRAMMING EQUATIONS :

Total supply current = 1mA (I_{set} = 10µA)
Gain-bandwidth product = 1MHz (I_{set} = 10µA)
Slew rate = 0.5V/µs (I_{set} = 10µA)
Input bias current ≈30 nA (I_{set} = 10µA)
I_{set} = current into pin 8 and pin 9
(see schematic diagram)

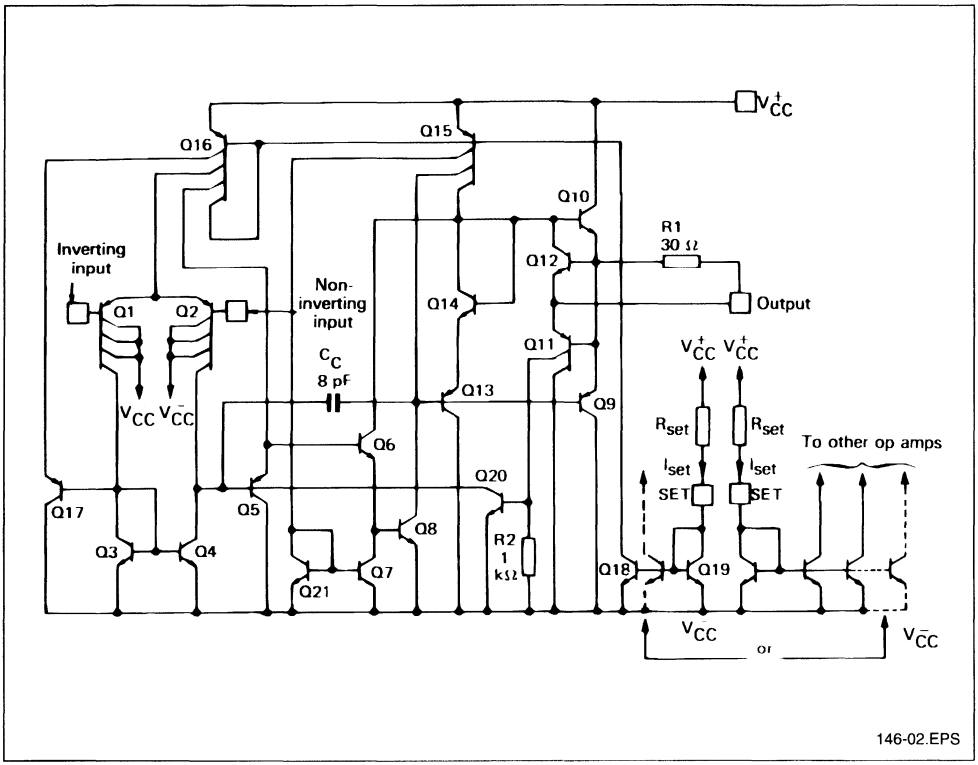
$$I_{set} = \frac{V_{CC}^{+} - V_{CC}^{-} - 0.6V}{R_{set}}$$

PIN CONNECTIONS (top view)



146-01.EPS

SCHEMATIC DIAGRAM (1/4 LM146)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	LM146	LM246	LM346	Unit
V_{CC}	Supply Voltage	±22	±22	±22	V
V_i	Input Voltage - (note 1)	±15	±15	±15	V
V_{id}	Differential Input Voltage	±30	±30	±30	V
	Output Short-circuit Duration - (note 2)	Infinite			
P_{tot}	Power Dissipation N/D Suffix J Suffix		500 900		mW
T_{oper}	Operating Free-air Temperature Range	–55 to +125	–40 to +105	0 to +70	°C
T_{stg}	Storage Temperature Range	–65 to +150	–65 to +150	–65 to +150	°C

Notes : 1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Any of the amplifier outputs can be shorted to ground indefinitly ; however more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

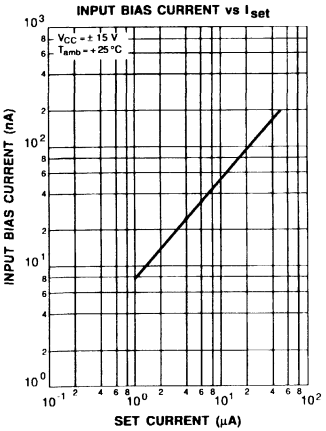
146-02 TBI

ELECTRICAL CHARACTERISTICS

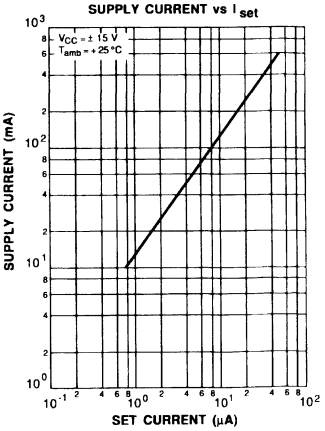
V_{CC} = ±15V, I_{set} = 10µA, T_{amb} = +25°C (unless otherwise specified)

Symbol	Parameter	LM146			LM246 - LM346			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage ($R_S \leq 10k\Omega$) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		0.5	3 5		0.5	5 6	mV
I_{io}	Input Offset Current T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		2	20 25		2	100 100	nA
I_{ib}	Input Bias Current T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		30	100 100		30	250 250	nA
A_{vd}	Large Signal Voltage Gain (V_o = ±10V, R_L = 10kΩ) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	100 50	1000		50 25	1000		V/mV
SVR	Supply Voltage Rejection Ratio ($R_S \leq 10k\Omega$) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	80 80	110		80 80	110		dB
I_{CC}	Supply Current, all Amp, no Load T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		1	2 2		1	2 2	mA
V_{icm}	Input Common Mode Voltage Range T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	±13.5 ±13.5			±13.5 ±13.5			V
CMR	Common Mode Rejection Ratio ($R_S \leq 10k\Omega$) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	80 70	110		80 70	110		dB
I_{OS}	Output Short-circuit Current T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	10 4	20	30 35	10 4	20	30 35	mA
± V_{opp}	Output Voltage Swing (R_L = 10kΩ) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	12 12	14		12 12	14		V
SR	Slew Rate (V_I = ±10V, R_L = 10kΩ, C_L = 100pF, T_{amb} = 25°C, unity Gain)	0.3	0.5		0.3	0.5		V/µs
R_I	Input Resistance		1			1		MΩ
C_I	Input Capacitance		2			2		pF
V_{o1}/V_{o2}	Channel Separation (R_L = 10kΩ, V_o = 12V_{pp})		120			120		dB
GBP	Gain Bandwidth Product (V_I = 10 mV, R_L = 10kΩ, C_L = 100pF f = 100kHz, T_{amb} = 25°C)	0.8	1		0.5	1		MHz
THD	Total Harmonic Distortion (f = 1kHz, A_v = 20dB, R_L = 10kΩ C_L = 100pF, T_{amb} = 25°C, v_o = 2V_{pp})		0.015			0.015		%
e_n	Equivalent Input Noise Voltage (f = 1kHz, R_s = 100Ω)		28			28		$\frac{nV}{\sqrt{Hz}}$

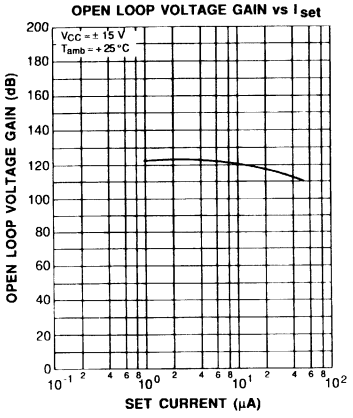
146-03.TBL



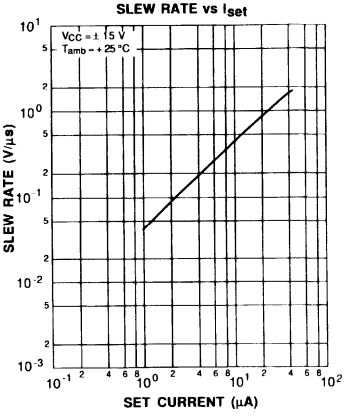
146-03.EPS



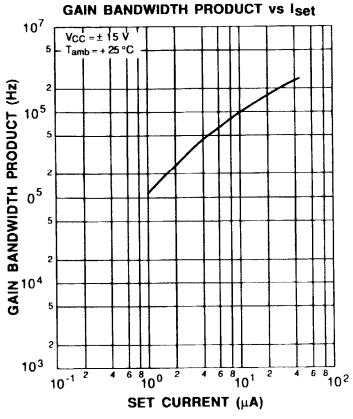
146-04.EPS



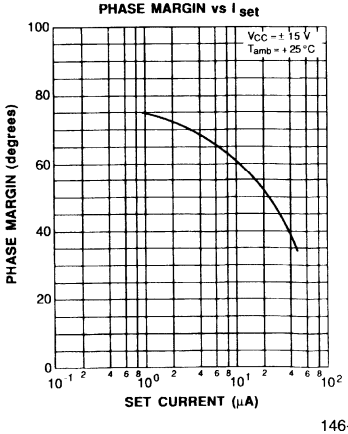
146-05.EPS



146-06.EPS

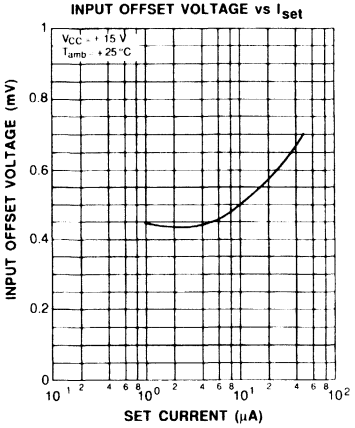


146-07.EPS



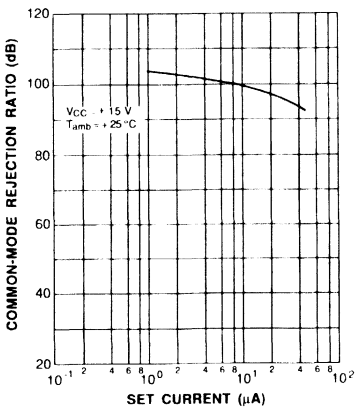
146-08.EPS

INPUT OFFSET VOLTAGE vs I_{set}



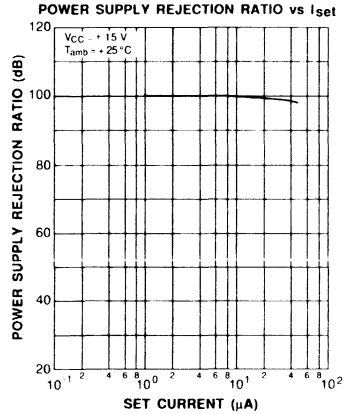
146-09.EPS

COMMON-MODE REJECTION RATIO vs I_{set}



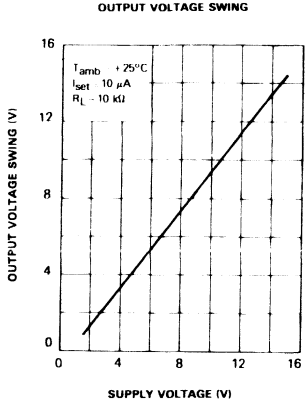
146-10.EPS

POWER SUPPLY REJECTION RATIO vs I_{set}



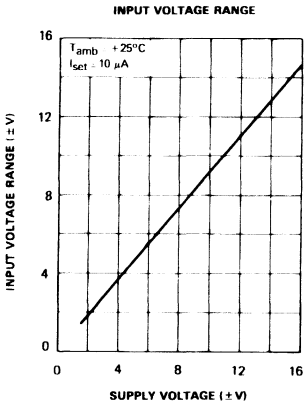
146-11 EPS

OUTPUT VOLTAGE SWING



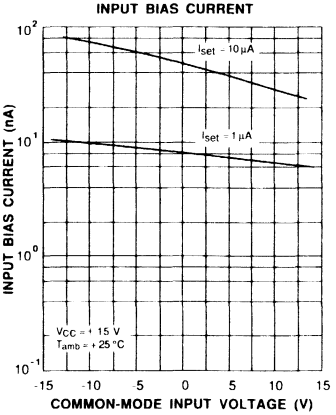
146-12.EPS

INPUT VOLTAGE RANGE



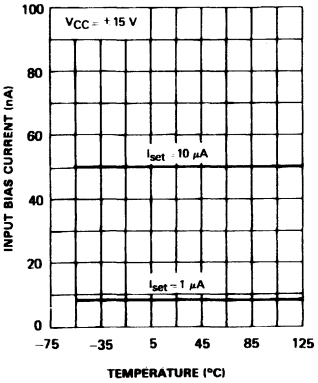
146-13.EPS

INPUT BIAS CURRENT



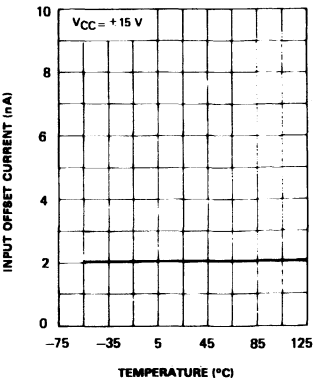
146-14.EPS

INPUT BIAS CURRENT vs TEMPERATURE



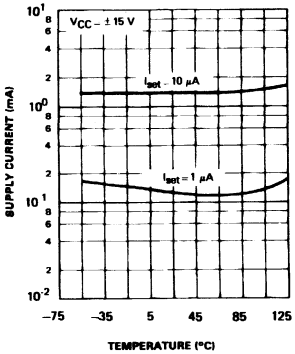
146-15.EPS

INPUT OFFSET CURRENT vs TEMPERATURE



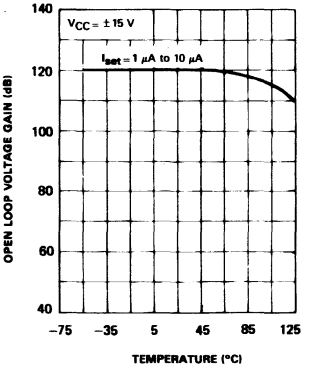
146-16.EPS

SUPPLY CURRENT vs TEMPERATURE



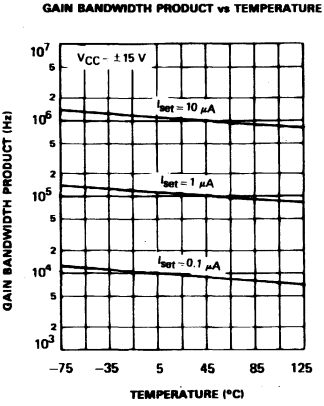
146-17.EPS

OPEN LOOP VOLTAGE GAIN vs TEMPERATURE



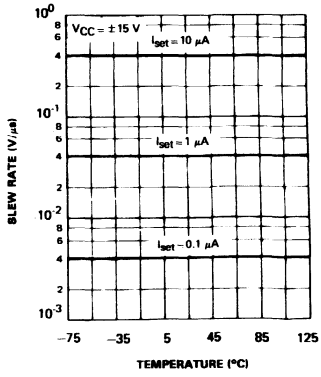
146-18.EPS

GAIN BANDWIDTH PRODUCT vs TEMPERATURE



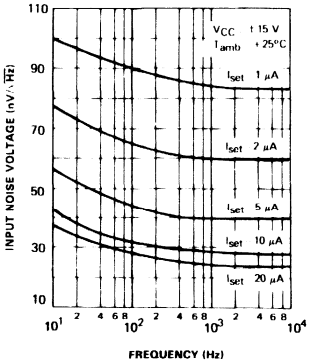
146-19.EPS

SLEW RATE vs TEMPERATURE



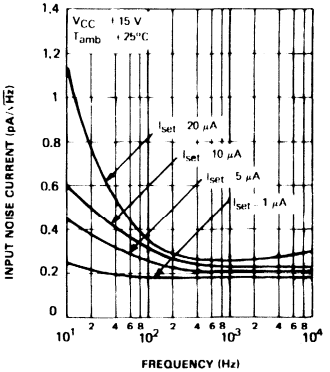
146-20.EPS

INPUT NOISE VOLTAGE vs FREQUENCY



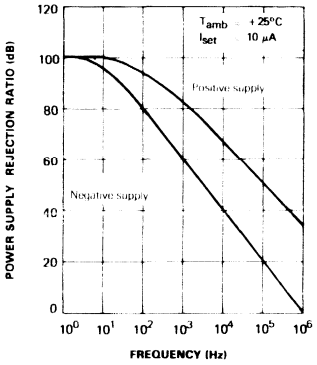
146-21.EPS

INPUT NOISE CURRENT vs FREQUENCY



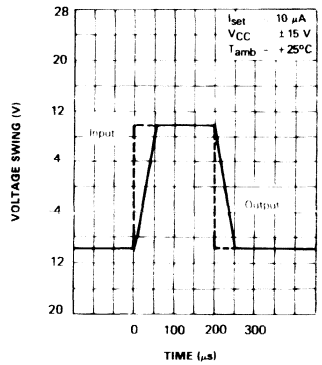
146-22.EPS

POWER SUPPLY REJECTION RATIO

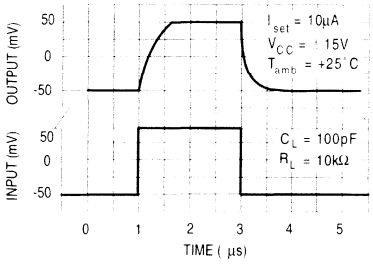


146-23.EPS

VOLTAGE FOLLOWER PULSE RESPONSE

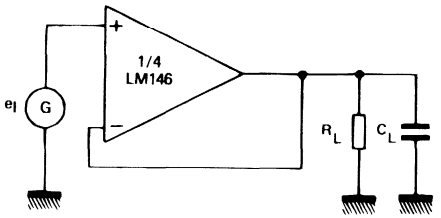


146-24.EPS



146-25.EPS

TRANSIENT RESPONSE TEST CIRCUIT



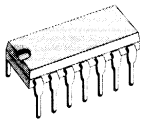
146-26.EPS

SGS-THOMSON MICROELECTRONICS

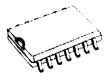
LM148
LM248 - LM348

FOUR UA741
QUAD BIPOLAR OPERATIONAL AMPLIFIERS

- LOW SUPPLY CURRENT : 0.53mA/AMPLIFIER
- CLASS AB OUTPUT STAGE : NO CROSS-OVER DISTORTION
- PIN COMPATIBLE WITH LM124
- LOW INPUT OFFSET VOLTAGE : 1mV
- LOW INPUT OFFSET CURRENT : 2nA
- LOW INPUT BIAS CURRENT : 30nA
- GAIN BANDWIDTH PRODUCT : 1.3MHz
- HIGH DEGREE OF ISOLATION BETWEEN AMPLIFIERS : 120dB
- OVERLOAD PROTECTION FOR INPUTS AND OUTPUTS



N
DIP14
(Plastic Package)



D
SO14
(Plastic Micropackage)

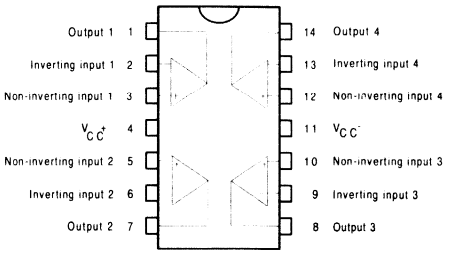
J
CERDIP14
(Cerdip Package)

ORDER CODES

Part Number	Temperature Range	Package		
		N	J	D
LM148	−55°C, +125°C	•	•	•
LM248	−40°C, +105°C	•	•	•
LM348	0°C, +70°C	•	•	•
Examples : LM148J, LM348D				

148-01.TBL

PIN CONNECTIONS (top view)



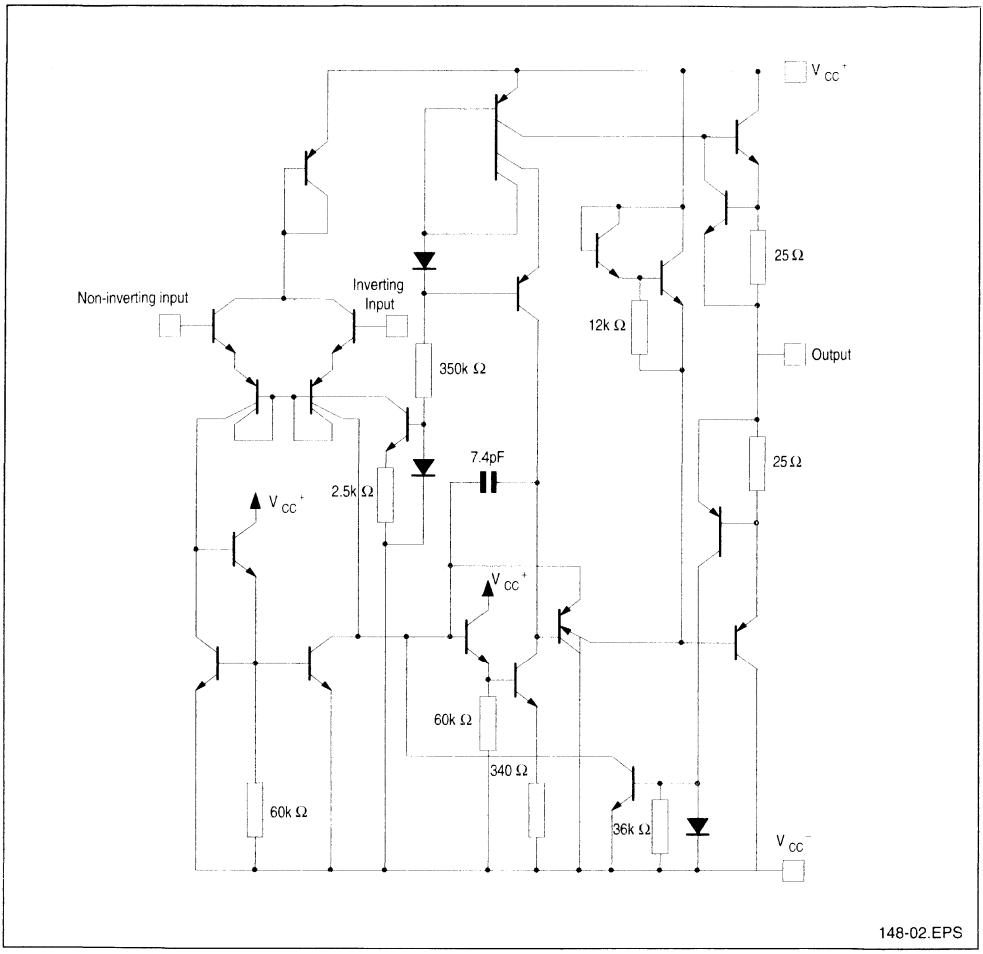
148-01.EPS

DESCRIPTION

The LM148 consists of four independent, high gain internally compensated, low power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar UA741 operational amplifier. In addition the total supply current for all four amplifiers is comparable to the supply current of a single UA741 type op amp. Other features include input offset current and input bias current which are much less than those of a standard UA741. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling.

The LM148 can be used anywhere multiple UA741 type amplifiers are being used and in applications where amplifier matching or high packing density is required.

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	LM148	LM248	LM348	Unit
V_{CC}	Supply Voltage	± 22	± 22	± 22	V
V_{id}	Differential Input Voltage	±44	± 44	± 44	V
V_i	Input Voltage (note 1)	± 22	± 22	± 22	V
P_{tot}	Power Dissipation	500	500	500	mW
	Output Short-circuit Duration (note 2)		Infinite		
T_{oper}	Operating Free-air Temperature Range	−55, +125	−40, +105	0, +70	°C
T_{stg}	Storage Temperature Range	−65, +150	−65, +150	−65, +150	°C

148-02.TBL

Notes : 1. For supply voltage less than maximum value, the absolute maximum input voltage is equal to the supply voltage.
2. Any of the amplifier outputs can be shorted to ground indefinitely ; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

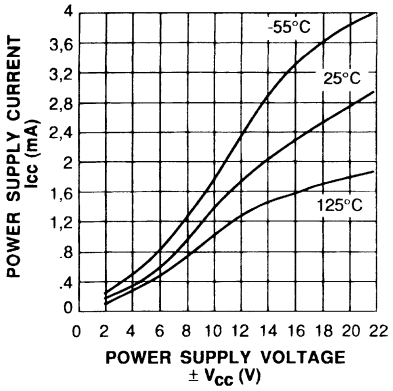
ELECTRICAL CHARACTERISTICS

V_{CC} = ±15V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	LM148 - LM248 - LM348			Unit
		Min.	Typ.	Max.	
V_{io}	Input Offset Voltage ($R_S \leq 10k\Omega$) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		1	5 6	mV
I_{io}	Input Offset Current T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		2	25 75	nA
I_{ib}	Input Bias Current T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		30	100 300	nA
A_{vd}	Large Signal Voltage Gain (V_o = ±10V, R_L = 2kΩ) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	50 25	160		V/mV
SVR	Supply Voltage Rejection Ratio ($R_S \leq 10k\Omega$) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	77 77	100		dB
I_{CC}	Supply Current, all Amp, no Load T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		2.1	3.6 4.8	mA
V_{icm}	Input Common Mode Voltage Range T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	±12 ±12			V
CMR	Common Mode Rejection Ratio ($R_S \leq 10k\Omega$) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	70 70	110		dB
I_{OS}	Output Short-circuit Current T_{amb} = 25°C	10	25	35	mA
± V_{opp}	Output Voltage Swing T_{amb} = 25°C R_L = 10kΩ R_L = 2kΩ $T_{min.} \leq T_{amb} \leq T_{max.}$ R_L = 10kΩ R_L = 2kΩ	12 10 12 10	13 12		V
SR	Slew Rate (V_I = ±10V, R_L = 10kΩ, C_L = 100pF, T_{amb} = 25°C, unity Gain)	0.25	0.5		V/µs
t_r	Rise Time (V_I = ±10V, R_L = 10kΩ, C_L = 100pF, T_{amb} = 25°C, unity Gain)		0.3		µs
K_{OV}	Overshoot (V_I = ±10V, R_L = 10kΩ, C_L = 100pF, T_{amb} = 25°C, unity Gain)		5		%
R_I	Input Resistance	0.8	2.5		MΩ
GBP	Gain Bandwidth Product (V_I = 10 mV, R_L = 10kΩ, C_L = 100pF, f = 100kHz, T_{amb} = 25°C)	0.7	1.3		MHz
THD	Total Harmonic Distortion (f = 1kHz, A_v = 20dB, R_L = 10kΩ, C_L = 100pF, T_{amb} = 25°C, v_o = $2V_{pp}$)		0.08		%
e_n	Equivalent Input Noise Voltage (f = 1kHz, R_s = 100Ω)		40		$\frac{nV}{\sqrt{Hz}}$
V_{o1}/V_{o2}	Channel Separation		120		dB

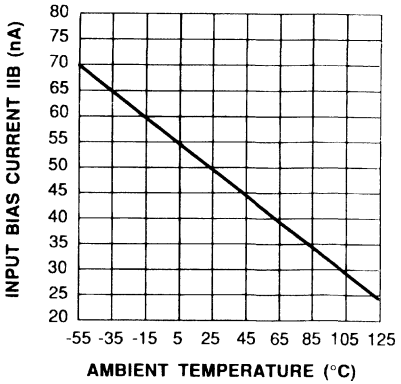
148-03.TBL

POWER SUPPLY CURRENT vs POWER SUPPLY VOLTAGE



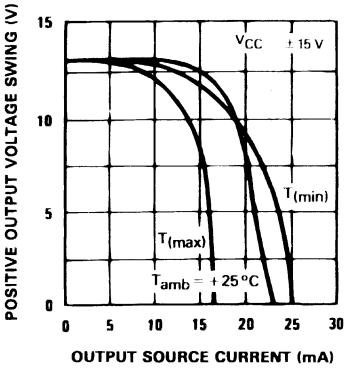
148-03.EPS

INPUT BIAS CURRENT vs AMBIENT TEMPERATURE



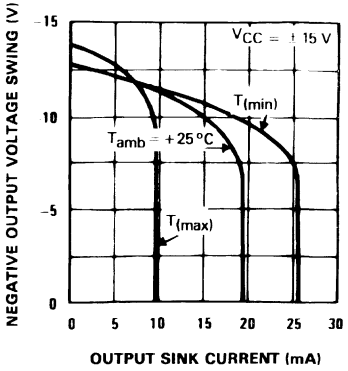
148-04.EPS

POSITIVE CURRENT LIMIT



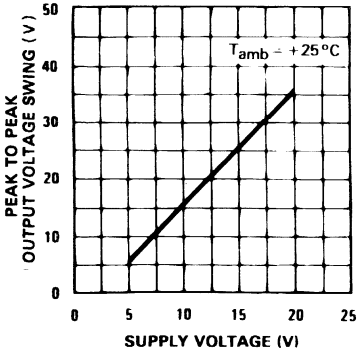
148-05.EPS

NEGATIVE CURRENT LIMIT



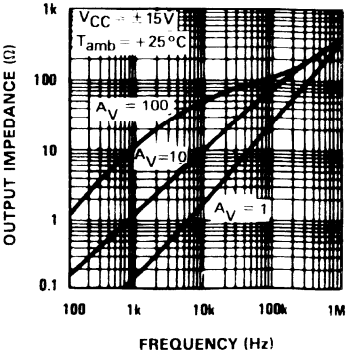
148-06.EPS

OUTPUT VOLTAGE SWING



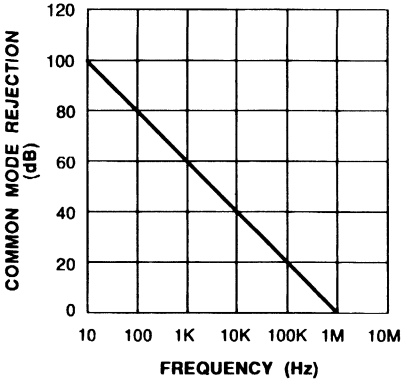
148-07.EPS

OUTPUT IMPEDANCE



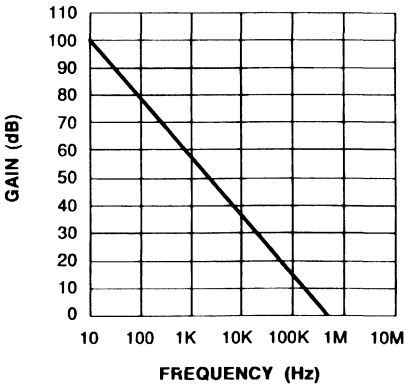
148-08.EPS

COMMON MODE REJECTION RATIO vs FREQUENCY



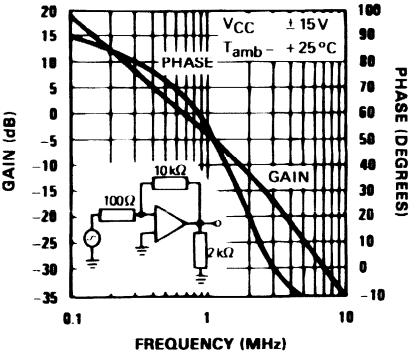
148-09.EPS

OPEN LOOP FREQUENCY RESPONSE



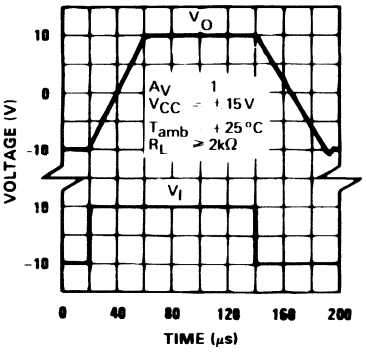
148-10.EPS

BODE PLOT (LM148)



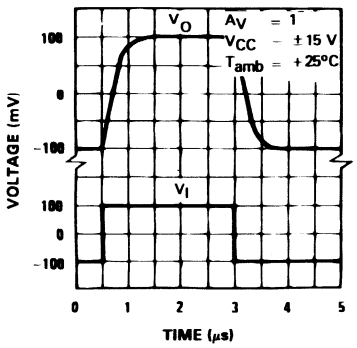
148-11.EPS

LARGE SIGNAL PULSE RESPONSE (LM148)



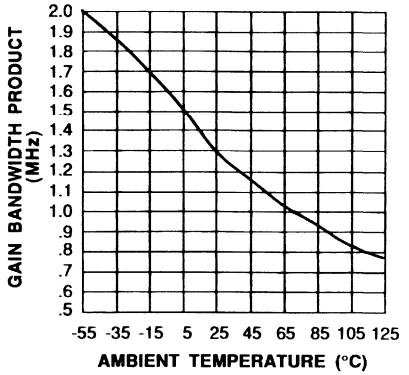
148-12.EPS

SMALL SIGNAL PULSE RESPONSE (LM148)



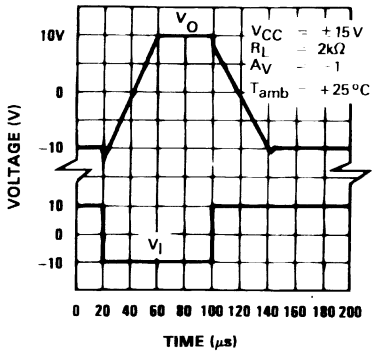
148-13.EPS

GAIN BANDWIDTH PRODUCT vs AMBIENT TEMPERATURE



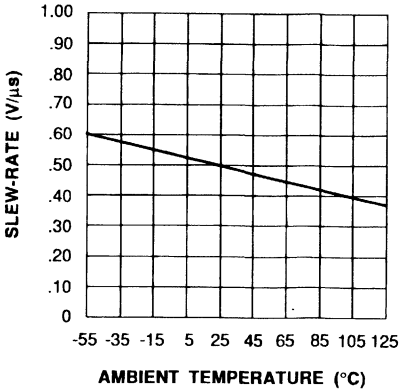
148-14.EPS

INVERTING LARGE SIGNAL PULSE RESPONSE (LM148)



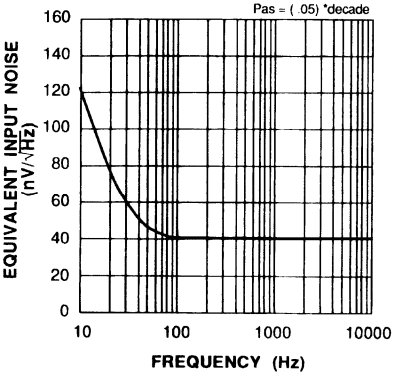
148-15.EPS

SLEW-RATE vs TEMPERATURE



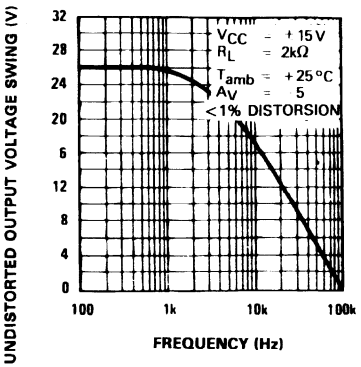
148-16.EPS

EQUIVALENT INPUT NOISE vs FREQUENCY



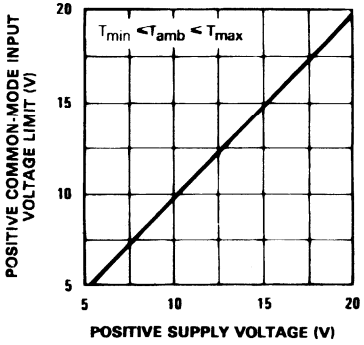
148-17.EPS

UNDISTORTED OUTPUT VOLTAGE SWING



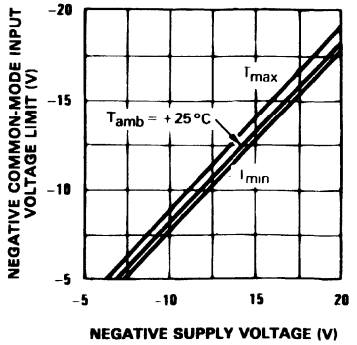
148-18.EPS

POSITIVE COMMON-MODE INPUT VOLTAGE LIMIT

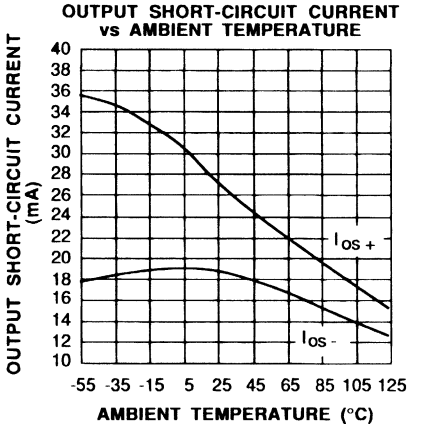


148-19.EPS

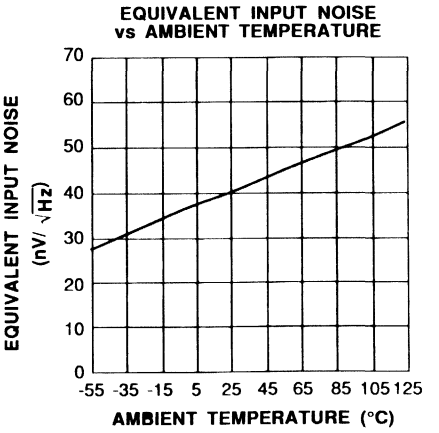
NEGATIVE COMMON-MODE INPUT VOLTAGE LIMIT



148-20.EPS

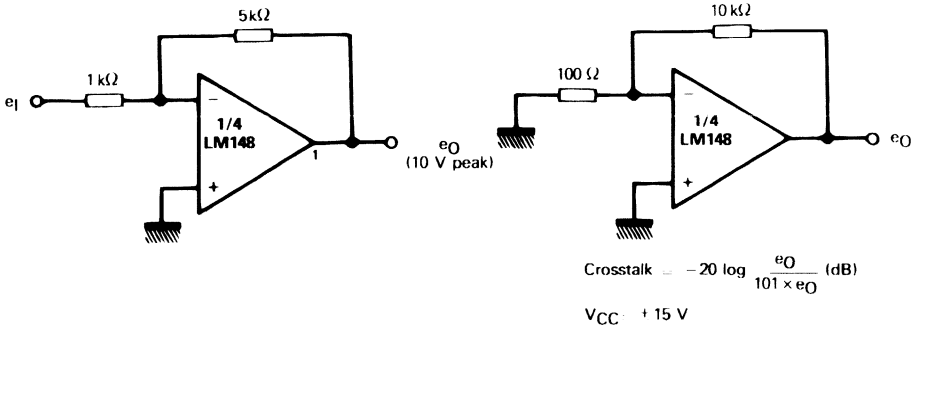


148-21.EPS



148-22.EPS

TEST CIRCUITS



148-23.EPS

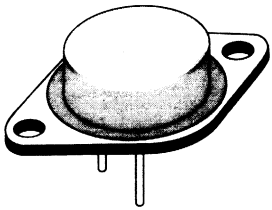
SGS-THOMSON
MICROELECTRONICS

LM150/250
LM350

THREE-TERMINAL 3 A ADJUSTABLE VOLTAGE REGULATORS

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST/1)

- GUARANTEED 3A OUTPUT CURRENT
- ADJUSTABLE OUTPUT DOWN TO 1.2V
- LINE REGULATION TYPICALLY 0.005% /V
- LOAD REGULATION TYPICALLY 0.1%
- GUARANTEED THERMAL REGULATION
- CURRENT LIMIT CONSTANT WITH TEMPERATURE
- STANDARD 3-LEAD TRANSISTOR PACKAGE

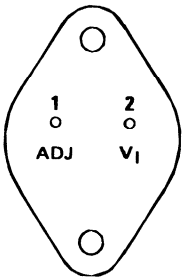


TO3
K SUFFIX
(Steel Can)

ORDER CODE

PART NUMBER	TEMPERATURE RANGE	PACKAGE
		K
LM150	-55 °C to + 150 °C	•
LM250	-25 °C to + 150 °C	•
LM350	0 °C to + 125 °C	•
EXAMPLE: LM150K		

PIN CONNECTION
(bottom view)

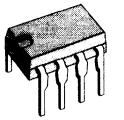


Case is output

LM158/A - LM258/A LM358/A - LM2904

LOW POWER DUAL OPERATIONAL AMPLIFIERS

- INTERNALLY FREQUENCY COMPENSATED
- LARGE DC VOLTAGE GAIN : 100dB
- WIDE BANDWIDTH (unity gain) : 1.1MHz (temperature compensated)
- VERY LOW SUPPLY CURRENT/AMPLI (500µA) - ESSENTIALLY INDEPENDENT OF SUPPLY VOLTAGE
- LOW INPUT BIAS CURRENT : 20nA (temperature compensated)
- LOW INPUT OFFSET VOLTAGE : 2mV
- LOW INPUT OFFSET CURRENT : 2nA
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GROUND
- DIFFERENTIAL INPUT VOLTAGE RANGE EQUAL TO THE POWER SUPPLY VOLTAGE
- LARGE OUTPUT VOLTAGE SWING 0V TO (V_{CC} – 1.5V)



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

J
CERDIP8
(Cerdip Package)

H
TO99
(Metal Can)

ORDER CODES

Part Number	Temperature Range	Package			
		H	N	J	D
LM158/A	–55°C, +125°C	•	•	•	•
LM258/A	–40°C, +105°C	•	•	•	•
LM358/A	0°C, +70°C	•	•	•	•
LM2904	–40°C, +105°C	•	•	•	•

Examples : LM158H, LM258N, LM2904D

158-01.TBL

DESCRIPTION

These circuits consist of two independent, high gain, internally frequency compensated which were designed specifically to operate from a single power supply over a wide range of voltages. The low power supply drain is independent of the magnitude of the power supply voltage.

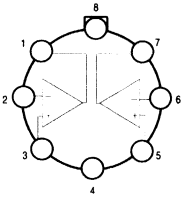
Application areas include transducer amplifiers, dc gain blocks and all the conventional op-amp circuits which now can be more easily implemented in single power supply systems. For example, these circuits can be directly operated off the standard + 5V power supply voltage which is used in logic systems and will easily provide the required interface electronics without requiring any additional power supply.

In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

The gain-bandwidth product is temperature compensated.

PIN CONNECTIONS (top views)

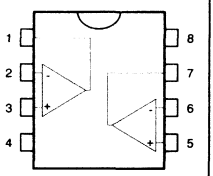
TO99



158-01.EPS

1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^-

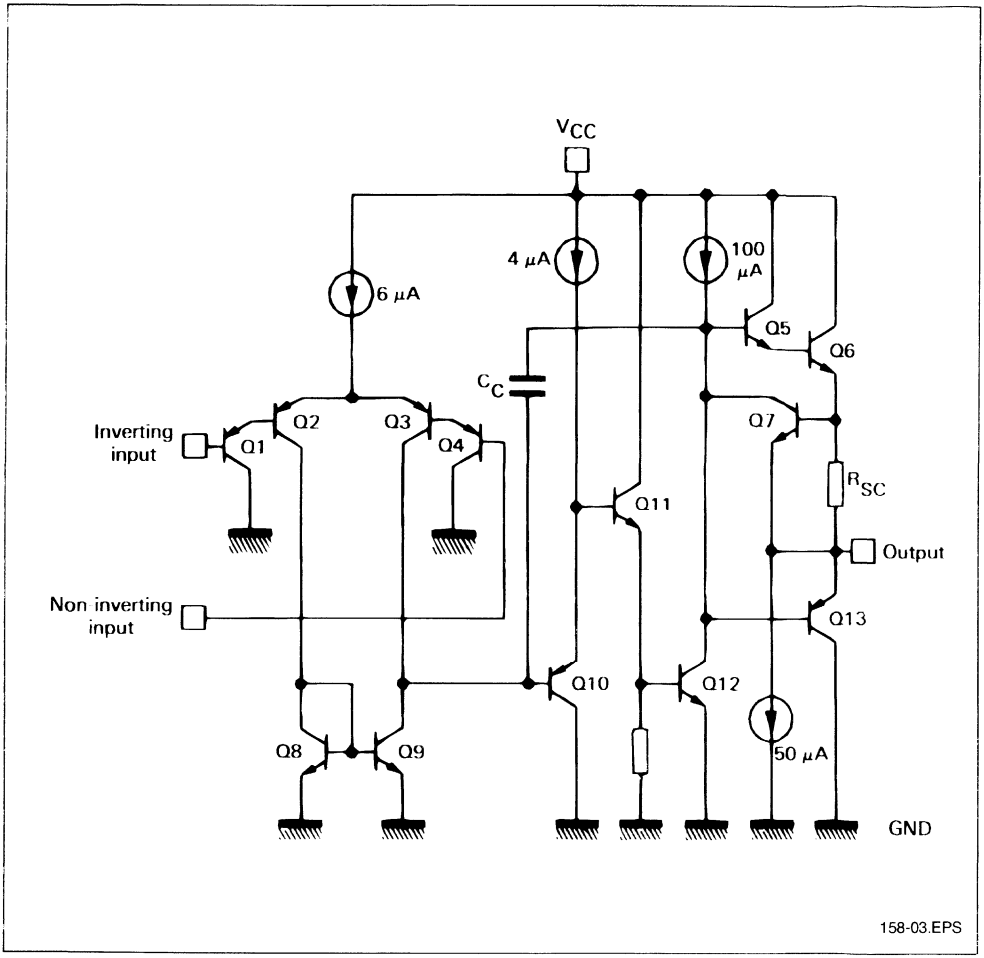
DIP8/CERDIP8
SO8



158-02.EPS

5 - Non-inverting input 2
6 - Inverting input 2
7 - Ouput 2
8 - V_{CC}^+

SCHEMATIC DIAGRAM (1/2 LM158)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	LM158,A	LM258,A LM2904	LM358,A	Unit
V_{CC}	Supply Voltage	+32	+32	+32	V
V_i	Input Voltage	–0.3 to +32	–0.3 to +32	–0.3 to +32	V
V_{id}	Differential Input Voltage	+32	+32	+32	V
	Output Short-circuit Duration - (note 2)		Infinite		
P_{tot}	Power Dissipation	500	500	500	mW
I_{in}	Input Current - (note 1)	50	50	50	mA
T_{oper}	Operating Free-air Temperature Range	–55 to +125	–40 to +105	0 to +70	°C
T_{stg}	Storage Temperature Range	–65 to +150	–65 to +150	–65 to +150	°C

ELECTRICAL CHARACTERISTICS

V_{CC}^+ = +5V, V_{CC}^- = Ground, V_O = 1.4V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	LM158A LM258A LM358A			LM158 - LM258 LM358 - LM2904			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage - (note 3) T_{amb} = 25°C LM158, LM258 LM158A $T_{min.} \le T_{amb} \le T_{max.}$ LM158, LM258		1	3 2 4		2	7 5 9 7	mV
I_{io}	Input Offset Current T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$		2	10 30		2	30 40	nA
I_{ib}	Input Bias Current - (note 4) T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$		20	50 100		20	150 200	nA
A_{vd}	Large Signal Voltage Gain (V_{CC} = +15V, R_L = 2kΩ, V_O = 1.4V to 11.4V) T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$	50 25	100		50 25	100		V/mV
SVR	Supply Voltage Rejection Ratio (R_S = 10kΩ) (V_{CC}^+ = 5 to 30V) T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$	65 65	100		65 65	100		dB
I_{CC}	Supply Current, all Amp, no Load V_{CC} = +5V, $T_{min.} \le T_{amb} \le T_{max.}$ V_{CC} = +30V, $T_{min.} \le T_{amb} \le T_{max.}$		0.7	1.2 2		0.7	1.2 2	mA
V_{icm}	Input Common Mode Voltage Range (V_{CC} = +30V) - (note 6) T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$	0 0		V_{CC}^+–1.5 V_{CC}^+–2	0 0		V_{CC}^+–1.5 V_{CC}^+–2	V
CMR	Common-mode Rejection Ratio (R_S = 10kΩ) T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$	70 60	85		70 60	85		dB
I_O	Output Short Circuit Current (V_{CC} = +15V, V_o = 2V, V_{id} = +1V)	20	40	60	20	40	60	mA
I_{sink}	Output Current Sink (V_{id} = -1V) V_{CC} = +15V, V_O = 2V V_{CC} = +15V, V_O = +0.2V	10 12	20 50		10 12	20 50		mA µA
V_{OPP}	Output Voltage Swing (R_L = 2kΩ) T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$	0 0		V_{CC}^+–1.5 V_{CC}^+–2	0 0		V_{CC}^+–1.5 V_{CC}^+–2	V
V_{OH}	High Level Output Voltage (V_{CC}^+ = 30V) T_{amb} = 25°C R_L = 2kΩ $T_{min.} \le T_{amb} \le T_{max.}$ T_{amb} = 25°C R_L = 10kΩ $T_{min.} \le T_{amb} \le T_{max.}$	26 26 27 27	27 28 		26 26 27 27	27 28 		V
V_{OL}	Low Level Output Voltage (R_L = 10kΩ) T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$		5	20 20		5	20 20	mV
SR	Slew Rate (V_{CC} = 15V, V_I = 0.5 to 3V, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)	0.3	0.6		0.3	0.6		V/µs

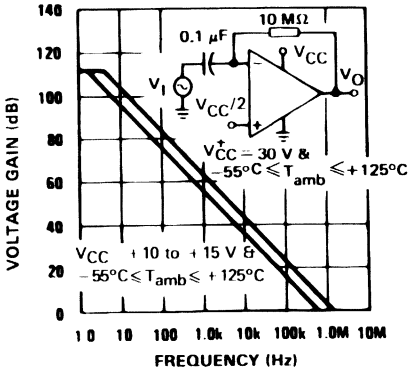
158-03.TBL

ELECTRICAL CHARACTERISTICS (continued)

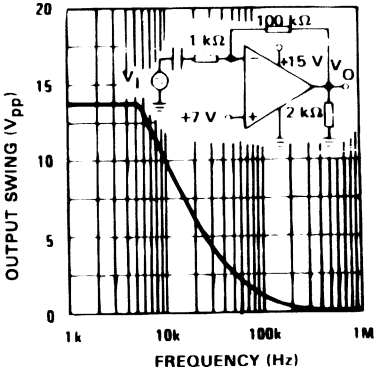
Symbol	Parameter	LM158A LM258A LM358A			LM158 - LM258 LM358 - LM2904			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
GBP	Gain Bandwidth Product (V_{CC} = 30V, f = 100kHz, T_{amb} = 25°C, V_{in} = 10mV, R_L = 2kΩ, C_L = 100pF)	0.7	1.1		0.7	1.1		MHz
THD	Total Harmonic Distortion (f = 1kHz, A_v = 20dB, R_L = 2kΩ, V_{CC} = 30V, C_L = 100pF, T_{amb} = 25°C, V_O = 2 PP)		0.02			0.02		%
e_n	Equivalent Input Noise voltage (f = 1kHz, R_s = 100Ω, V_{CC} = 30V)		55			55		$\frac{nV}{\sqrt{Hz}}$
DV_{io}	Input Offset Voltage Drift		7	15		7	30	µV/°C
DI_{io}	Input Offset Current Drift		10	200		10	300	pA/°C
V_{O1}/V_{O2}	Channel Separation (note 5) 1kHz ≤ f ≤ 20kHz		120			120		dB

Notes :
1. This input current only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also NPN parasitic action on the IC chip. This transistor action can cause the output voltages of the Op-amps to go to the V_{CC} voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative.
   This is not destructive and normal output will set up again for input voltage higher than –0.3V.
2. Short-circuits from the output to V_{CC} can cause excessive heating if $V_{CC}^+ > 15V$. The maximum output current is approximatively 40mA independent of the magnitude of V_{CC}. Destructive dissipation can result from simultaneous short-circuits on all amplifiers.
3. V_O = 1.4V, R_S = 0Ω, 5V < V_{CC}^+ < 30V, 0 < V_{ic} < V_{CC}^+ – 1.5V.
4. The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
5. Due to the proximity of external components insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequences.
6. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V_{CC}^+ – 1.5V.
   But either or both inputs can go to +32V without damage.

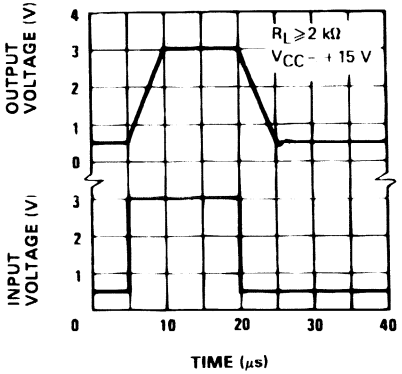
OPEN LOOP FREQUENCY RESPONSE (Note 3)



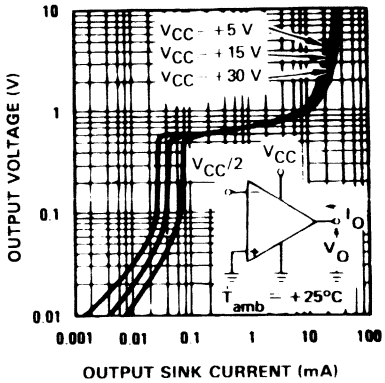
LARGE SIGNAL FREQUENCY RESPONSE



VOLTAGE FOLLOWER PULSE RESPONSE

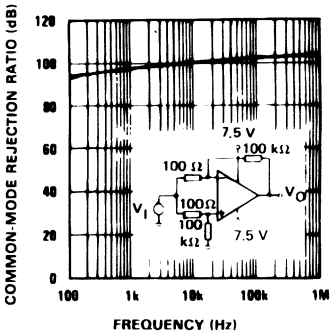


OUTPUT CHARACTERISTICS



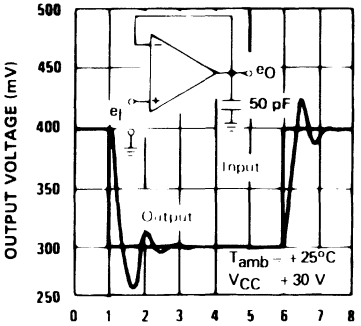
158-04.EPS

COMMON-MODE REJECTION RATIO

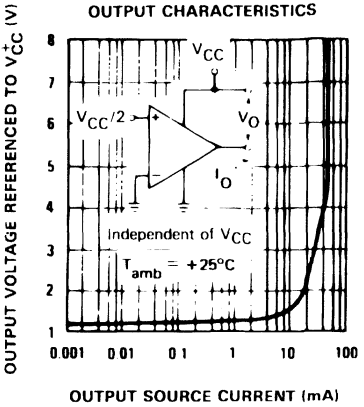


158-05.EPS

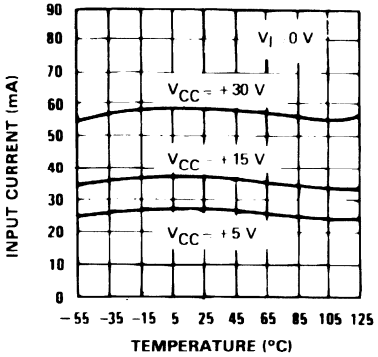
VOLTAGE FOLLOWER PULSE RESPONSE (SMALL SIGNAL)



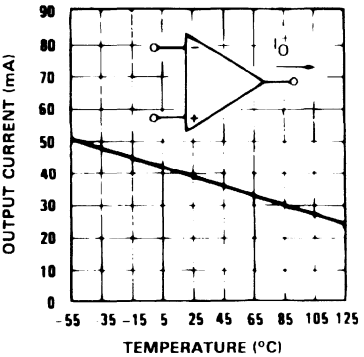
OUTPUT CHARACTERISTICS



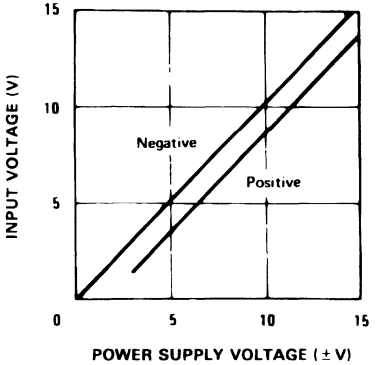
INPUT CURRENT (Note 1)



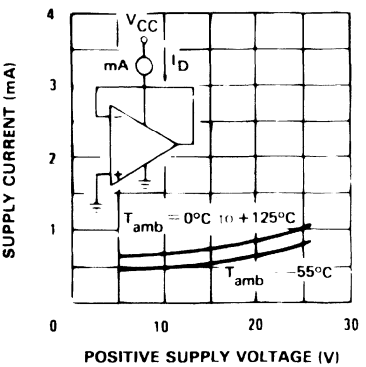
CURRENT LIMITING (Note 1)



INPUT VOLTAGE RANGE

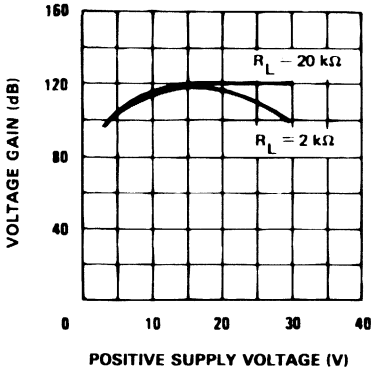


SUPPLY CURRENT



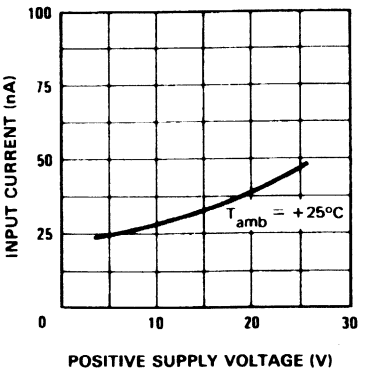
158-06.EPS

VOLTAGE GAIN



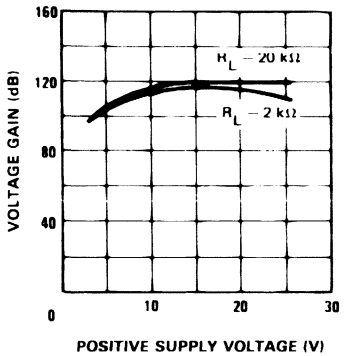
158-07.EPS

INPUT CURRENT



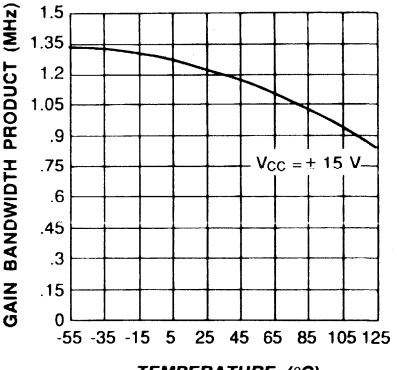
158-08.EPS

VOLTAGE GAIN



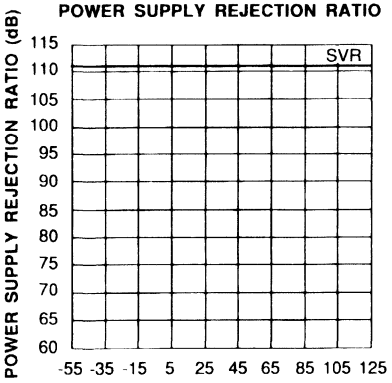
158-09.EPS

GAIN BANDWIDTH PRODUCT



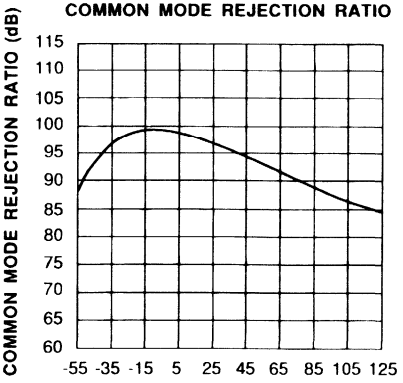
158-10.EPS

POWER SUPPLY REJECTION RATIO



158-11.EPS

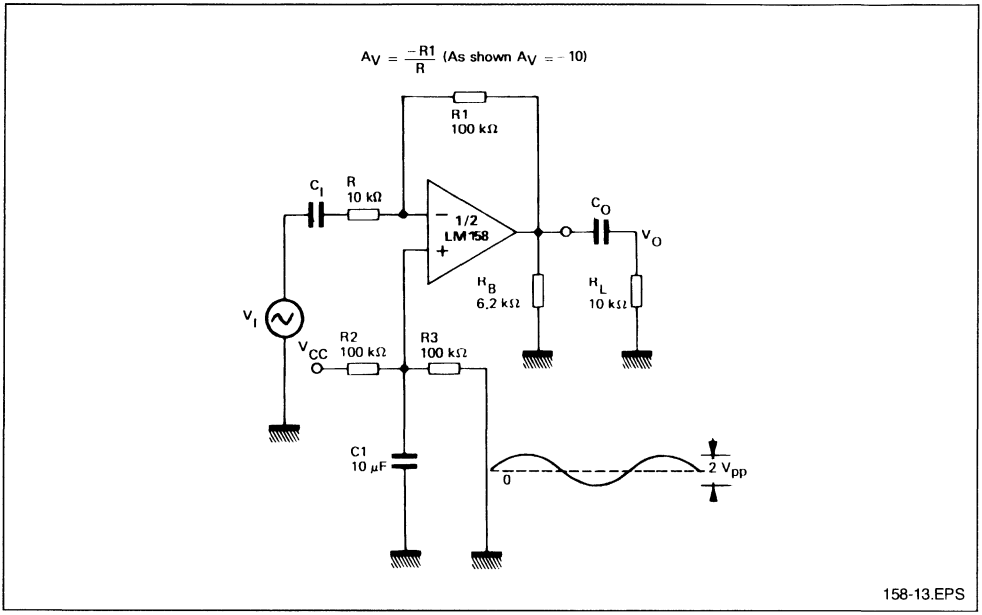
COMMON MODE REJECTION RATIO



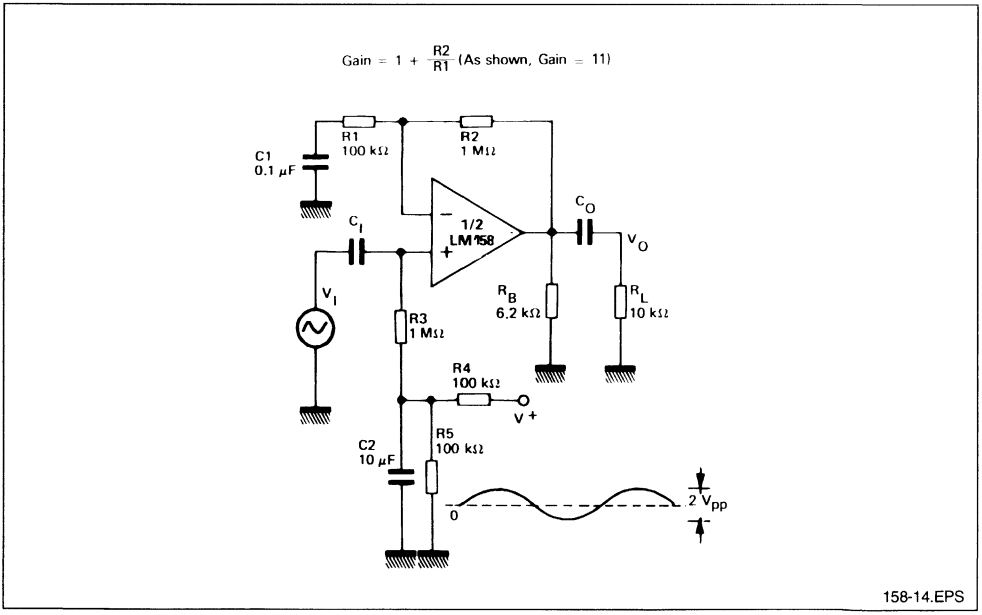
158-12.EPS

TYPICAL APPLICATIONS (single supply voltage) V_{CC} = +5V_{DC}

AC COUPLED INVERTING AMPLIFIER

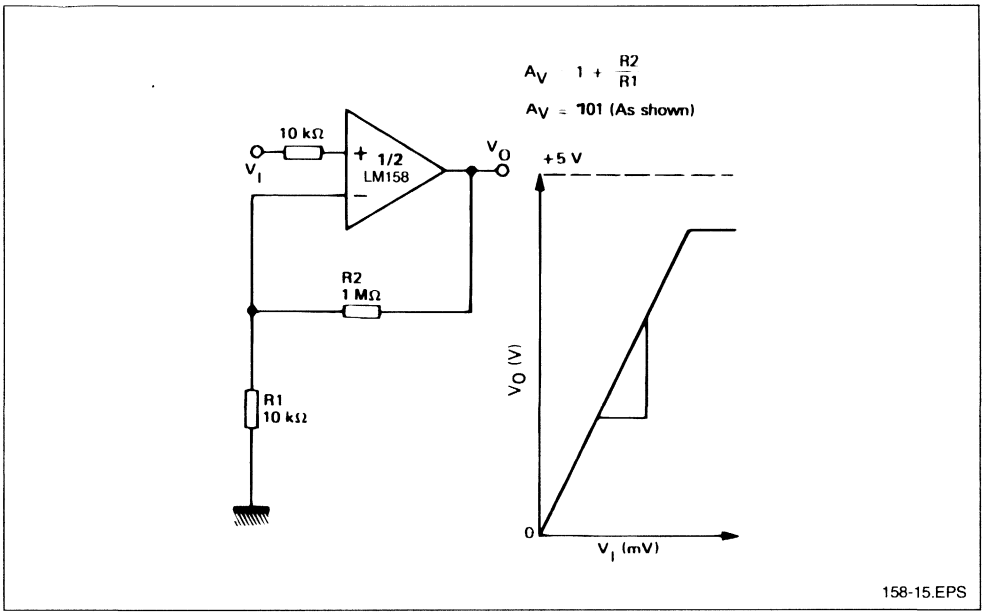


AC COUPLED NON INVERTING AMPLIFIER



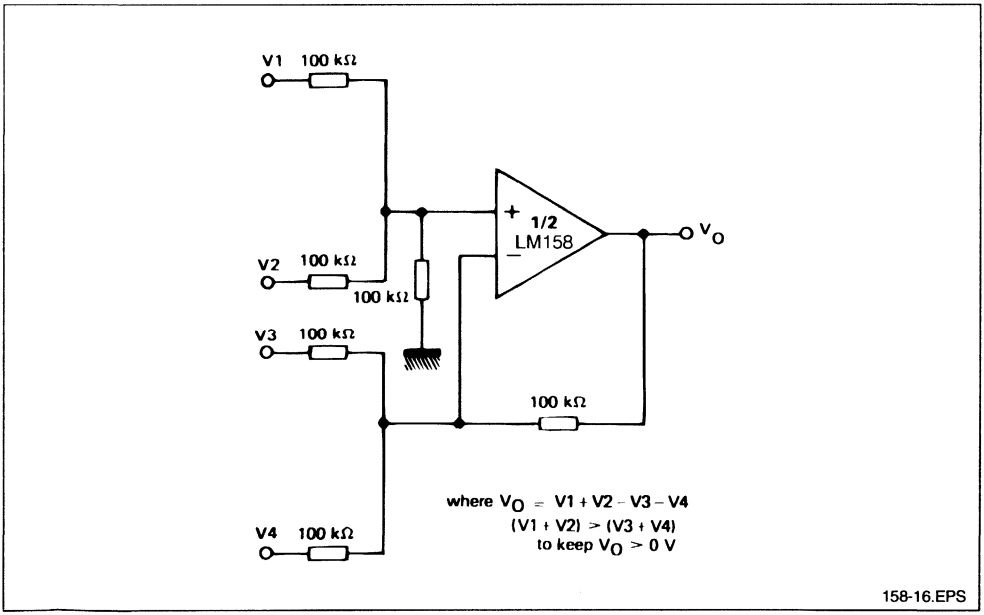
TYPICAL APPLICATIONS (single supply voltage) V_{CC} = +5V_{DC} (continued)

NON INVERTING DC AMPLIFIER



158-15.EPS

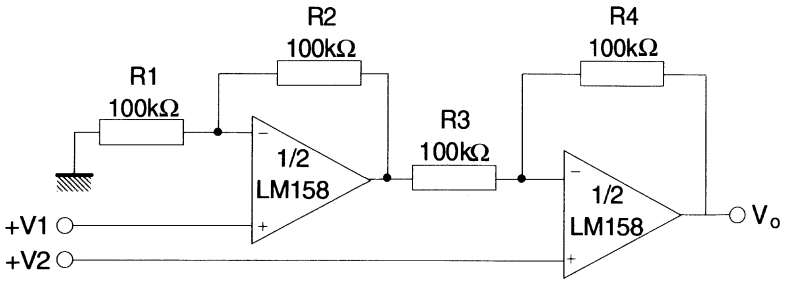
DC SUMING AMPLIFIER



158-16.EPS

TYPICAL APPLICATIONS (single supply voltage) V_{CC} = +5V_{DC} (continued)

HIGH INPUT IMPEDANCE, DC DIFFERENTIAL AMPLIFIER



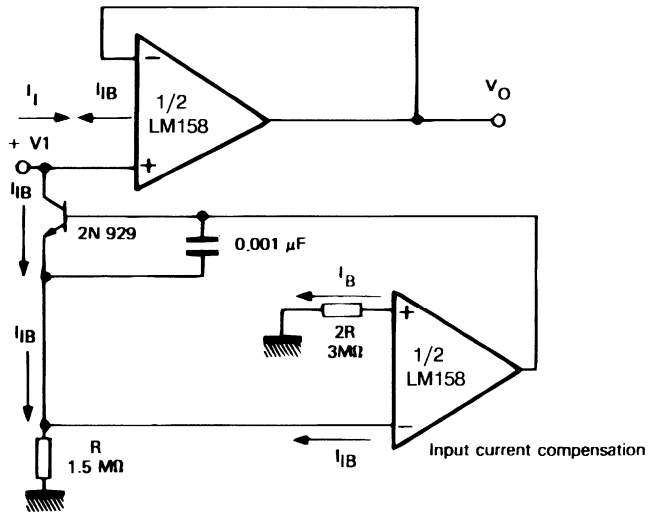
for $\frac{R1}{R2}=\frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

$V_o = (1 + \frac{R4}{R3}) (V2 - V1)$

As shown : $V_o = 2 (V2 - V1)$

158-17.EPS

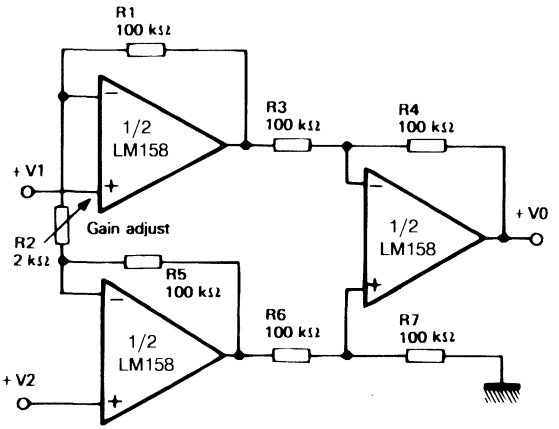
USING SYMMETRICAL AMPLIFIERS TO REDUCE INPUT CURRENT (general concept)



158-18.EPS

TYPICAL APPLICATIONS (single supply voltage) V_{CC} = +5V_{DC} (continued)

HIGH INPUT Z ADJUSTABLE-GAIN DC INSTRUMENTATION AMPLIFIER



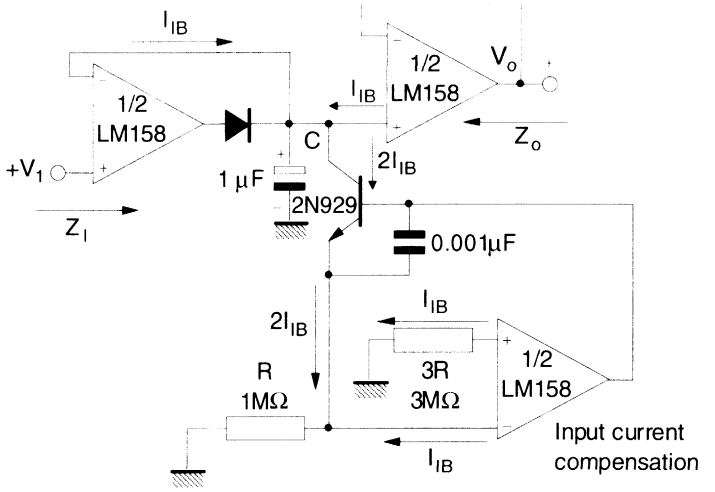
If R1 = R5 and R3 = R4 = R6 = R7

$V_O = \left(1 + \frac{2\,R1}{R2}\right)(V2 - V1)$

As shown : V_O = 101 (V2 - V1)

158-19.EPS

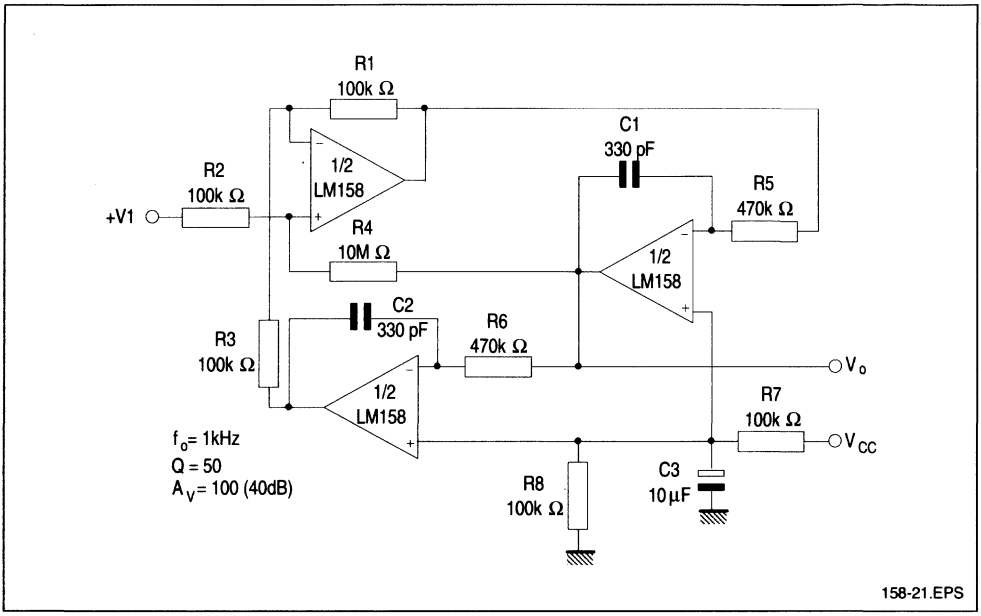
LOW DRIFT PEAK DETECTOR



158-20.EPS

TYPICAL APPLICATIONS (single supply voltage) V_{CC} = +5V_{DC} (continued)

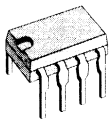
ACTIVE BAND-PASS FILTER



LM193/A - LM293/A LM393/A - LM2903

LOW POWER DUAL VOLTAGE COMPARATORS

- WIDE SINGLE SUPPLY VOLTAGE RANGE OR DUAL SUPPLIES +2V TO +36V OR ±1V TO ±18V
- VERY LOW SUPPLY CURRENT (0.4mA) INDEPENDENT OF SUPPLY VOLTAGE (1 mW/comparator at +5V)
- LOW INPUT BIAS CURRENT : 25nA TYP
- LOW INPUT OFFSET CURRENT : ±5nA TYP
- LOW INPUT OFFSET VOLTAGE : ±1mV TYP
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GROUND
- LOW OUTPUT SATURATION VOLTAGE : 250mV TYP. (I_O = 4mA)
- DIFFERENTIAL INPUT VOLTAGE RANGE EQUAL TO THE SUPPLY VOLTAGE
- TTL, DTL, ECL, MOS, CMOS COMPATIBLE OUTPUTS



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

J
CERDIP8
(Cerdip Package)

H
TO99
(Metal Can)

DESCRIPTION

These devices consist of two independent precision voltage comparators with an offset voltage specifications as low as 2mV max for LM393A, LM293A and LM193A.

All these comparators were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible.

These comparators also have a unique characteristic in that the input common-mode voltage range includes ground even though operated from a single power supply voltage.

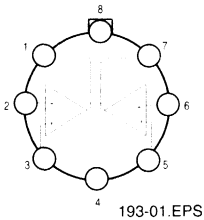
ORDER CODES

Part Number	Temperature Range	Package			
		H	N	J	D
LM193/A	−55, +125°C	•	•	•	•
LM293/A	−40, +105°C	•	•	•	•
LM393/A	0, +70°C	•	•	•	•
LM2903	−40, +105°C	•	•	•	•
Examples : LM193H, LM393D					

193-01.TBL

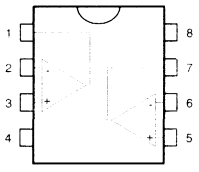
PIN CONNECTIONS (top views)

TO99



193-01.EPS

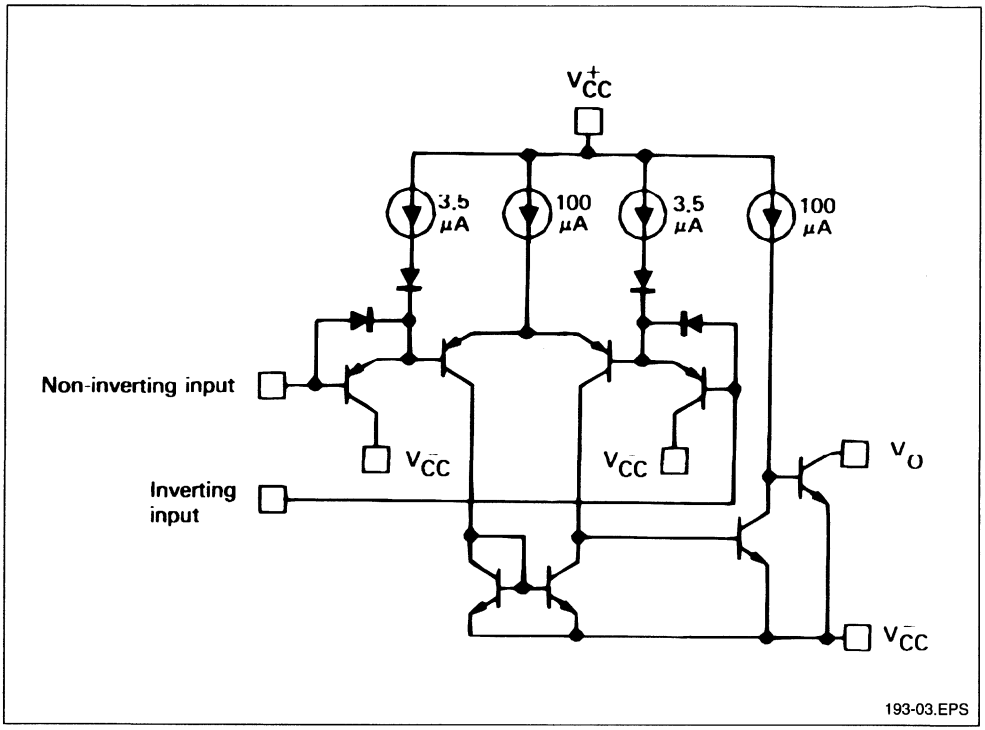
DIP8/CERDIP8
SO8



193-02.EPS

1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^-
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - V_{CC}^+

SCHEMATIC DIAGRAM (1/2 LM193)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	LM193,A	LM293,A	LM393,A LM2903	Unit
V_{CC}	Supply Voltage	±18 or 36	±18 or 36	±18 or 36	V
V_{id}	Differential Input Voltage	±36	±36	±36	V
V_i	Input Voltage	–0.3 to +36	–0.3 to +36	–0.3 to +36	V
–	Output Short-circuit to Ground – (note 1)	Infinite			
P_{tot}	Power Dissipation LM393AH	830	830	570 830	mW
T_{oper}	Operating Free-air TemperatureRange LM2903	–55 to +125	–40 to +105	0 to +70 –40 to +105	°C
T_{stg}	Storage Temperature Range	–65 to +150	–65 to +150	–65 to +150	°C

193-02.TBL

Notes : 1. Short-circuit from the output to V_{CC}^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20mA, independent of the magnitude of V_{CC}^+.

ELECTRICAL CHARACTERISTICS

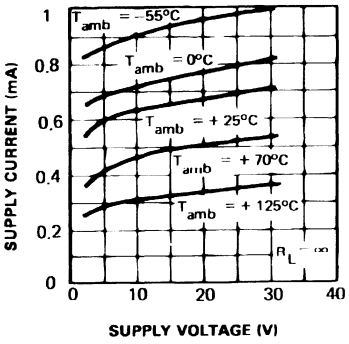
V_{CC}^+ = +5V, V_{CC}^- = GND, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	LM193A - LM293A LM393A			LM193 - LM293 LM393 - LM2903			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage – (note 2) T_{amb} = +25°C LM2903 $T_{min.} \le T_{amb} \le T_{max.}$ LM2903		1	2 4		1	5 7 9 15	mV
I_{ib}	Input Bias Current – (note 3) T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$		25	100 300		25	250 400	nA
I_{io}	Input Offset Current T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$		3	25 100		5	50 150	nA
A_{vd}	Large Signal Voltage Gain V_{CC} = 15V, R_L = 15kΩ, V_o = 1 to 11V LM2903	50	200		50 25	200		V/mV
I_{CC}	Supply Current (all comparators) V_{CC} = 5V, no load V_{CC} = 30V, no load		0.4 1	1 2.5		0.4 1	1 2.5	mA
V_{icm}	Input Common Mode Voltage Range - (note 4) T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$	0 0		V_{CC}^+-1.5 V_{CC}^+ -2	0 0		V_{CC}^+-1.5 V_{CC}^+ -2	V
V_{id}	Differential Input Voltage - (note 6)			V_{CC}^+			V_{CC}^+	V
I_{sink}	Output Sink Current (V_{id} = -1V, V_O = 1.5V)	6	16		6	16		mA
V_{OL}	Low Level Output Voltage (V_{id} = -1V, I_{sink} = 4mA)) T_{amb} = 25°C $T_{min.} < T_{amb} < T_{max.}$		250	400 700		250	400 700	mV
I_{OH}	High Level Output Current (V_{id} = 1V, V_{CC} = V_O = 30V) T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max}$		0.1	 1		0.1	 1	nA µA
t_{re}	Response Time (R_L = 5.1kΩ to V_{CC}^+, V_{ref} = +1.4V) – (note 5)		1.3			1.3		µs
t_{rel}	Large Signal Response Time (V_i = TTL, V_{ref} = +1.4 V, R_L = 5.1kΩ to V_{CC}^+)		300			300		ns

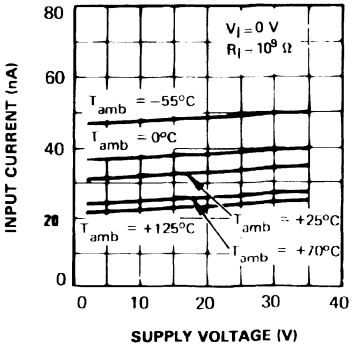
193-03.TBL

Notes :
2. At output switch point, V_O = 1.4V, R_S = 0Ω with V_{CC}^+ from 5V to 30V and over the full input common-mode range (0V to V_{CC}^+ 1.5V).
3. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading charge exists on the reference or input lines.
4. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V_{CC}^+ –1.5V, but either or both inputs can go to +30V without damage.
5. The response time specified is for a 100mV input step with 5mV overdrive. For larger overdrive signals 300ns can be obtained.
6. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range the comparator will provide a proper output state. The low input voltage state must not be less than –0.3V (or 0.3V below the negative power supply, if used).

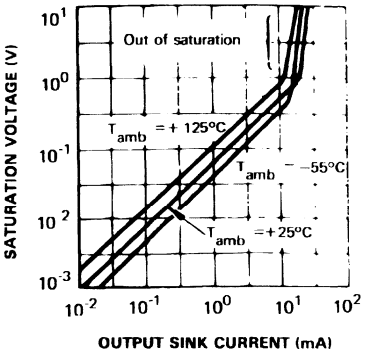
SUPPLY CURRENT



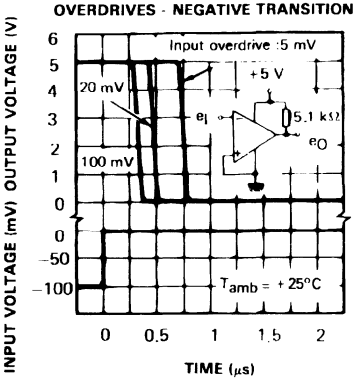
INPUT CURRENT



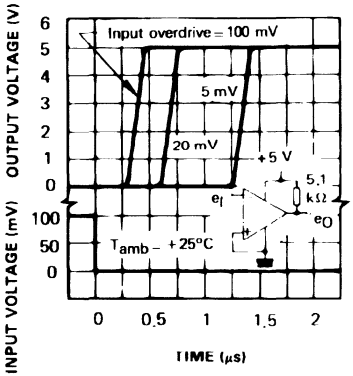
OUTPUT SATURATION VOLTAGE



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES - NEGATIVE TRANSITION



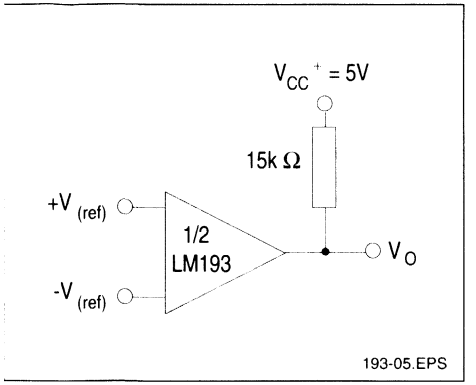
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES - POSITIVE TRANSITION



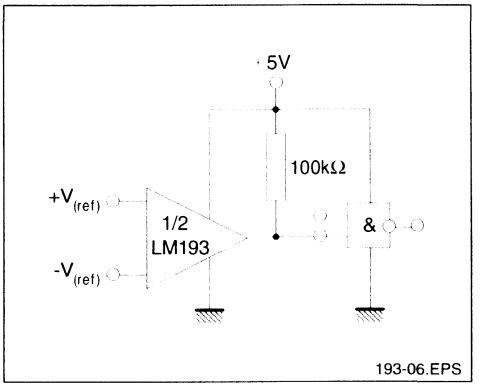
193-04.EPS

TYPICAL APPLICATIONS

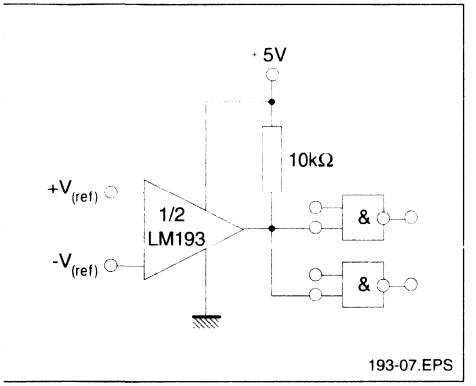
BASIC COMPARATOR



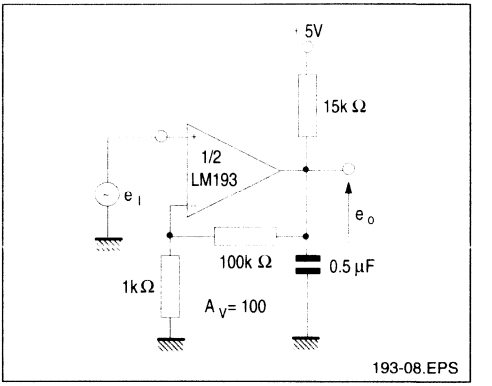
DRIVING CMOS



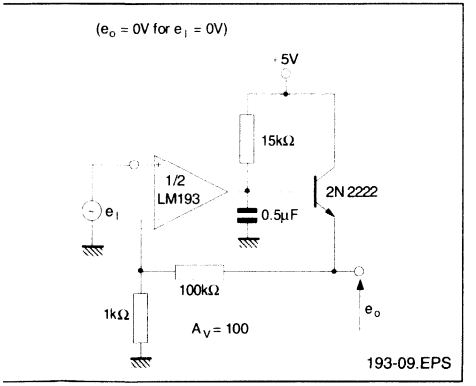
DRIVING TTL



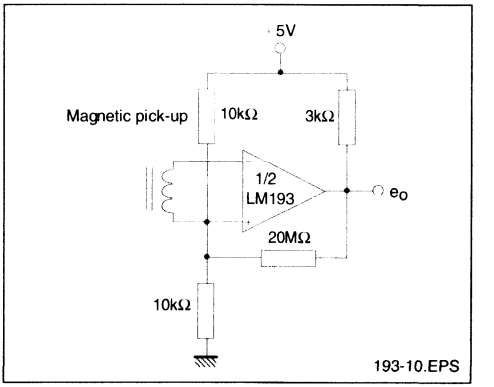
LOW FREQUENCY OP AMP



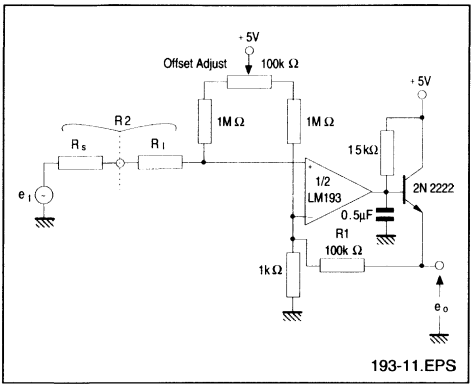
LOW FREQUENCY OP AMP



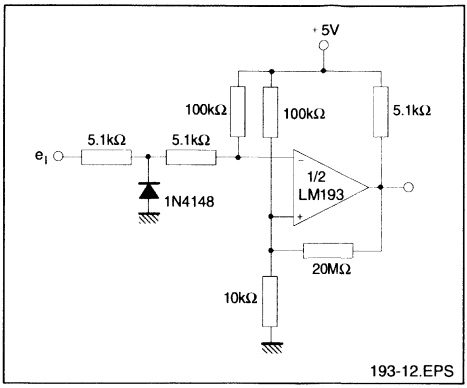
TRANSDUCER AMPLIFIER



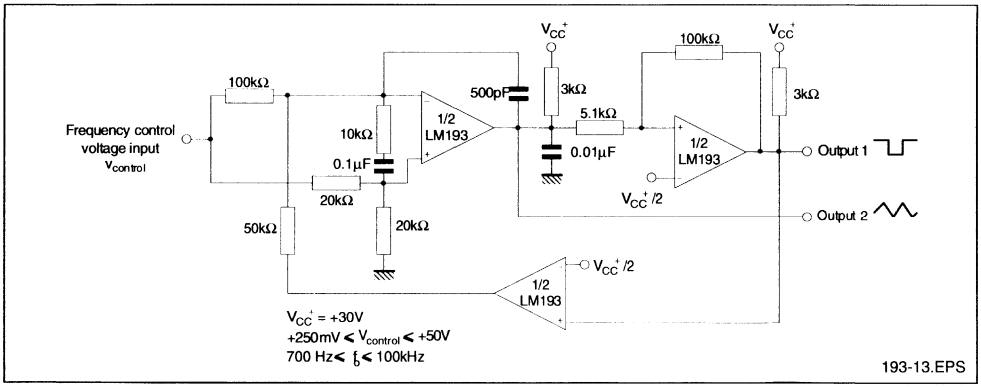
LOW FREQUENCY OP AMP WITH OFFSET ADJUST



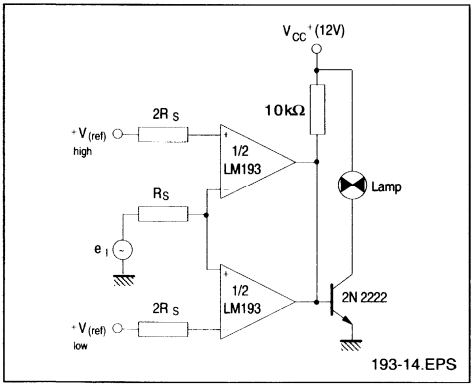
ZERO CROSSING DETECTOR (SINGLE POWER SUPPLY)



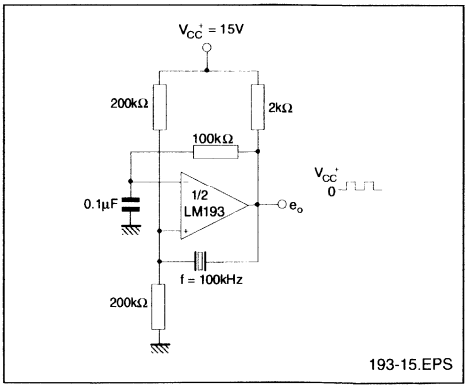
TWO DECADES HIGH FREQUENCY VCO



LIMIT COMPARATOR

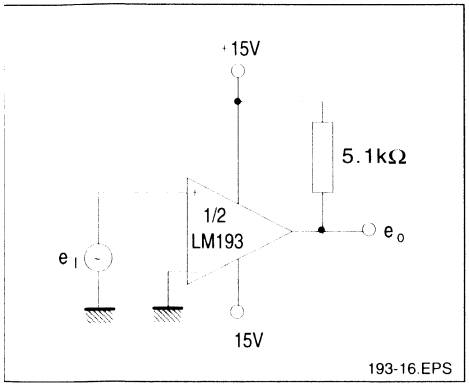


CRYSTAL CONTROLLED OSCILLATOR

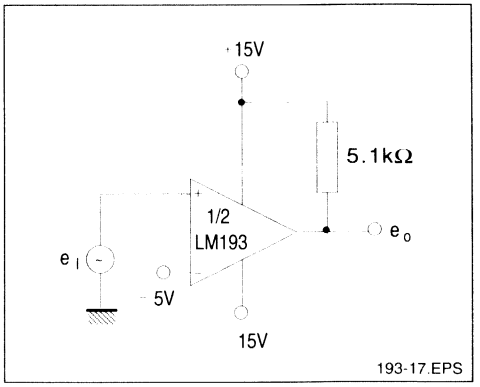


SPLIT-SUPPLY APPLICATIONS

ZERO CROSSING DETECTOR



COMPARATOR WITH A NEGATIVE REFERENCE

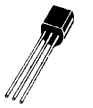


SGS-THOMSON MICROELECTRONICS

LM236/A
LM336/B

2.5V VOLTAGE REFERENCES

- LOW TEMPERATURE COEFFICIENT
- WIDE OPERATING CURRENT OF 400μA TO 10mA
- 0.2Ω DYNAMIC IMPEDANCE
- GUARANTEED TEMPERATURE STABILITY
- FAST TURN-ON



Z
TO92
(Plastic Package

D
SO8
(Plastic Micropackage)

DESCRIPTION

The LM236 and LM336 are precision 2.5V regulator diodes. These voltage reference monolithic ICs operate like 2.5V zener diodes with a low temperature coefficient and a dynamic impedance of 0.2Ω. A third pin enables adjusting the reference voltage and the temperature coefficient.

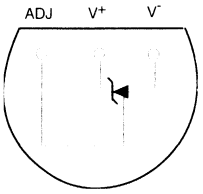
ORDER CODES

Part number	Temperature Range	Package	
		Z	D
LM236/A	−25°C, +85°C	•	•
LM336/B	0°C, +70°C	•	•

236-01.TBL

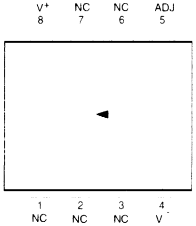
PIN CONNECTIONS

TO92
(Bottom view)



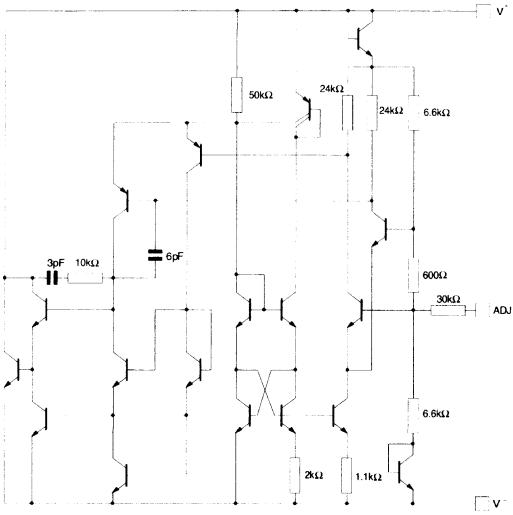
236-01.EPS

SO8
(Top view)



236-02.EPS

SCHEMATIC DIAGRAM



236-03.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	LM236,A	LM336,B	Unit
	Current			mA
I_R	Reverse	15	15	
I_F	Forward	10	10	
T_{oper}	Operating Free-air Temperature Range	–25 to +85	0 to +70	°C
T_{stg}	Storage Temperature Range	–65 to +150		°C

ELECTRICAL CHARACTERISTICS

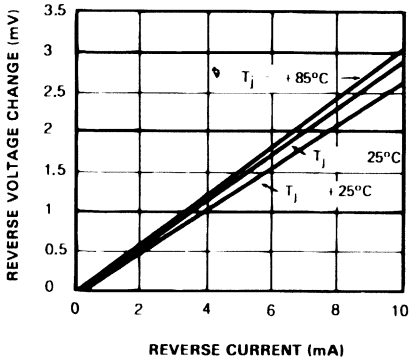
LM236,A $-25°C \leq T_{amb} \leq +85°C$

LM336,B $0°C \leq T_{amb} \leq +70°C$

(unless otherwise specified)

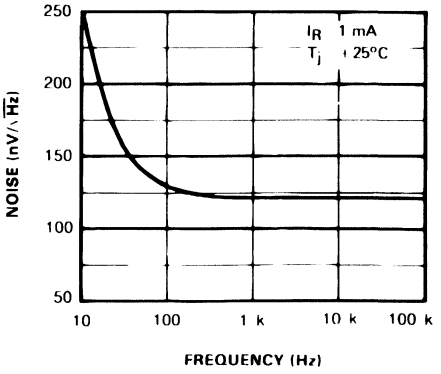
Symbol	Parameter	LM236,A			LM336,B			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_R	Reverse Breakdown Voltage (T_{amb} = +25°C, I_R = 1mA)							V
	LM236, LM336	2.44	2.49	2.54	2.39	2.49	2.59	
	LM236A, LM336B	2.465	2.49	5.515	2.44	2.49	2.59	
ΔV_R	Reverse Breakdown Voltage Change with Current (400µA ≤ I_R ≤ 10mA)							mV
	T_{amb} = +25°C		2.6	6		2.6	10	
	$T_{min.} \leq T_{amb} \leq T_{max.}$		3	10		3	12	
Z_D	Reverse Dynamic Impedance (I_R = 1mA)							Ω
	T_{amb} = +25°C		0.2	0.6		0.2	1	
	$T_{min.} \leq T_{amb} \leq T_{max.}$		0.4	1		0.4	1.4	
K_{VT}	Temperature Stability (V_R = 2.49V, I_R = 1mA)		3.5	9		1.8	6	mV
K_{VH}	Long Term Stability (T_{amb} = +25°C ±0.1°C, I_R = 1mA)		20			20		ppm

REVERSE VOLTAGE CHANGE



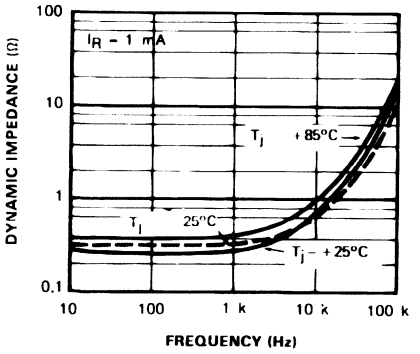
236-04.EPS

ZENER NOISE VOLTAGE



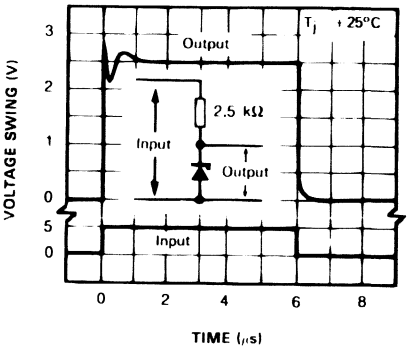
236-05.EPS

DYNAMIC IMPEDANCE



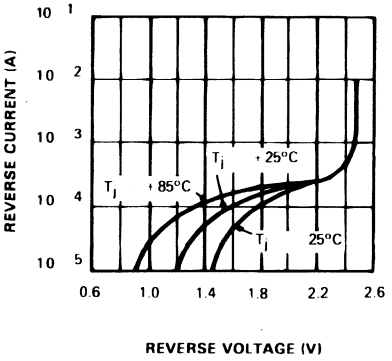
236-06.EPS

RESPONSE TIME



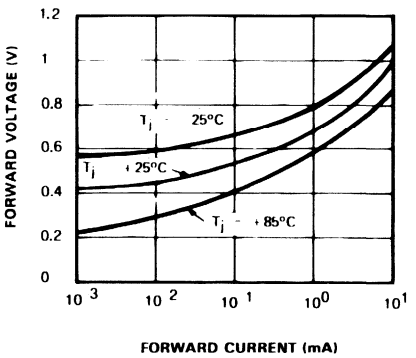
236-07.EPS

REVERSE CHARACTERISTICS

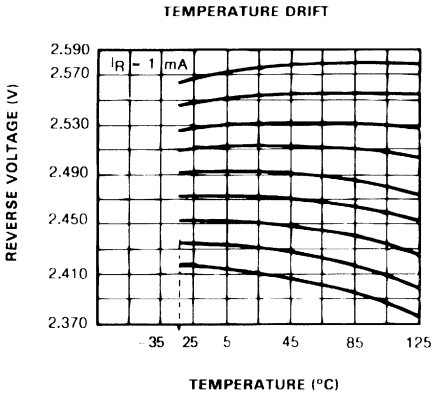


236-08.EPS

FORWARD CHARACTERISTICS



236-09.EPS



236-10.EPS

APPLICATION HINTS

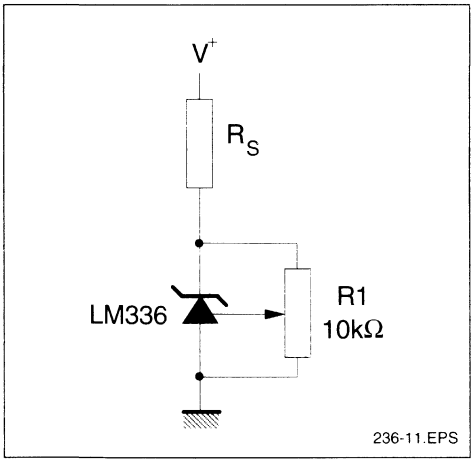
The LM236, LM336 voltage references are easier to use than zener diodes. Their low impedance and wide current range facilitate biasing in any circuits. Besides, the breakdown voltage or the temperature coefficient can be adjusted so as to optimize the performance of the circuit.

Figure 1 represents a LM336 with a 10kΩ potentiometer to adjust the reverse breakdown voltage can be adjusted without altering the temperature coefficient of the circuit. The adjustment range is generally sufficient to adjust the initial tolerance of the circuit and the inaccuracy of the amplifier circuit.

To obtain a lower temperature coefficient two diodes can be connected in series as indicated in Figure 2. When the circuit is adjusted to 2.49V the temperature coefficient is minimized.

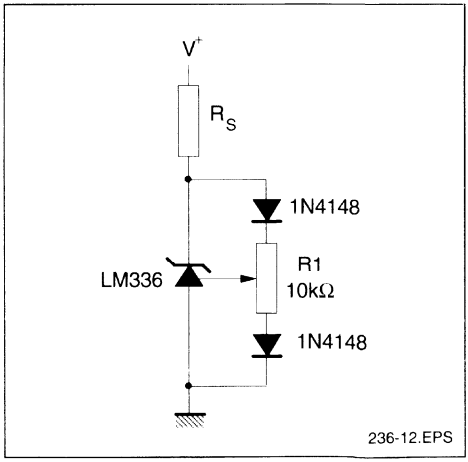
For a correct temperature coefficient, the diodes should be at the same ambient temperature as the LM336. The value of F1 is not critical (2-20kΩ).

Figure 1 : The LM336 with Pot for Adjustment of Breakdown Voltage



236-11.EPS

Figure 2 : Temperature Coefficient Adjustment



236-12.EPS

TYPICAL APPLICATIONS

Figure 3 : 2.5V Reference

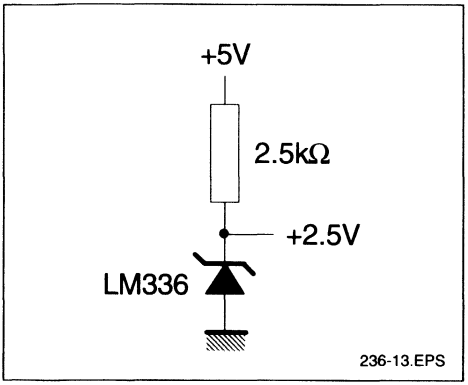


Figure 4 : Wide Input Range Reference

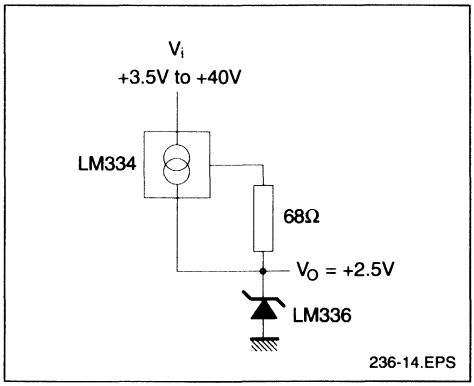


Figure 5 : Precision Power Regulator with Low Temperature Coefficient

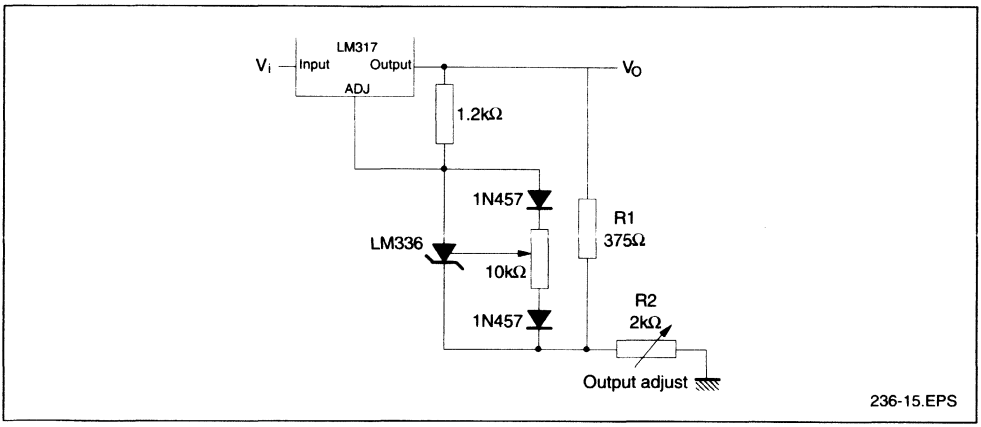


Figure 6 : Adjustable Shunt Regulator

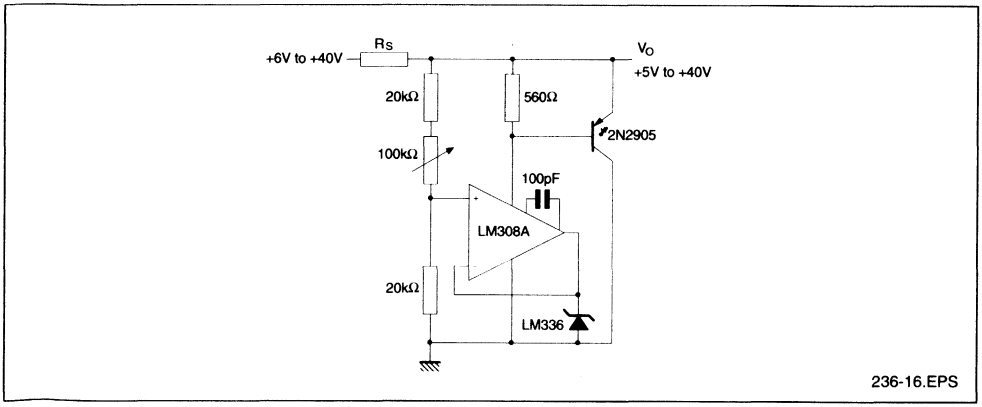


Figure 7 : Linear Ohmmeter

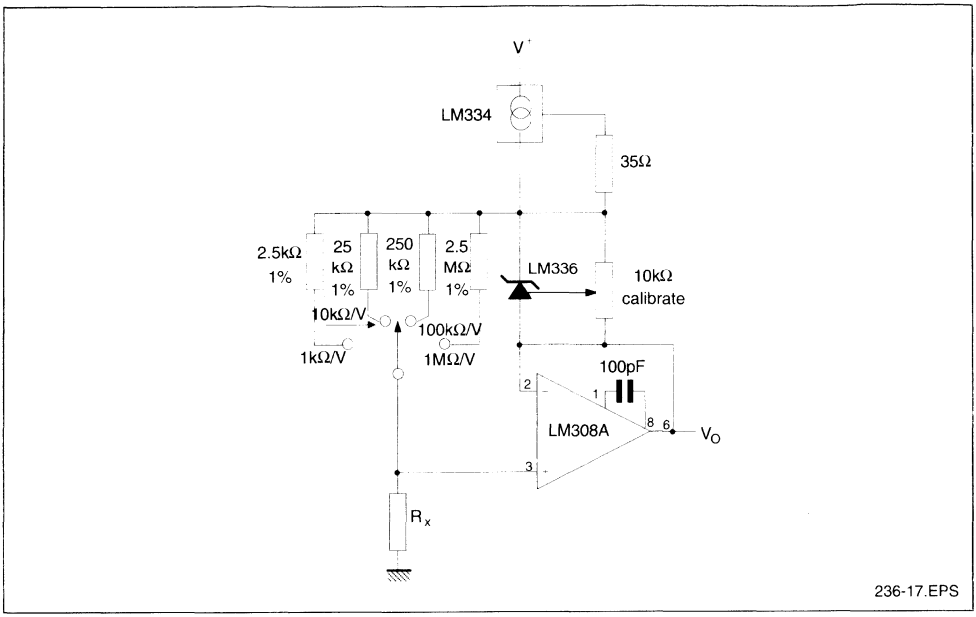


Figure 8 : Bipolar Output Reference

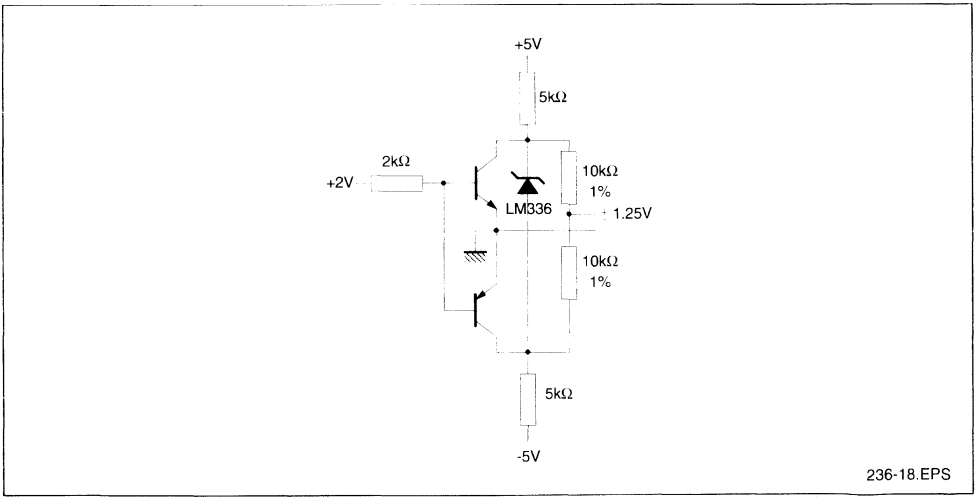


Figure 9 : 5V Buffered Reference

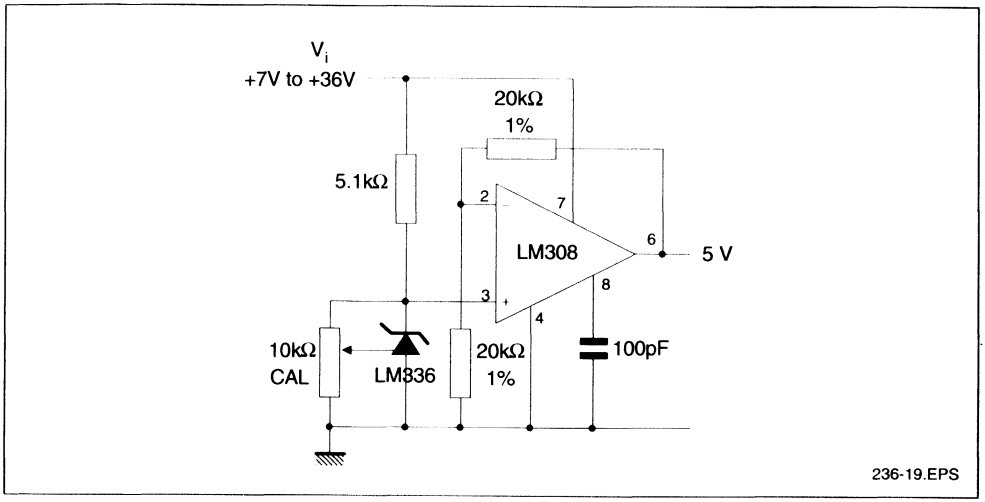
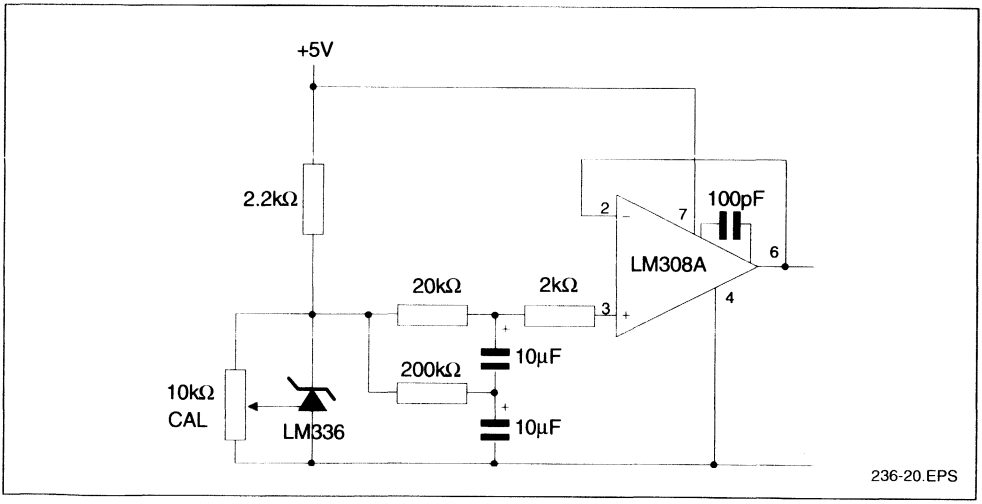


Figure 10 : Low Noise Buffered Reference



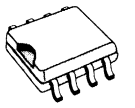
SGS-THOMSON MICROELECTRONICS

LM317L

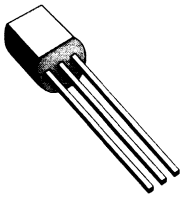
LOW CURRENT 1.2V TO 37V ADJUSTABLE VOLTAGE REGULATOR

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST/1)

- OUTPUT VOLTAGE RANGE : 1.2 TO 37V
- OUTPUT CURRENT IN EXCESS OF 100 mA
- LINE REGULATION TYP. 0.01%
- LOAD REGULATION TYP. 0.1%
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTOR SAFE AREA COMPENSATION
- FLOATING OPERATION FOR HIGH VOLTAGE APPLICATIONS



SO-8



TO-92

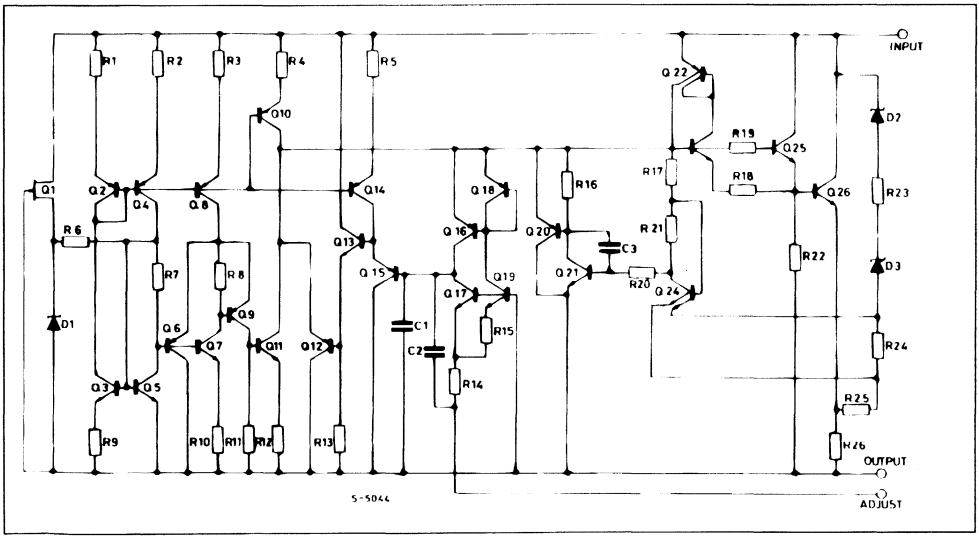
DESCRIPTION

The LM317L is a monolithic integrated circuit in SO-8 and TO-92 packages intended for use as positive adjustable voltage regulators.

It is designed to supply until 100 mA of load current with an output voltage adjustable over a 1.2 to 37V range.

The nominal output voltage is selected by means of only a resistive divider, making the device exceptionally easy to use and eliminating the stocking of many fixed regulators.

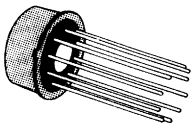
SCHEMATIC DIAGRAM



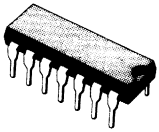
HIGH PRECISION VOLTAGE REGULATOR

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST/1)

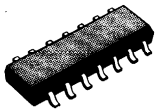
- INPUT VOLTAGE UP TO 40V
- OUTPUT VOLTAGE ADJUSTABLE FROM 2 TO 37V
- POSITIVE OR NEGATIVE SUPPLY OPERATION
- SERIES, SHUNT, SWITCHING OR FLOATING OPERATION
- OUTPUT CURRENT TO 150mA WITHOUT EXTERNAL PASS TRANSISTOR
- ADJUSTABLE CURRENT LIMITING



TO-100



DIP-14
(Ceramic and Plastic)

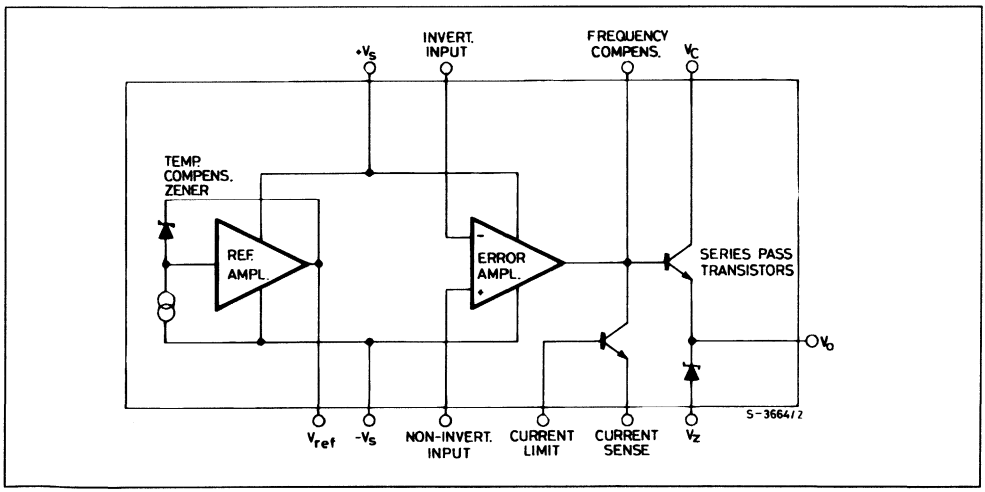


SO-14

DESCRIPTION

The LM723 is a monolithic integrated programmable voltage regulator, assembled in 14-lead dual in-line plastic and ceramic package, 10-lead Metal Can (TO-100 type) and SO-14 micropackage. The circuit provides internal current limiting. When the output current excedes 150mA an external NPN or PNP pass element may be used. Provisions are made for adjustable current limiting and remote shut-down.

BLOCK DIAGRAM



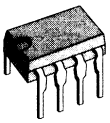
SGS-THOMSON MICROELECTRONICS

LM833

LOW NOISE DUAL OPERATIONAL AMPLIFIERS

PRELIMINARY DATA

- LOW VOLTAGE NOISE : 4.5nV$\sqrt{Hz}$
- HIGH GAIN BANDWIDTH PRODUCT : 15MHz
- HIGH SLEW RATE : 7.0V/µs
- LOW DISTORTION : 0.002%
- EXCELLENT FREQUENCY STABILITY
- ESD PROTECTION 2000V



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

DESCRIPTION

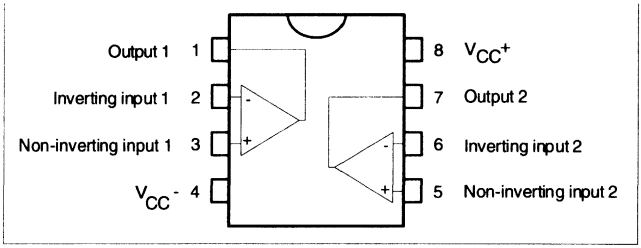
The LM833 is a monolithic dual operational amplifier dedicated to audio applications. The LM833 offers low voltage noise (4.5nV$\sqrt{Hz}$) and high frequency performances (15MHz gain bandwidth product, 7V/µs slew rate).
In addition the LM833 has also a very low distortion (0.002%) and excellent phase/gain margins.

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
LM833	-40, +105°C	•	•

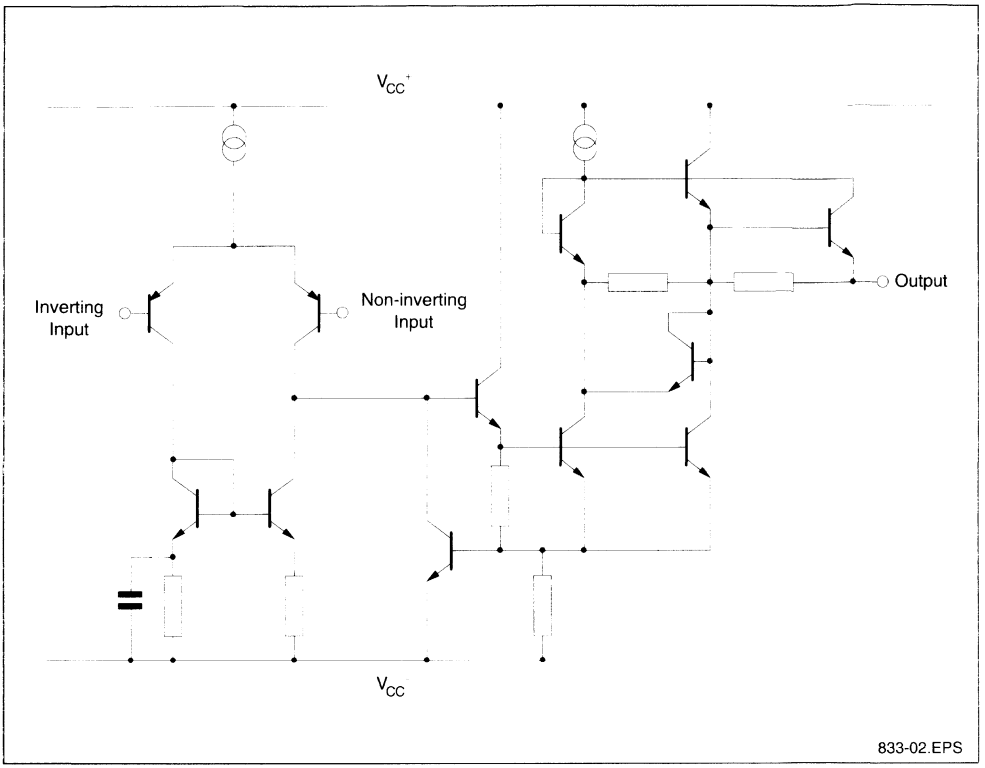
833-01.TBL

PIN CONNECTIONS (top view)



833-01.EPS

SCHEMATIC DIAGRAM (1/2 LM833)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (V_{CC}^+ to V_{CC}^-)	+36	V
V_{id}	Differential Input Voltage - (note 1)	30	V
V_{in}	Input Voltage - (note 1)	± 15	V
	Output Short-Circuit Duration - (note 2)	Infinite	
T_{oper}	Operating Free-air Temperature Range	-40 to +105	°C
T_j	Maximum Junction Temperature	+150	°C
T_{stg}	Storage Temperature	-65 to +150	°C
P_{tot}	Maximum Power Dissipation - (note 2)	500	mW

Notes : 1. Either or both input voltages must not exceed the magnitude of V_{CC}^+ or V_{CC}^-
2. Power dissipation must be considered to ensure maximum junction temperature (T_j) is not exceeded

ELECTRICAL CHARACTERISTICS

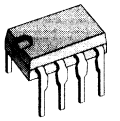
V_{CC}^+ = +15V, V_{CC}^- = -15V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IO}	Input Offset Voltage (R_S = 10Ω, V_{ic} = 0V, V_o = 0V)		0.3	5	mV
DV_{IO}	Input Offset Voltage Drift (R_S = 10Ω, V_o = 0V, $T_{min.} \leq T_{amb} \leq T_{max.}$)		2		µV/°C
I_{io}	Input Offset Current (V_{ic} = 0V, V_O = 0V)		25	200	nA
I_{ib}	Input Bias Current (V_{ic} = 0V, V_O = 0V)		300	1000	nA
V_{icm}	Common Mode Input Voltage Range	±12	±14		V
A_{vd}	Large Signal Voltage Gain (R_L = 2kΩ, V_O = ±10V)	90	100		dB
$\pm V_{opp}$	Output Voltage Swing (V_{id} = ±1V) R_L = 2.0kΩ R_L = 2.0kΩ R_L = 10kΩ R_L = 10kΩ	 10 12	 13.7 -14 13.9 -14.4	 -10 -12	V
CMR	Common Mode Rejection Ratio (V_{ic} = ±12V)	80	100		dB
SVR	Supply Voltage Rejection Ratio (V_{CC}^+ / V_{CC}^- = +15V / -15V to +5V / -5V)	80	105		dB
I_{CC}	Supply Current (V_O = 0V, both amplifiers)		4	8	mA
SR	Slew Rate (V_i = -10V to +10V, R_L = 2kΩ, A_V = +1V)	5	7		V/µs
GBP	Gain Bandwidth Product (f = 100kHz, R_L = 2kΩ, C_L = 100pF)	10	15		MHz
B	Unity Gain Bandwidth (Open loop)		9		MHz
Øm	Phase Margin		60		Degrees
e_n	Equivalent Input Noise Voltage (R_S = 100Ω, f = 1kHz)		4.5		$\frac{nV}{\sqrt{Hz}}$
i_n	Equivalent Input Noise current (f = 1kHz)		0.5		$\frac{pA}{\sqrt{Hz}}$
FPB	Full Power Bandwidth (V_O = 27Vpp, R_L = 2kΩ, THD ≤ 1%)		120		kHz
THD	Total Harmonic Distortion (R_L = 2kΩ, f = 20Hz to 20kHz, V_O = $3V_{rms}$, A_V = +1)		0.002		%
V_{O1}/V_{O2}	Channel Separation (f = 20Hz to 20kHz)		120		dB

833-03.TBL

HIGH PERFORMANCE DUAL OPERATIONAL AMPLIFIERS

- LOW POWER CONSUMPTION
- SHORT CIRCUIT PROTECTION
- LOW DISTORTION, LOW NOISE
- HIGH GAIN-BANDWIDTH PRODUCT
- HIGH CHANNEL SEPARATION



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

H
TO99
(Metal Can)

DESCRIPTION

The LS204 is a high performance dual operational amplifier with frequency and phase compensation built into the chip. The internal phase compensation allows stable operation as voltage follower in spite of its high gain-bandwidth products.

The circuit presents very stable electrical characteristics over the entire supply voltage range, and is particularly intended for professional and telecom applications (active filters, etc).

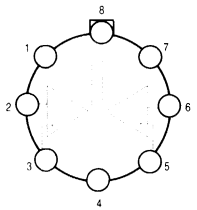
ORDER CODES

Part Number	Temperature Range	Package		
		H	N	D
LS204C	0°C, +70°C	•	•	•
LS204I	-40°C, +105°C	•	•	•
LS204M	-55°C, +125°C	•	•	•

204-01.TBL

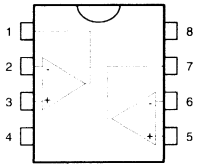
PIN CONNECTIONS (top views)

TO99



204-01.EPS

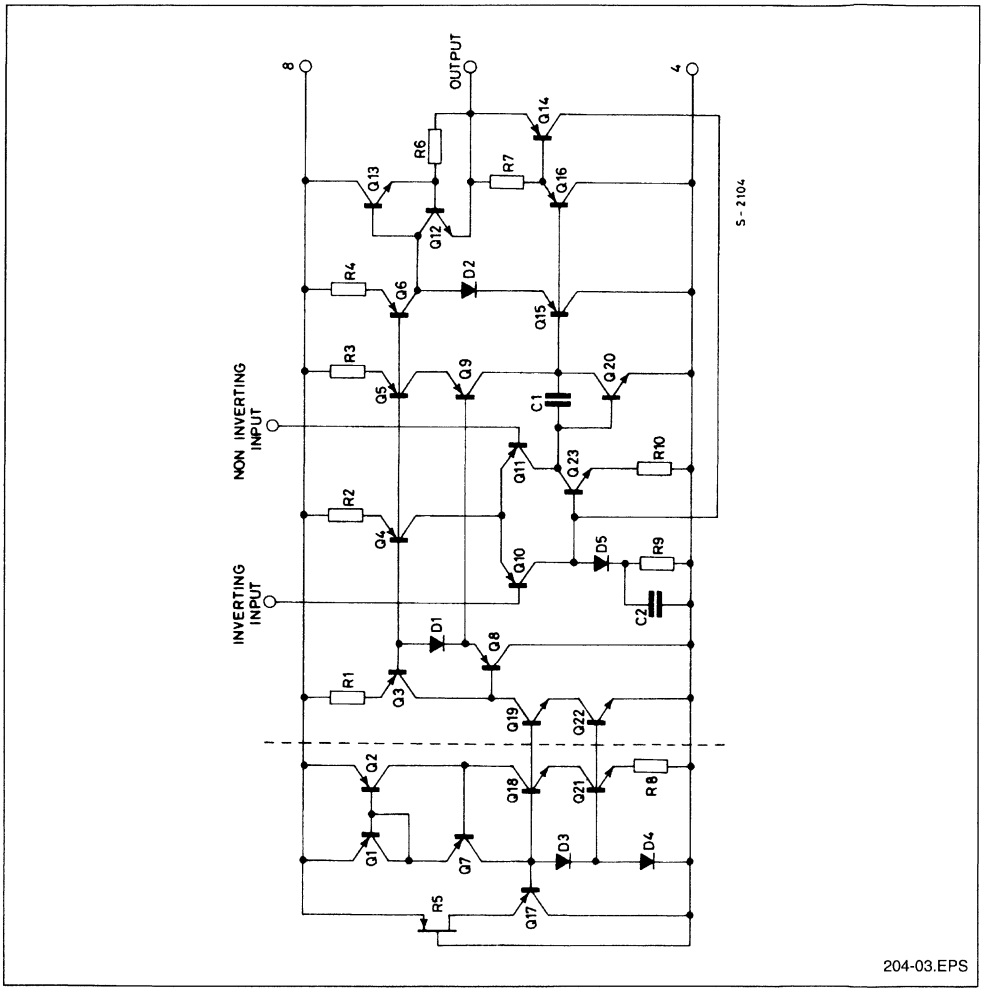
DIP8/SO8



204-02.EPS

1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^-
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output
8 - V_{CC}^+

SCHEMATIC DIAGRAM (1/2 LS204)



ABSOLUTE MAXIMUM RATINGS

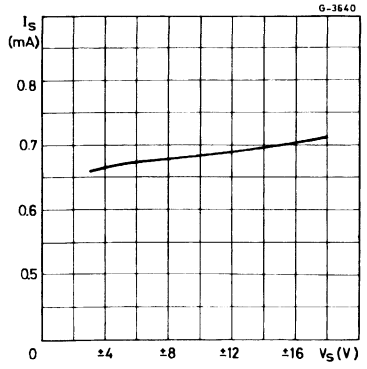
Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		±18	V
V_i	Input Voltage		$\pm V_{CC}$	
V_{id}	Differential Input Voltage		$\pm(V_{CC} - 1)$	
T_{oper}	Operating Temperature Range	LS204C LS204I LS204M	0 to +70 -40 to +105 -55 to +125	°C
P_{tot}	Power Dissipation at T_{amb} = 70°C		500	mW
T_j	Junction Temperature		150	°C
T_{stg}	Storage Temperature		-65 to 150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = ±15V, T_{amb} = 25°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	LS204I - LS204M			LS204C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{CC}	Supply Current			0.7	1.2		0.8	1.5	mA
I_{ib}	Input Bias Current			50	150		100	300	nA
		$T_{min.} < T_{op} < T_{max.}$			300			700	nA
R_i	Input Resistance	f = 1kHz		1			0.5		MΩ
V_{io}	Input Offset Voltage	$R_s \leq 10k\Omega$		0.5	2.5		0.5	3.5	mV
		$R_s \leq 10k\Omega$ $T_{min.} < T_{op} < T_{max.}$			3.5			5	mV
DV_{io}	Input Offset Voltage Drift	$R_s \leq 10k\Omega$ $T_{min.} < T_{op} < T_{max.}$		5			5		µV/°C
I_{io}	Input Offset Current			5	20		12	50	nA
		$T_{min.} < T_{op} < T_{max.}$			40			100	nA
DI_{io}	Input Offset Current Drift	$T_{min.} < T_{op} < T_{max.}$		0.08			0.1		nA/°C
I_{os}	Output Short Circuit Current			23			23		mA
A_{vd}	Large Signal Voltage Gain	$T_{min.} < T_{op} < T_{max.}$ $R_L = 2k\Omega$ $V_{CC} = \pm15V$ $V_{CC} = \pm4V$	90	100 95		86	100 95		dB
GBP	Gain-bandwidth Product	f = 100kHz	1.8	3		1.5	2.5		MHz
e_n	Equivalent Input Noise Voltage	f = 1kHz $R_s = 50\Omega$ $R_s = 1k\Omega$ $R_s = 10k\Omega$		8 10 18	15		10 12 20		nV/√Hz
THD	Total Harmonic Distortion	A_V = 20dB $R_L = 2k\Omega$ $V_O = 2V_{PP}$ f = 1kHz		0.03	0.1		0.03	0.1	%
$\pm V_{opp}$	Output Voltage Swing	$R_L = 2k\Omega$ $V_{CC} = \pm15V$ $V_{CC} = \pm4V$	±13	±3		±13	±3		V
V_{opp}	Large Signal Voltage Swing	$R_L = 10k\Omega$ f = 10kHz		28			28		V_{PP}
SR	Slew Rate	Unity Gain, $R_L = 2k\Omega$	0.8	1.5			1		V/µs
CMR	Common Mode Rejection Ratio	V_{ic} = 10V $T_{min.} < T_{op} < T_{max.}$	90			86			dB
SVR	Supply Voltage Rejection Ratio	V_{ic} = 1V f = 100Hz $T_{min.} < T_{op} < T_{max.}$	90			86			dB
V_{O1}/V_{O2}	Channel Separation	f = 1kHz	100	120			120		dB

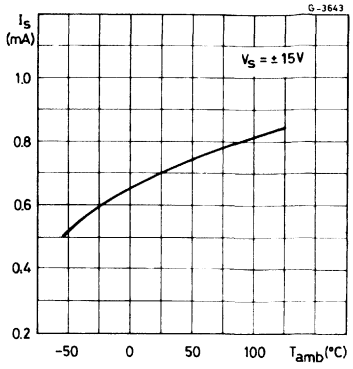
204-03.TBL

Figure 1 : Supply Current versus Supply Voltage



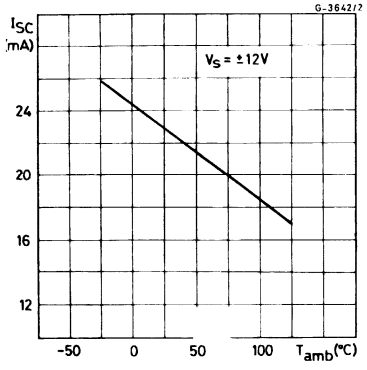
204-04.EPS

Figure 2 : Supply Current versus Ambient Temperature



204-05.EPS

Figure 3 : Output Short Circuit Current versus Ambient Temperature



204-06.EPS

Figure 4 : Open Loop Frequency and Phase Response

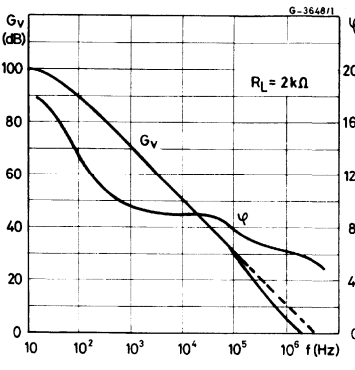


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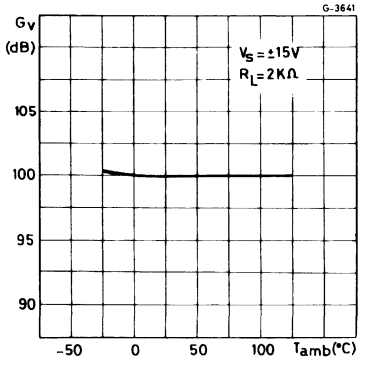
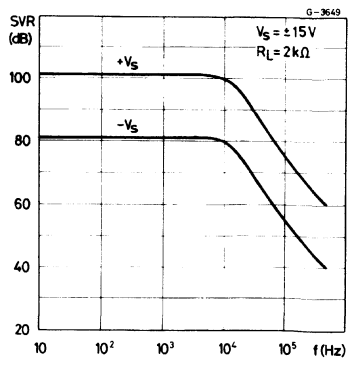
Figure 5 : Output Loop Gain versus Ambient Temperature



204-08.EPS

Figure 6 : Supply Voltage Rejection versus Frequency



204-09.EPS

Figure 7 : Large Signal Frequency Response

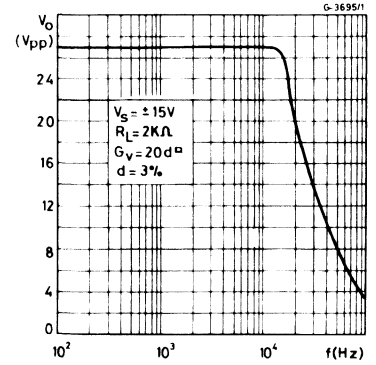


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Figure 8 : Output Voltage Swing versus Load Resistance

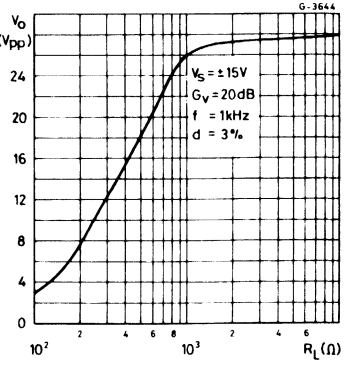

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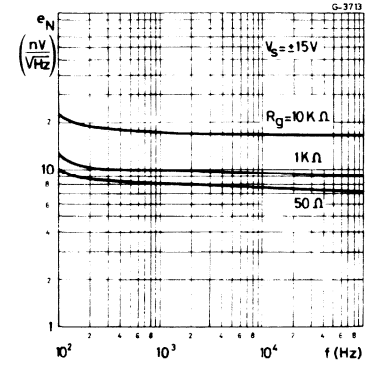
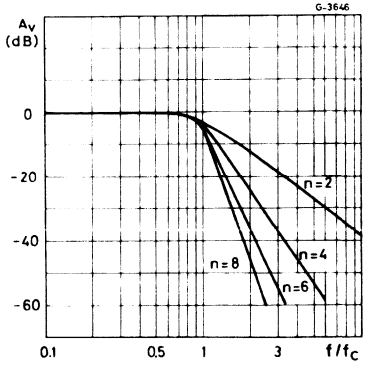
Figure 9 : Total Input Noise versus Frequency



204-12.EPS

Figure 10 : Amplitude Response



204-13.EPS

Figure 11 : Amplitude Response

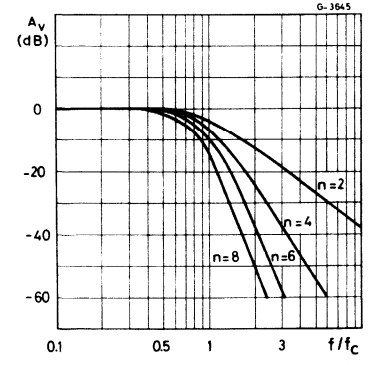


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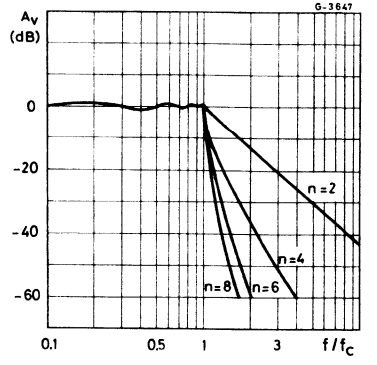
Figure 12 : Amplitude Response (±1dB ripple)



204-15.EPS

APPLICATION INFORMATION : Active low-pass filter

BUTTERWORTH

The Butterworth is a "maximally flat" amplitude response filter. Butterworth filters are used for filtering signals in data acquisition systems to prevent aliasing errors in sampled-data applications and for general purpose low-pass filtering.

The cut-off frequency f_c, is the frequency at which the amplitude response is down 3dB. The attenuation rate beyond the cutoff frequency is n6 dB per octave of frequency where n is the order (number of poles) of the filter.

Other characteristics :

- Flattest possible amplitude response.
- Excellent gain accuracy at low frequency end of passband.

BESSEL

The Bessel is a type of "linear phase" filter. Because of their linear phase characteristics, these filters approximate a constant time delay over a limited frequency range. Bessel filters pass transient waveforms with a minimum of distortion. They are also used to provide time delays for low pass filtering of modulated waveforms and as a "running average" type filter.

The maximum phase shift is $\frac{-n\Pi}{2}$ radians where n is the order (number of poles) of the filter. The cut-off frequency fc, is defined as the frequency at which the phase shift is one half of this value. For accurate delay, the cut-off frequency should be twice the maximum signal frequency.

The following table can be used to obtain the -3dB frequency of the filter.

	2 pole	4 Pole	6 Pole	8 Pole
–3dB Frequency	$0.77f_c$	$0.67f_c$	$0.57f_c$	$0.50f_c$

Other characteristics :

- Selectivity not as great as Chebyschev or Butterworth.
- Very little overshoot response to step inputs.
- Fast rise time.

CHEBYSCHEV

Chebyschev filters have greater selectivity than either Bessel or Butterworth at the expense of ripple in the passband.

Chebyschev filters are normally designed with peak-to-peak ripple values from 0.2dB to 2dB.

Increased ripple in the passband allows increased attenuation above the cut-off frequency.

The cut-off frequency is defined as the frequency at which the amplitude response passes through the specified maximum ripple band and enters the stop band.

Other characteristics :

- Greater selectivity
- Very non-linear phase response
- High overshoot response to step inputs

The table below shows the typical overshoot and settling time response of the low pass filters to a step input.

	Number of Poles	Peak Overshoot	Settling Time (% of final value)		
		% Overshoot	±1%	±0 .1%	±0 0.1%
Butterworth	2	4	$1.1/f_c$sec.	$1.7/f_c$sec.	$1.9/f_c$sec.
	4	11	$1.7/f_c$	$2.8/f_c$	$3.8/f_c$
	6	14	$2.4/f_c$	$3.9/f_c$	$5.0/f_c$
	8	16	$3.1/f_c$	$5.1/f_c$	$7.1/f_c$
Bessel	2	0.4	$0.8/f_c$	$1.4/f_c$	$1.7/f_c$
	4	0.8	$1.0/f_c$	$1.8/f_c$	$2.4/f_c$
	6	0.6	$1.3/f_c$	$2.1/f_c$	$2.7/f_c$
	8	0.3	$1.6/f_c$	$2.3/f_c$	$3.2/f_c$
Chebyschev (ripple ±0.25dB)	2	11	$1.1/f_c$	$1.6/f_c$	–
	4	18	$3.0/f_c$	$5.4/f_c$	–
	6	21	$5.9/f_c$	$10.4/f_c$	–
	8	23	$8.4/f_c$	$16.4/f_c$	–
Chebyschev (ripple ±1dB)	2	21	$1.6/f_c$	$2.7/f_c$	–
	4	28	$4.8/f_c$	$8.4/f_c$	–
	6	32	$8.2/f_c$	$16.3/f_c$	–
	8	34	$11.6/f_c$	$24.8/f_c$	–

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Design of 2nd order active low pass filter (Sallen and Key configuration unity gain-op-amp)

Fixed R = R1 = R2, we have (see fig. 13).

$$C1 = \frac{1}{R}\frac{\xi}{\omega_c}$$

$$C2 = \frac{1}{R}\frac{1}{\xi\omega_c}$$

The diagram of fig.14 shows the amplitude response for different values of damping factor ξ in 2nd order filters.

Figure 13 : Filter Configuration

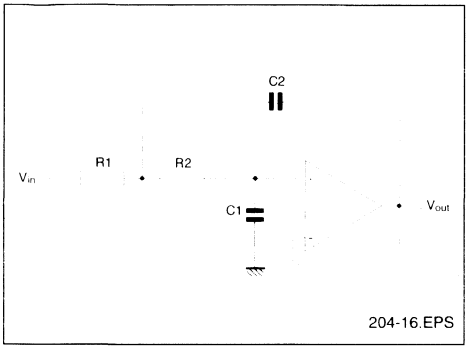
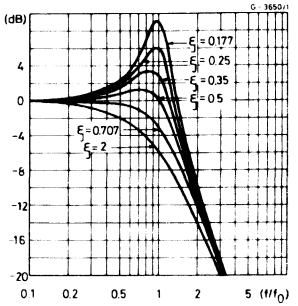


Figure 14 : Filter Respons versus Damping Factor



Three parameters are needed to characterize the frequency and phase response of a 2nd order active filter : the gain (G_V), the damping factor (ξ) or the Q-factor ($Q = (2\xi)^{-1}$), and the cutoff frequency (f_c).

The higher order responses are obtained with a series of 2nd order sections. A simple RC section is introduced when an odd filter is required.

The choice of 'ξ' (or Q-factor) determines the filter response (see table 1).

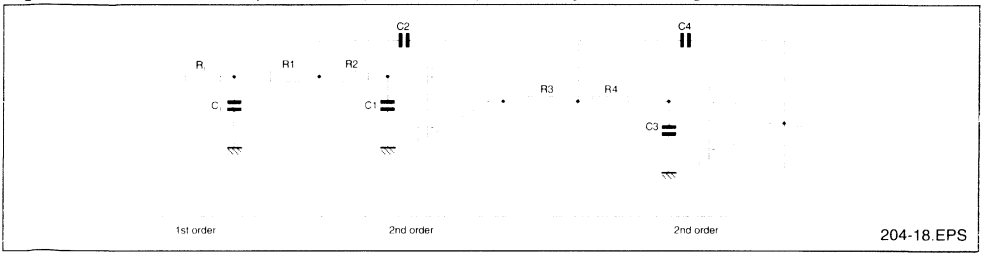
Table 1

Filter Response	ξ	Q	Cutoff Frequency f_c
Bessel	$\frac{\sqrt{3}}{2}$	$\frac{\sqrt{1}}{3}$	Frequency at which Phase Shift is -90°C
Butterworth	$\frac{\sqrt{2}}{2}$	$\frac{\sqrt{1}}{2}$	Frequency at which G_V = -3dB
Chebyschev	$\frac{\sqrt{2}}{2}$	$\frac{\sqrt{1}}{2}$	Frequency at which the amplitude response passes through specified max. ripple band and enters the stop band.

204-05.TBL

EXAMPLE

Figure 15 : 5th Order Low-pass Filter (Butterworth) with Unity Gain Configuration



In the circuit of fig. 15, for f_c = 3.4kHz and $R_i = R_1 = R_2 = R_3 = R_4$ = 10kΩ, we obtain :

$$C_i = 1.354 \cdot \frac{1}{R} \cdot \frac{1}{2\Pi f_C} = 6.33nF$$

$$C_1 = 0.421 \cdot \frac{1}{R} \cdot \frac{1}{2\Pi f_C} = 1.97nF$$

$$C_2 = 1.753 \cdot \frac{1}{R} \cdot \frac{1}{2\Pi f_C} = 8.20nF$$

$$C_3 = 0.309 \cdot \frac{1}{R} \cdot \frac{1}{2\Pi f_C} = 1.45nF$$

$$C_4 = 3.325 \cdot \frac{1}{R} \cdot \frac{1}{2\Pi f_C} = 15.14nF$$

The attenuation of the filter is 30dB at 6.8kHz and better than 60dB at 15kHz.

The same method, referring to Tab. 2 and fig. 16, is used to design high-pass filter. In this case the damping factor is found by taking the reciprocal of the numbers in Tab. 2. For f_c = 5kHz and $C_i = C_1 = C_2 = C_3 = C_4$ = 1nF we obtain :

$$R_i = \frac{1}{0.354} \cdot \frac{1}{C} \cdot \frac{1}{2\Pi f_C} = 25.5k\Omega$$

$$R_1 = \frac{1}{0.421} \cdot \frac{1}{C} \cdot \frac{1}{2\Pi f_C} = 75.6k\Omega$$

$$R_2 = \frac{1}{1.753} \cdot \frac{1}{C} \cdot \frac{1}{2\Pi f_C} = 18.2k\Omega$$

$$R_3 = \frac{1}{0.309} \cdot \frac{1}{C} \cdot \frac{1}{2\Pi f_C} = 103k\Omega$$

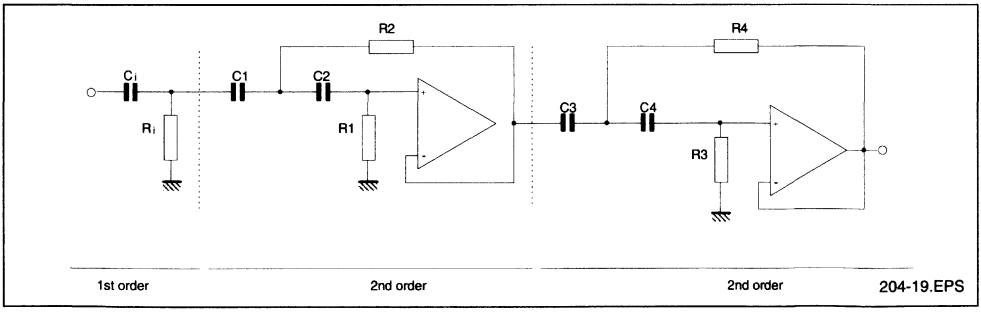
$$R_4 = \frac{1}{3.325} \cdot \frac{1}{C} \cdot \frac{1}{2\Pi f_C} = 9.6k\Omega$$

Table 2 : Damping Factor for Low-pass Butterworth Filters

Order	C_i	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
2		0.707	1.41						
3	1.392	0.202	3.54						
4		0.92	1.08	0.38	2.61				
5	1.354	0.421	1.75	0.309	3.235				
6		0.966	1.035	0.707	1.414	0.259	3.86		
7	1.336	0.488	1.53	0.623	1.604	0.222	4.49		
8		0.98	1.02	0.83	1.20	0.556	1.80	0.195	5.125

204-06.TBL

Figure 16 : 5th Order High-pass Filter (Butterworth) with Unity Gain Configuration

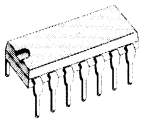


SGS-THOMSON MICROELECTRONICS

LS404

HIGH PERFORMANCE QUAD OPERATIONAL AMPLIFIERS

- SINGLE OR SPLIT SUPPLY OPERATION
- LOW POWER CONSUMPTION
- SHORT CIRCUIT PROTECTION
- LOW DISTORTION, LOW NOISE
- HIGH GAIN-BANDWIDTH PRODUCT
- HIGH CHANNEL SEPARATION



N
DIP14
(Plastic Package)

D
SO14
(Plastic Micropackage)

DESCRIPTION

The LS404 is a high performance quad operational amplifier with frequency and phase compensation built into the chip. The internal phase compensation allows stable operation as voltage follower in spite of its high gain-bandwidth products.

The circuit presents very stable electrical characteristics over the entire supply voltage range, and it particularly intended for professional and telecom applications (active filters, etc).

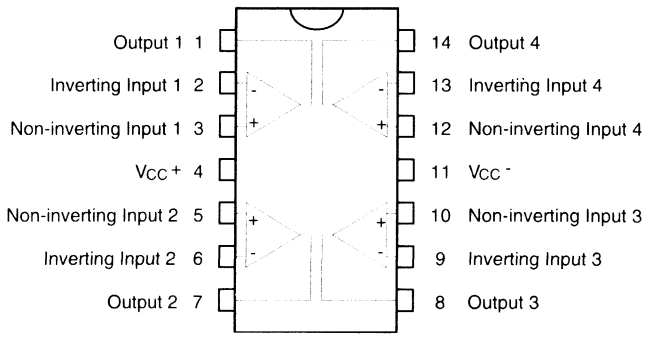
The patented input stage circuit allows small input signal swings below the negative supply voltage and prevents phase inversion when the inputs is over driver.

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
LS404C	0°C, +70°C	•	•
LS404I	-40°C, +105°C	•	•
LS404M	-55°C, +125°C	•	•

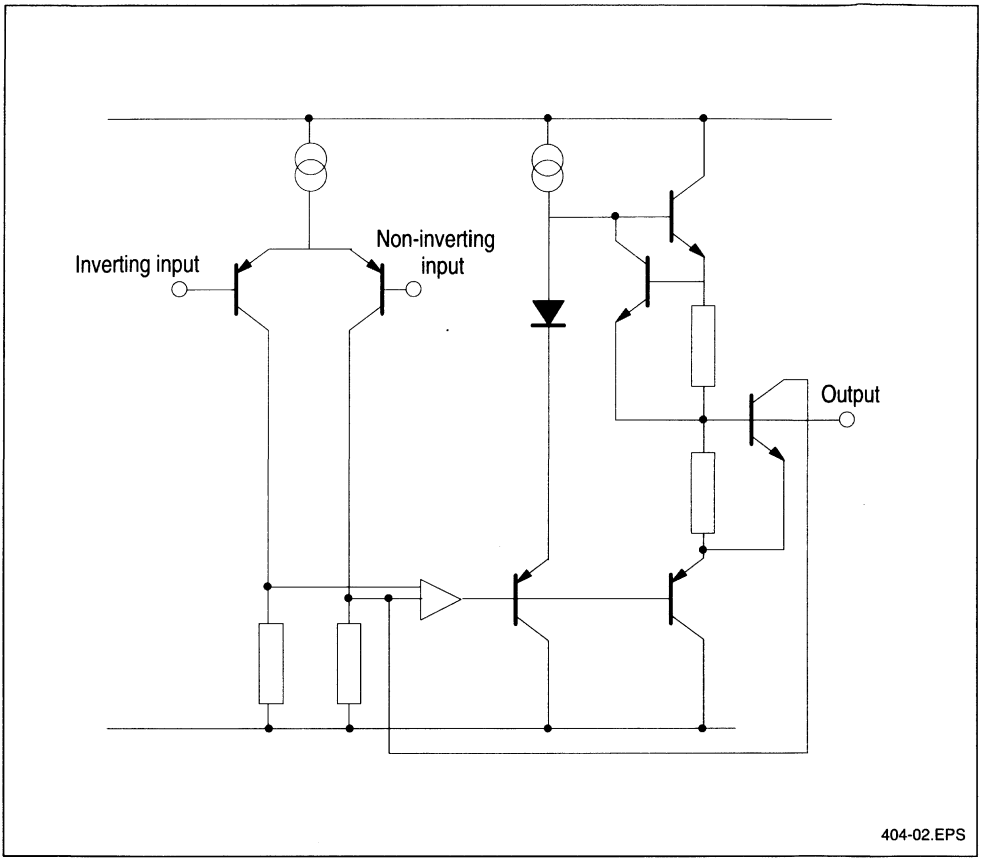
404-01.TBL

PIN CONNECTIONS (top view)



404-01.EPS

EQUIVALENT SCHEMATIC DIAGRAM (1/4 LS404)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		±18	V
V_i	Input Voltage	(positive) (negative)	$+V_{CC}$ $-V_{CC}$ - 0.5	V
V_{id}	Differential Input Voltage		± (V_{CC} - 1)	
T_{oper}	Operating Temperature Range	LS404C LS404I LS404M	0 to +70 -40 to +105 -55 to +125	°C
P_{tot}	Power Dissipation at T_{amb} = 70°C		400	mW
T_{stg}	Storage Temperature		-65 to 150	°C

404-03.TBL

ELECTRICAL CHARACTERISTICS (V_{CC} = ±15V, T_{amb} = 25°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	LS404I - LS404M			LS404C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{CC}	Supply Current			1.3	2		1.5	3	mA
I_{ib}	Input Bias Current			50	200		100	300	nA
R_i	Input Resistance	f = 1kHz		1			1		MΩ
V_{io}	Input Offset Voltage	$R_s \leq 10k\Omega$		0.7	2.5		0.5	5	mV
DV_{io}	Input Offset Voltage Drift	$R_s \leq 10k\Omega$ $T_{min.} < T_{op} < T_{max.}$		5			5		µV/°C
I_{io}	Input Offset Current			10	40		20	80	nA
DI_{io}	Input Offset Current Drift	$T_{min.} < T_{op} < T_{max.}$		0.08			0.1		$\frac{nA}{°C}$
I_{os}	Output Short Circuit Current			23			23		mA
A_{vd}	Large Signal Voltage Gain	R_L = 2kΩ V_{CC} = ±15V V_{CC} = ±4V	90	100 95		86	100 95		dB
GBP	Gain-bandwidth Product	f = 100kHz	1.8	3		1.5	2.5		MHz
e_n	Equivalent Input Noise Voltage	f = 1kHz R_s = 50Ω R_s = 1kΩ R_s = 10kΩ		8 10 18	15		10 12 20		$\frac{nV}{\sqrt{Hz}}$
THD	Total Harmonic Distortion	Unity Gain R_L = 2kΩ, V_O = $2V_{pp}$ f = 1kHz f = 20kHz		0.01 0.03	0.4		0.01 0.03		%
$\pm V_{opp}$	Output Voltage Swing	R_L = 2kΩ V_{CC} = ±15V V_{CC} = ±4V	±13	±3		±13	±3		V
V_{opp}	Large Signal Voltage Swing	f = 10kHz R_L = 10kΩ R_L = 1kΩ		22 20			22 20		V_{PP}
SR	Slew Rate	Unity Gain, R_L = 2kΩ	0.8	1.5			1		V/µs
CMR	Common Mode Rejection Ratio	V_{ic} = 10V	90	94		80	90		dB
SVR	Supply Voltage Rejection Ratio	V_{ic} = 1V f = 100Hz	90	94		86	90		dB
V_{O1}/V_{O2}	Channel Separation	f = 1kHz	100	120			120		dB

404-03.TBL

Figure 1: Supply Current versus Supply Voltage

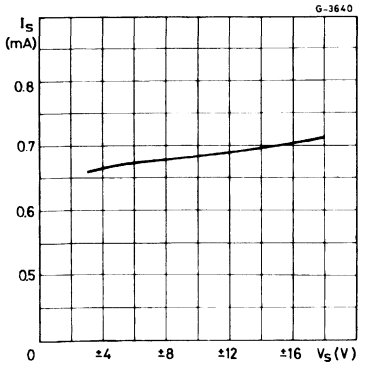


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Figure 2 : Supply Current versus Ambient Temperature

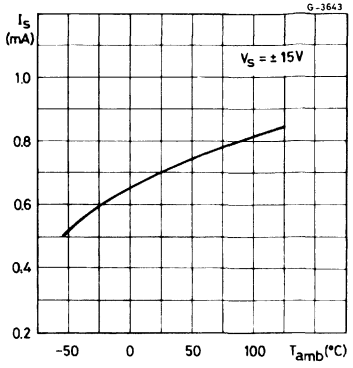

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Figure 3 : Output Short Circuit Current versus Ambient Temperature

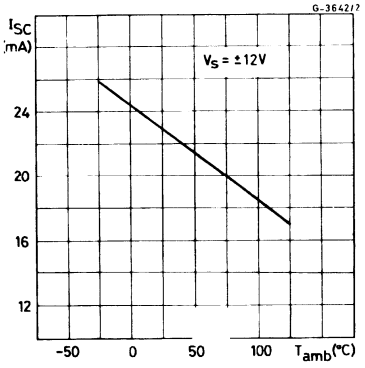

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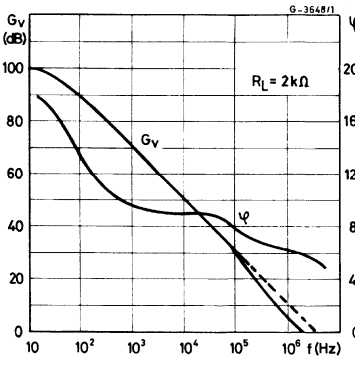
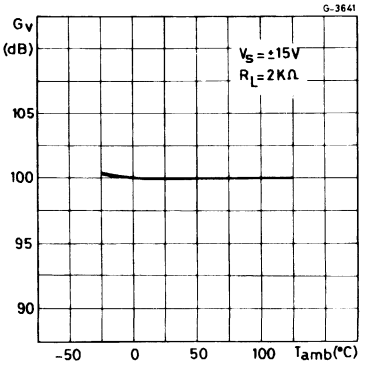
Figure 4 : Open Loop Frequency and Phase Response



404-06.EPS

Figure 5 : Output Loop Gain versus Ambient Temperature



404-07.EPS

Figure 6 : Supply Voltage Rejection versus Frequency

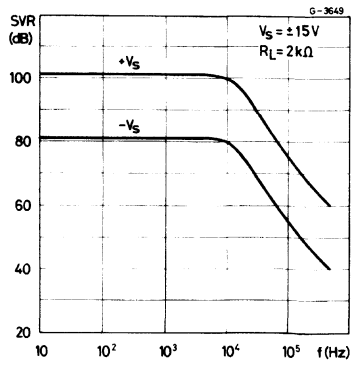


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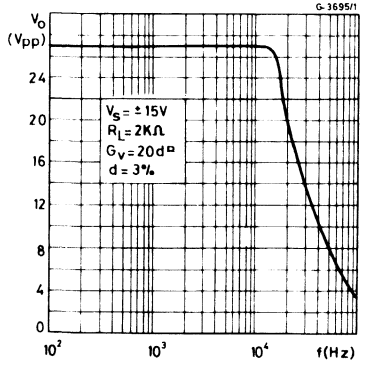
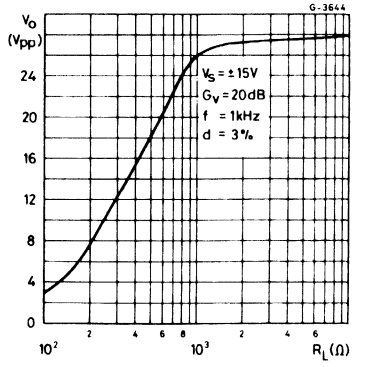
Figure 7: Large Signal Frequency Response



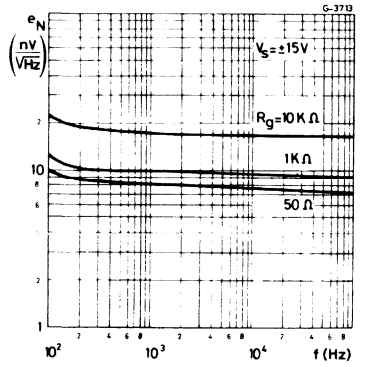
404-09.EPS

Figure 8 : Output Voltage Swing versus Load Resistance



404-10.EPS

Figure 9 : Total Input Noise versus Frequency



404-11.EPS

Figure 10 : Amplitude Response

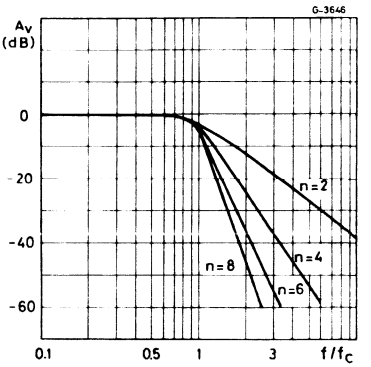


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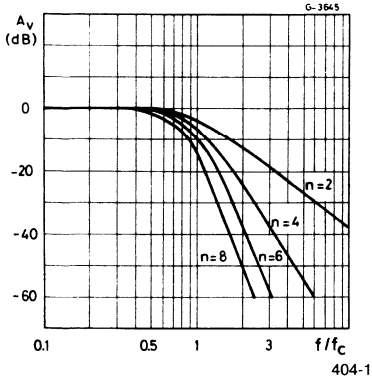
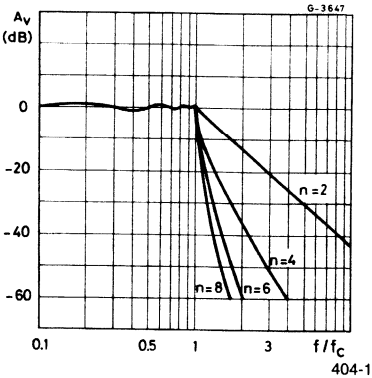
Figure 11 : Amplitude Response



404-13.EPS

Figure 12 : Amplitude Response (±1dB ripple)



404-14.EPS

APPLICATION INFORMATION : Active low-pass filter

BUTTERWORTH

The Butterworth is a "maximally flat" amplitude response filter. Butterworth filters are used for filtering signals in data acquisition systems to prevent aliasing errors in sampled-data applications and for general purpose low-pass filtering.

The cut-off frequency f_c, is the frequency at which the amplitude response is down 3dB. The attenuation rate beyond the cutoff frequency is -n6 dB per octave of frequency where n is the order (number of poles) of the filter.

Other characteristics :

- Flattest possible amplitude response.
- Excellent gain accuracy at low frequency end of passband.

BESSEL

The Bessel is a type of "linear phase" filter. Because of their linear phase characteristics, these filters approximate a constant time delay over a limited frequency range. Bessel filters pass transient waveforms with a minimum of distortion. They are also used to provide time delays for low pass filtering of modulated waveforms and as a "running average" type filter.

The maximum phase shift is $\frac{-n\Pi}{2}$ radians where n is the order (number of poles) of the filter. The cut-off frequency fc, is defined as the frequency at which the phase shift is one half of this value. For accurate delay, the cut-off frequency should be twice the maximum signal frequency.

The following table can be used to obtain the -3dB frequency of the filter.

	2 pole	4 Pole	6 Pole	8 Pole
–3dB Frequency	$0.77f_c$	$0.67f_c$	$0.57f_c$	$0.50f_c$

Other characteristics :

- Selectivity not as great as Chebyschev or Butterworth.
- Very little overshoot response to step inputs.
- Fast rise time.

CHEBYSCHEV

Chebyschev filters have greater selectivity than either Bessel or Butterworth at the expense of ripple in the passband.

Chebyschev filters are normally designed with peak-to-peak ripple values from 0.2dB to 2dB.

Increased ripple in the passband allows increased attenuation above the cut-off frequency.

The cut-off frequency is defined as the frequency at which the amplitude response passes through the specified maximum ripple band and enters the stop band.

Other characteristics :

- Greater selectivity
- Very non-linear phase response
- High overshoot response to step inputs

The table below shows the typical overshoot and settling time response of the low pass filters to a step input.

	Number of Poles	Peak Overshoot	Settling Time (% of final value)		
		% Overshoot	±1%	±0 .1%	±0 0.1%
Butterworth	2	4	$1.1/f_c$sec.	$1.7/f_c$sec.	$1.9/f_c$sec.
	4	11	$1.7/f_c$	$2.8/f_c$	$3.8/f_c$
	6	14	$2.4/f_c$	$3.9/f_c$	$5.0/f_c$
	8	16	$3.1/f_c$	$5.1/f_c$	$7.1/f_c$
Bessel	2	0.4	$0.8/f_c$	$1.4/f_c$	$1.7/f_c$
	4	0.8	$1.0/f_c$	$1.8/f_c$	$2.4/f_c$
	6	0.6	$1.3/f_c$	$2.1/f_c$	$2.7/f_c$
	8	0.3	$1.6/f_c$	$2.3/f_c$	$3.2/f_c$
Chebyschev (ripple ±0.25dB)	2	11	$1.1/f_c$	$1.6/f_c$	–
	4	18	$3.0/f_c$	$5.4/f_c$	–
	6	21	$5.9/f_c$	$10.4/f_c$	–
	8	23	$8.4/f_c$	$16.4/f_c$	–
Chebyschev (ripple ±1dB)	2	21	$1.6/f_c$	$2.7/f_c$	–
	4	28	$4.8/f_c$	$8.4/f_c$	–
	6	32	$8.2/f_c$	$16.3/f_c$	–
	8	34	$11.6/f_c$	$24.8/f_c$	–

Design of 2nd order active low pass filter (Sallen and Key configuration unity gain-op-amp)

Fixed R = R1 = R2, we have (see fig. 13).

$$C1 = \frac{1}{R}\,\frac{\xi}{\omega_c}$$

$$C2 = \frac{1}{R}\,\frac{1}{\xi\omega_c}$$

The diagram of fig.14 shows the amplitude response for different values of damping factor ξ in 2nd order filters.

Figure 13 : Filter Configuration

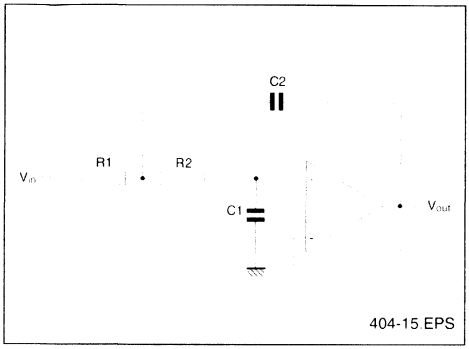
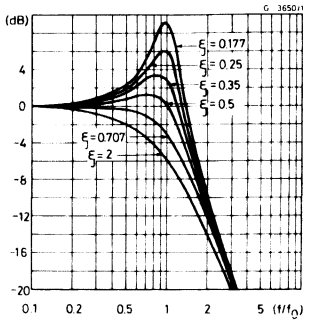


Figure 14 : Filter Respons versus Damping Factor



Three parameters are needed to characterize the frequency and phase response of a 2nd order active filter : the gain (G_v), the damping factor (ξ) or the Q-factor ($Q = (2\,\xi)^{-1}$). and the cut-off frequency (f_c).

The higher order responses are obtained with a series of 2nd order sections. A simple RC section is introduced when an odd filter is required.

The choice of 'ξ' (or Q-factor) determines the filter response (see table 1).

Table 1

Filter Response	ξ	Q	Cutoff Frequency f_c
Bessel	$\frac{\sqrt{3}}{2}$	$\frac{\sqrt{1}}{3}$	Frequency at which Phase Shift is -90°C
Butterworth	$\frac{\sqrt{2}}{2}$	$\frac{\sqrt{1}}{2}$	Frequency at which G_V = -3dB
Chebyschev	$\frac{\sqrt{2}}{2}$	$\frac{\sqrt{1}}{2}$	Frequency at which the amplitude response passes through specified max. ripple band and enters the stop band.

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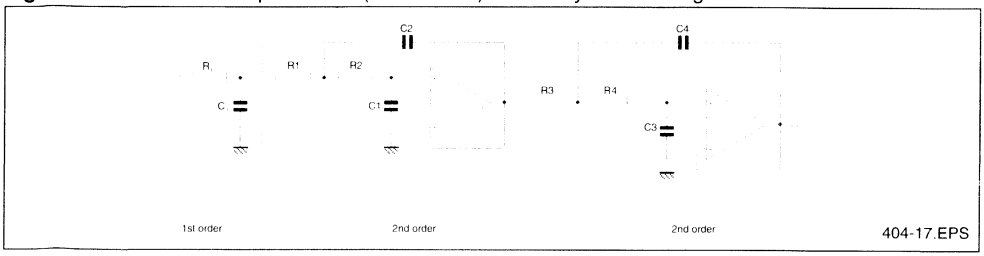
EXAMPLE

Figure 15 : 5th Order Low-pass Filter (Butterworth) with Unity Gain Configuration



In the circuit of fig. 15, for $f_c = 3.4kHz$ and $R_i = R_1 = R_2 = R_3 = R_4 = 10k\Omega$, we obtain :

$$C_i = 1.354 \cdot \frac{1}{R} \cdot \frac{1}{2\Pi f_C} = 6.33nF$$

$$C_1 = 0.421 \cdot \frac{1}{R} \cdot \frac{1}{2\Pi f_C} = 1.97nF$$

$$C_2 = 1.753 \cdot \frac{1}{R} \cdot \frac{1}{2\Pi f_C} = 8.20nF$$

$$C_3 = 0.309 \cdot \frac{1}{R} \cdot \frac{1}{2\Pi f_C} = 1.45nF$$

$$C_4 = 3.325 \cdot \frac{1}{R} \cdot \frac{1}{2\Pi f_C} = 15.14nF$$

The attenuation of the filter is 30dB at 6.8kHz and better than 60dB at 15kHz.

The same method, referring to Tab. 2 and fig. 16, is used to design high-pass filter. In this case the damping factor is found by taking the reciprocal of the numbers in Tab. 2. For $f_c = 5kHz$ and $C_i = C_1 = C_2 = C_3 = C_4 = 1nF$ we obtain :

$$R_i = \frac{1}{0.354} \cdot \frac{1}{C} \cdot \frac{1}{2\Pi f_C} = 25.5k\Omega$$

$$R_1 = \frac{1}{0.421} \cdot \frac{1}{C} \cdot \frac{1}{2\Pi f_C} = 75.6k\Omega$$

$$R_2 = \frac{1}{1.753} \cdot \frac{1}{C} \cdot \frac{1}{2\Pi f_C} = 18.2k\Omega$$

$$R_3 = \frac{1}{0.309} \cdot \frac{1}{C} \cdot \frac{1}{2\Pi f_C} = 103k\Omega$$

$$R_4 = \frac{1}{3.325} \cdot \frac{1}{C} \cdot \frac{1}{2\Pi f_C} = 9.6k\Omega$$

Table 2 : Damping Factor for Low-pass Butterworth Filters

Order	C_i	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
2		0.707	1.41						
3	1.392	0.202	3.54						
4		0.92	1.08	0.38	2.61				
5	1.354	0.421	1.75	0.309	3.235				
6		0.966	1.035	0.707	1.414	0.259	3.86		
7	1.336	0.488	1.53	0.623	1.604	0.222	4.49		
8		0.98	1.02	0.83	1.20	0.556	1.80	0.195	5.125

Figure 16 : 5th Order High-pass Filter (Butterworth) with Unity Gain Configuration

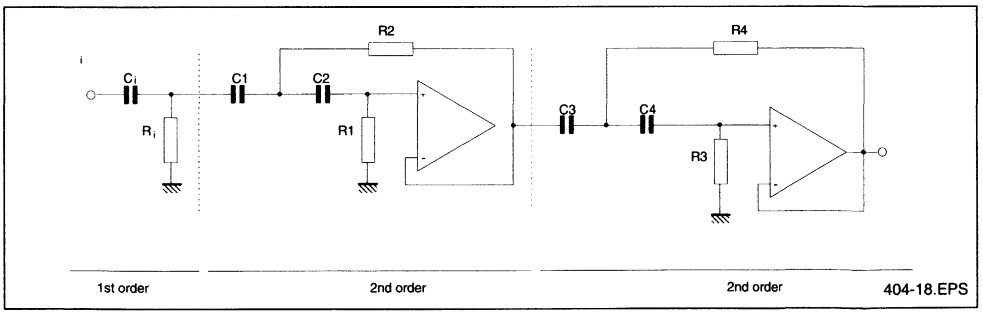


Figure 17 : Mutliple Feedback 8-pole Bandpass Filter

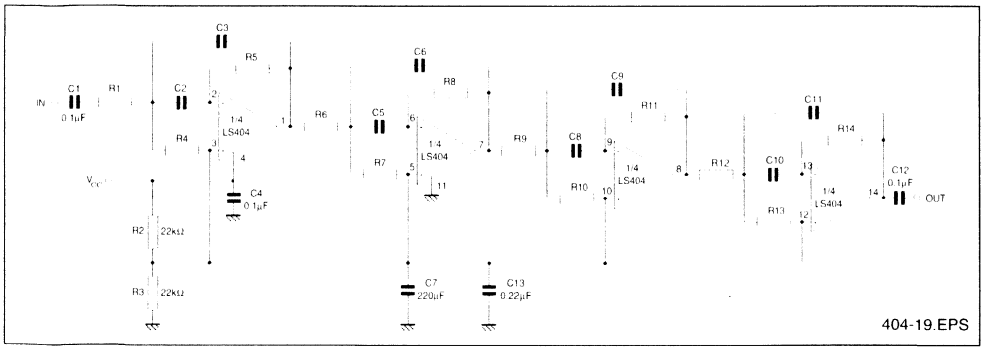


Figure 18 : Frequency Response of Bandpass Filter

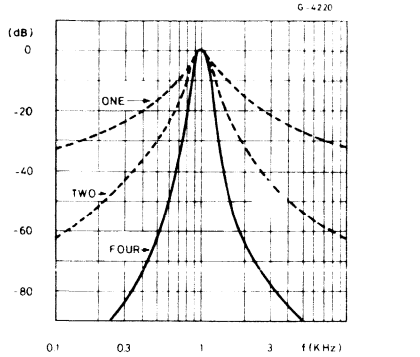


Figure 19 : Bandwidth of Bandpass Filter

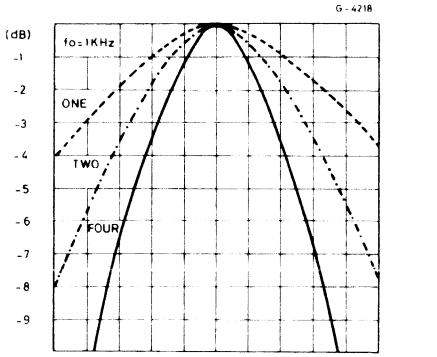
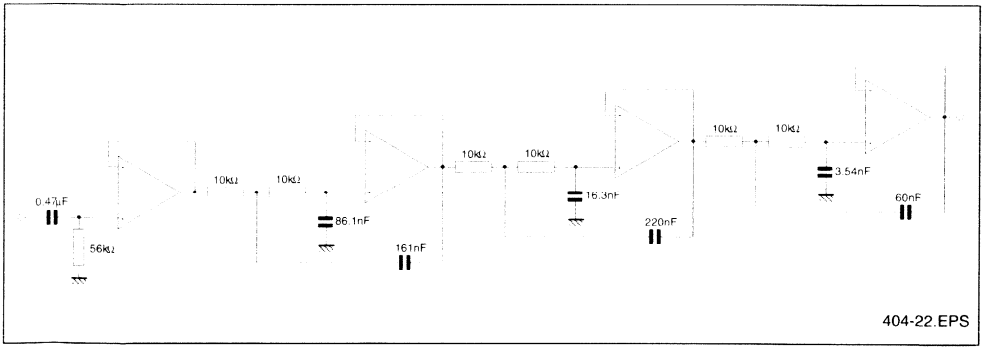
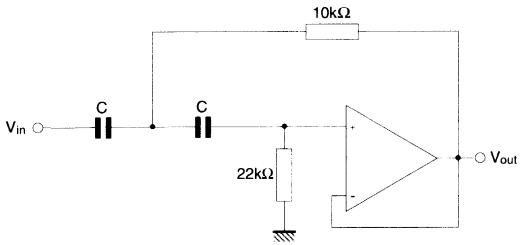


Figure 20 : Six-pole 355Hz Low-pass Filter (chebychev type)



This is a 6-pole Chebychev type with ±0.25dB ripple in the passband. A decoupling stage is used to avoid the influence of the input impedance on the filter's characteristics. The attenuation is about 55dB at 710Hz and reaches 80dB at 1065Hz. The in band attenuation is limited in practise to the ±0.25dB ripple and does not exceed 0.5dB at 0.9fc.

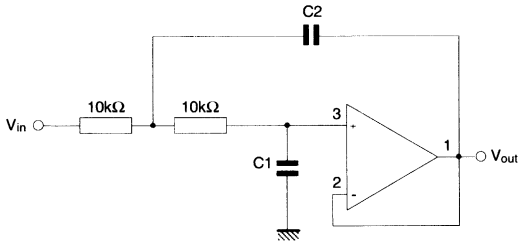
Figure 21 : Subsonic Filter (G_V = 0dB)



f_C (Hz)	C (µF)
15	0.68
22	0.47
30	0.33
55	0.22
100	0.10

404-23.EPS

Figure 22 : High Cut Filter (G_V = 0dB)



f_C (Hz)	C1 (nF)	C2 (nF)
3	3.9	6.8
5	2.2	4.7
10	1.2	2.2
15	0.68	1.5

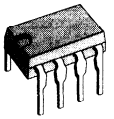
404-24.EPS

SGS-THOMSON MICROELECTRONICS

MC1458
MC1558

DUAL OPERATIONAL AMPLIFIERS

- LOW POWER CONSUMPTION
- LARGE INPUT VOLTAGE RANGE
- NO LATCH-UP
- HIGH GAIN
- SHORT-CIRCUIT PROTECTION
- NO FREQUENCY COMPENSATION REQUIRED



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

J
CERDIP8
(Cerdip Package)

H
TO99
(Metal Can)

DESCRIPTION

The MC1458 is a high performance monolithic dual operational amplifier constructed on a single silicon chip. It is intended for a wide range of analog applications.

- Summing amplifier
- Voltage follower
- Integrator
- Active filter
- Function generator

The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feed back applications.

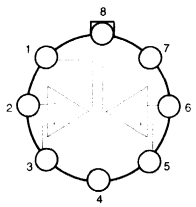
ORDER CODES

Part Number	Temperature Range	Package			
		H	N	J	D
MC1458	0, +70°C	•	•	•	•
MC1458I	–40, +105°C	•	•	•	•
MC1558	–55, +125°C	•	•	•	•
Example : MC1458H					

1458-01.TBL

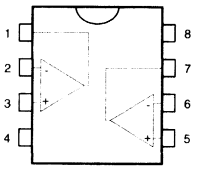
PIN CONNECTIONS (top views)

TO99



1458-01.EPS

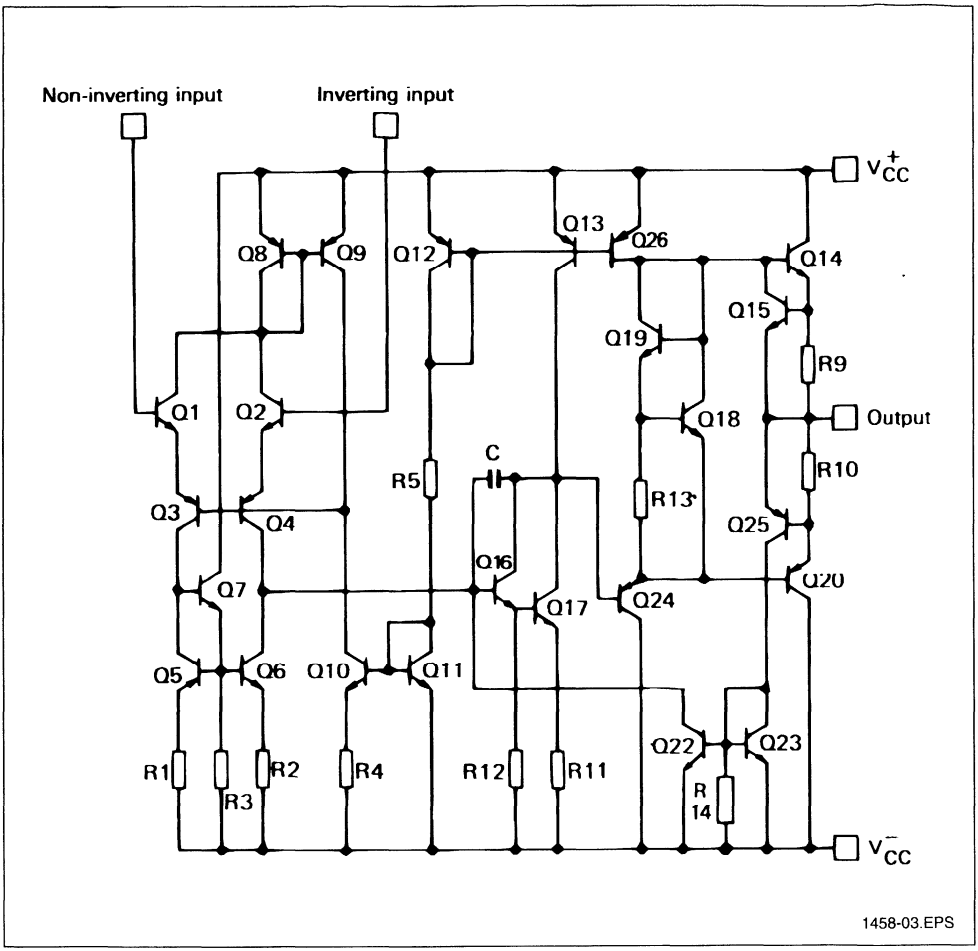
DIP8/CERDIP8
SO8



1458-02.EPS

1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^-
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - V_{CC}^+

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	MC1458	MC1458I	MC1558	Unit
V_{CC}	Supply Voltage	±22	±22	±22	V
V_i	Input Voltage	±15	±15	±15	V
V_{id}	Differential Input Voltage	±30	±30	±30	V
P_{tot}	Power Dissipation J Suffix H Suffix D Suffix N Suffix	660 660 300 500			mW
	Output Short-circuit Duration	Infinite			
T_{oper}	Operating Free-air Temperature Range	0 to +70	–40 to +105	–55 to +125	°C
T_{stg}	Storage Temperature Range	–65 to +150	–65 to +150	–65 to +150	°C

1458-02.TBL

ELECTRICAL CHARACTERISTICS

V_{CC} = ±15V, T_{amb} = 25°C, (unless otherwise specified)

Symbol	Parameter	MC1458 - 1458I - 1558			Unit
		Min.	Typ.	Max.	
V_{io}	Input Offset Voltage ($R_S \leq 10k\Omega$) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		1	5 6	mV
I_{io}	Input Offset Current T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		2	200 300	nA
I_{ib}	Input Bias Current T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		30	500 800	nA
A_{vd}	Large Signal Voltage Gain (V_O = ±10V, R_L = 2kΩ) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	50 25	200		V/mV
SVR	Supply Voltage Rejection Ratio ($R_S \leq 10k\Omega$) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	77 77	90		dB
I_{CC}	Supply Current, all Amp, no Load T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		2.3	5 6	mA
V_{icm}	Input Common Mode Voltage Range T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	±12 ±12			V
CMR	Common-mode Rejection Ratio ($R_S \leq$ 10 kΩ) T_{amb} = 25°C $T_{min} \leq T_{amb} \leq T_{max}$	70 70	90		dB
I_{OS}	Output Short-circuit Current T_{amb} = 25°C	10	20	35	mA
$\pm V_{OPP}$	Output Voltage Swing T_{amb} = 25°C R_L = 10kΩ R_L = 2kΩ $T_{min.} \leq T_{amb} \leq T_{max.}$ R_L = 10kΩ R_L = 2kΩ	12 10 12 10	14 13		V
SR	Slew Rate (V_I = ±10V, R_L = 2kΩ,C_L = 100pF, T_{amb} = 25°C, unity gain)	0.2	0.8		V/µs
t_r	Rise Time (V_I = 20mV, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)		0.3		µs
K_{OV}	Overshoot (V_I = 20mV, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)		5		%
R_I	Input Resistance	0.3	2		MΩ
Zic	Common-mode Input Impedance		200		MΩ
C_I	Input Capacitance		1.4		pF
R_O	Output Resistance		75		Ω
Bom	Large Signal Bandwidth (R_L = 2kΩ, $V_O \geq$ ±10V, A_{VD} = 1, THD ≤ 5%)		14		KHz
f_T	Transition Frequency (V_I = 10mV, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C)		1		MHz

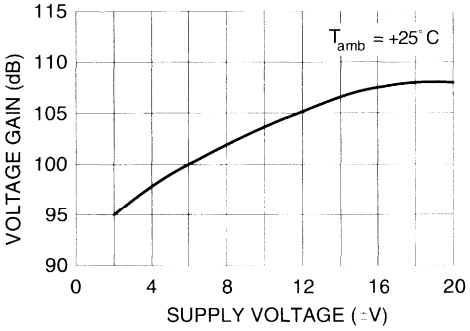
1458-03.TBL

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	MC1458 - 1458I MC1558			Unit
		Min.	Typ.	Max.	
GBP	Gain Bandwidth Product (V_I = 10mV, R_L = 2kΩ, C_L = 100pF, f = 100kHz, T_{amb} = 25°C)	0.4	1		MHz
THD	Total Harmonic Distortion (f = 1kHz, A_V = 20dB, R_L = 2kΩ, V_O = $2V_{PP}$, C_L = 100pF, T_{amb} = 25°C)		0.02		%
e_n	Equivalent Input Noise Voltage (f = kHz, R_s = 100Ω)		45		$\frac{nV}{\sqrt{Hz}}$
∅m	Phase Margin		65		Degrees
Am	Gain Margin		11		dB
V_{O1}/V_{O2}	Channel Separation		120		dB

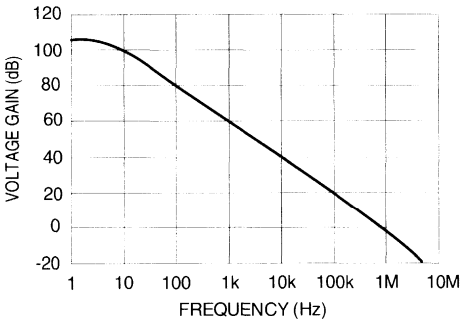
1458-04.TBL

OPEN LOOP VOLTAGE GAIN



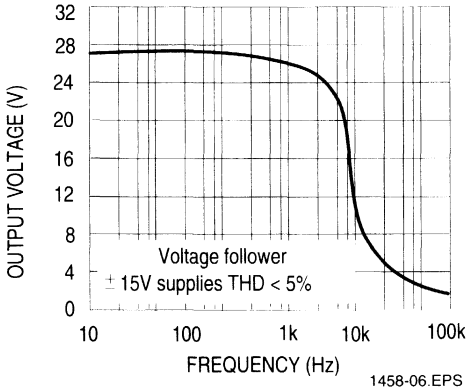
1458-04.EPS

OPEN LOOP FREQUENCY RESPONSE



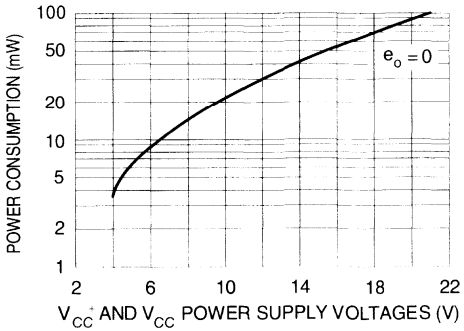
1458-05.EPS

POWER BANDWIDTH (LARGE SIGNAL SWING)



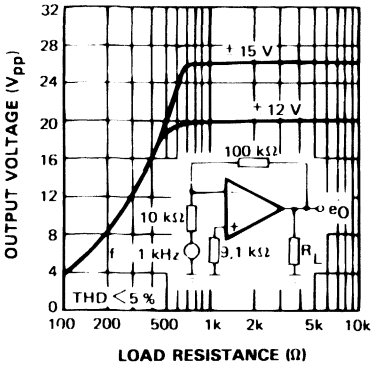
1458-06.EPS

POWER CONSUMPTION

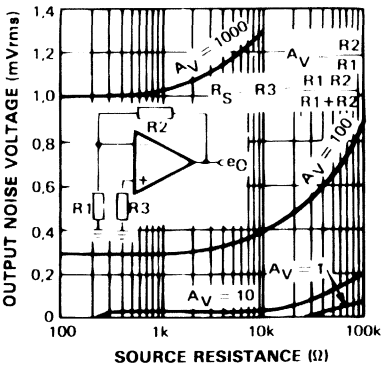


1458-07.EPS

OUTPUT VOLTAGE SWING

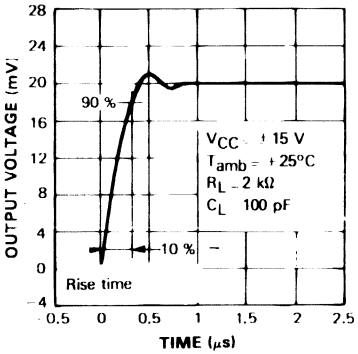


OUTPUT NOISE VOLTAGE

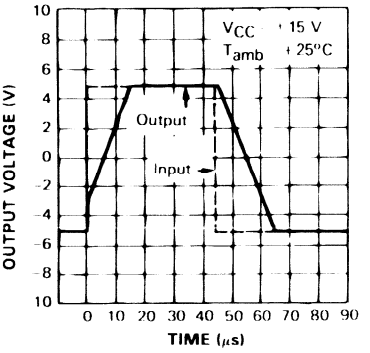


1458-08.EPS

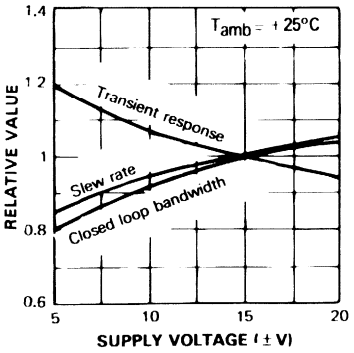
TRANSIENT RESPONSE



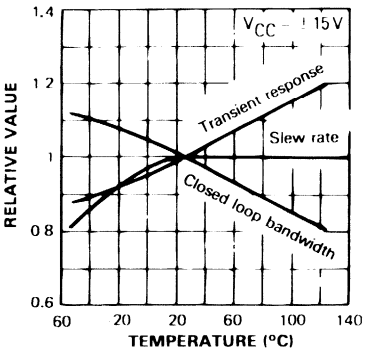
VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



FREQUENCY CHARACTERISTICS



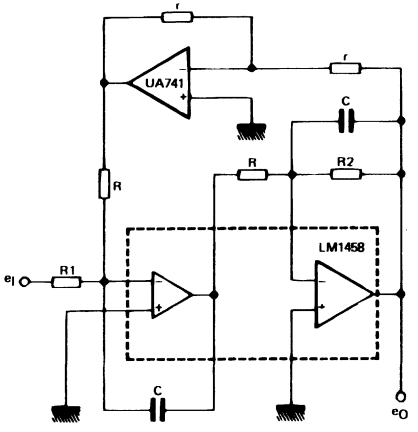
FREQUENCY CHARACTERISTICS



1458-09.EPS

TYPICAL APPLICATIONS

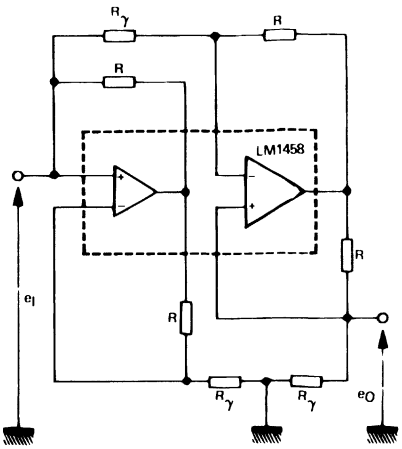
LOW PASS FILTER



$\omega_O = \frac{1}{RC}$ $\xi = \frac{1}{2}\frac{R}{R2}$ $A_V = \frac{R}{R1}$

1458-10.EPS

GIRATOR

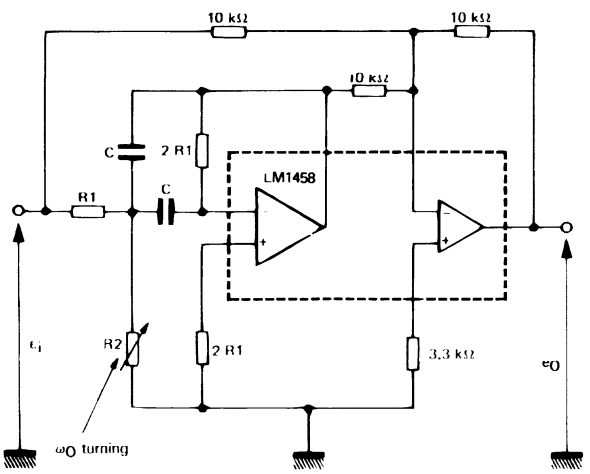


R_γ : Gyration resistance (≥ 1.5 kΩ)

$0.1\ R_\gamma \leq R \leq 0.5\ R_\gamma$

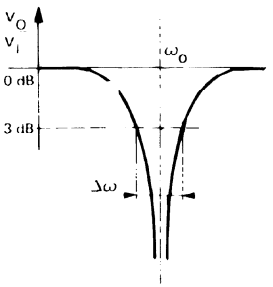
1458-11.EPS

TURNABLE NOTCH FILTER



$$\omega_O = \frac{1}{C\sqrt{2\,R1\,\frac{R1\ R2}{R1 + R2}}}$$

$$\Delta\omega = \frac{1}{CR1} \quad \text{(Bandwidth notched)}$$



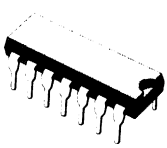
1458-12.EPS

SGS-THOMSON MICROELECTRONICS

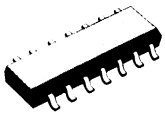
MC1488

RS232C QUAD LINE DRIVER

- CURRENT LIMITED OUTPUT ± 10 mA TYP.
- POWER-OFF SOURCE IMPEDANCE 300 ΩMIN.
- SIMPLE SLEW RATE CONTROL WITH EXTERNAL CAPACITOR
- FLEXIBLE OPERATING SUPPLY RANGE
- INPUTS ARE TTL AND μP COMPATIBLE



DIP-14 (0.25)
(Plastic and Ceramic)



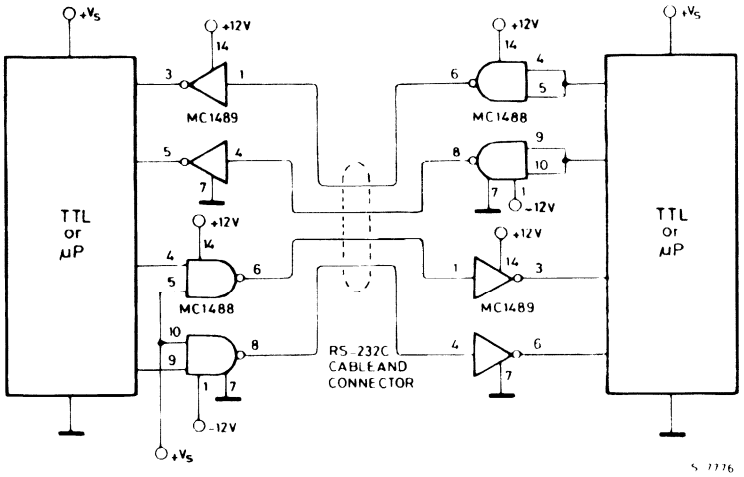
SO-14J

DESCRIPTION

The MC1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS232C.

ORDER CODES : MC1488P (Plastic DIP)
MC1488L (Ceramic DIP)
MC1488D (SO-14)

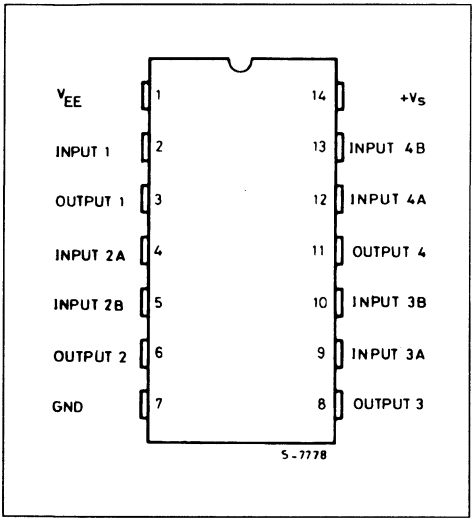
TYPICAL APPLICATION : RS232C Data Transmission.



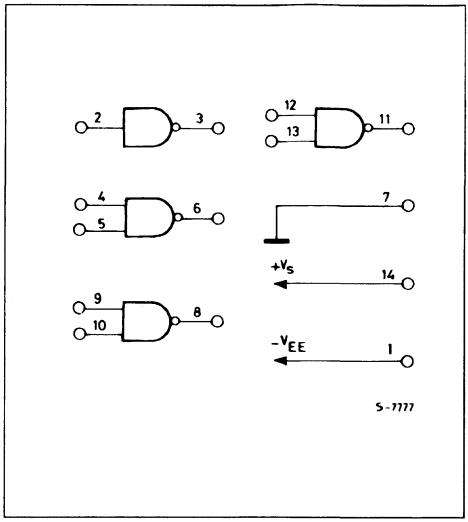
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Power Supply Voltage	15	V
V_{EE}	Power Supply Voltage	− 15	V
V_{IR}	Input Voltage Range	$-15 \leq V_{IR} \leq 7$	V
V_O	Output Signal Voltage	± 15	V
T_{amb}	Operating Ambient Temperature	0 to 75	°C
T_{stg}	Storage Temperature Range	− 65 to 150	°C

CONNECTION DIAGRAMS (top views)



LOGIC DIAGRAM



THERMAL DATA

			Plastic DIP - 14	Ceramic DIP - 14	SO - 14
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	max	200 °C/W	165 °C/W	165 °C/W

ELECTRICAL CHARACTERISTICS (V_S = 9 ±10 % V, V_{EE} = − 9 ±10 % V, T_{amb} = 0 to 75 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{IL}	Input Current	Low Logic State (V_{IL} = 0V)		1	1.6	mA	1
I_{IH}	Input Current	High Logic State (V_{IH} = 5V)			10	µA	1
V_{OH}	Output Voltage	High Logic State R_L = 3KΩ V_{IL} = 0.8V, V_S = 9V, V_{EE} = −9V V_{IL} = 0.8V, V_S = 13.2V, V_{EE} = −13.2V	 6 9	 7 10.5	 	 V V	 2 2
V_{OL}	Output Voltage	Low Logic State R_L = 3 KΩ V_{IH} = 1.9V, V_{EE} = −9V, V_S = 9V V_{IH} = 1.9V, V_{EE} = −13.2V, V_S = 13.2V	 − 6 − 9	 − 7 − 10.5	 	 V V	 2 2
I_{OS+} *	Positive Output Short - circuit Current		6	10	12	mA	3
I_{OS-} *	Negative Output Short-circuit Current		− 6	− 10	− 12	mA	3
R_O	Output Resistance	V_S = V_{EE} = 0 |Vo| = ± 2V	300			Ω	4
I_s	Positive Supply Current (R_i = ∞)	V_{IH} = 1.9 V V_S = 9 V V_{IL} = 0.8 V V_S = 9 V V_{IH} = 1.9 V V_S = 12 V V_{IL} = 0.8 V V_S = 12 V V_{IH} = 1.9 V V_S = 15 V V_{IL} = 0.8 V V_S = 15 V		15 4.5 19 5.5	20 6 25 7 34 12	mA	5
I_{EE}	Negative Supply Current (R_L = ∞)	V_{IH} = 1.9 V V_{EE} = − 9 V V_{IL} = 0.8 V V_{EE} = − 9 V V_{IH} = 1.9 V V_{EE} = − 12 V V_{IL} = 0.8 V V_{EE} = − 12 V V_{IH} = 1.9 V V_{EE} = − 15 V V_{IL} = 0.8 V V_{EE} = − 15 V		− 13 − 18	− 17 − 15 − 23 − 15 − 34 − 2.5	mA µA mA µA mA mA	5
P_c	Power Consumption	V_S = 9 V V_{EE} = − 9 V V_S = 12 V V_{EE} = − 12 V			333 567	mW	

SWITCHING CHARACTERISTICS (V_S = ± 9 ±1 % V, V_{EE} = − 9 ± 1 % V, T_{amb} = 25 °C)

t_{PLH}	Propagation Delay Time	Z_i = 3 KΩ and 15 pF		275	350	ns	6
t_{THL}	Fall Time	Z_i = 3 KΩ and 15 pF		45	75	ns	6
t_{PHL}	Propagation Delay Time	Z_i = 3 KΩ and 15 pF		110	175	ns	6
t_{TLH}	Rise Time	Z_i = 3 KΩ and 15 pF		55	100	ns	6

* Maximum package power dissipation may be exceeded if all outputs are shorted simultaneously

TEST CIRCUITS

Figure 1 : Input Current.

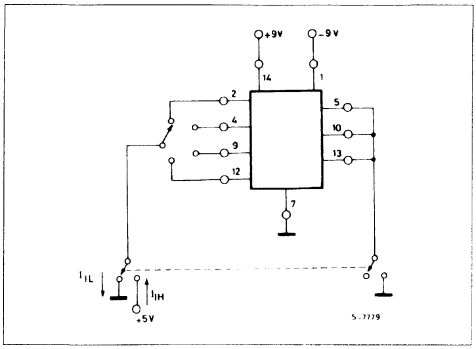


Figure 2 : Output Voltage.

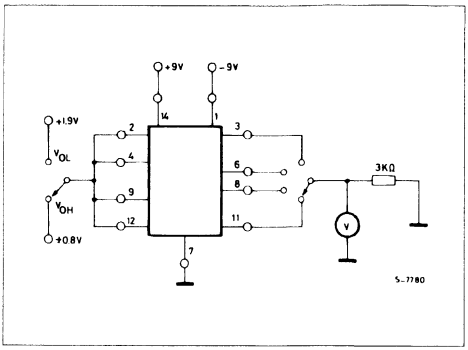


Figure 3 : Output Short-Circuit Current.

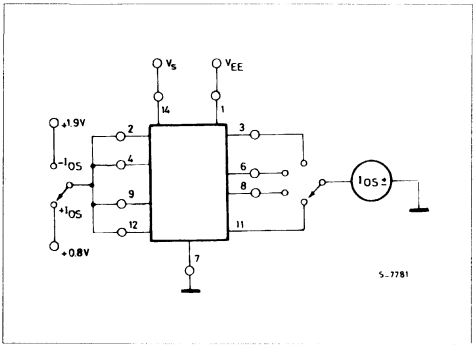


Figure 4 : Output Resistance (power off).

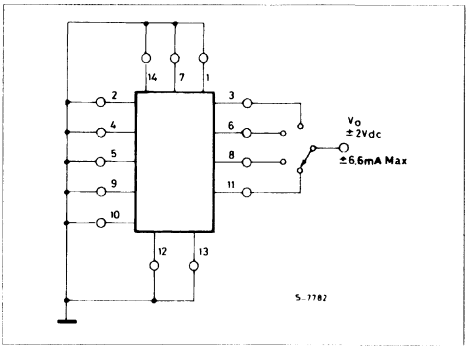


Figure 5 : Power Supply Currents.

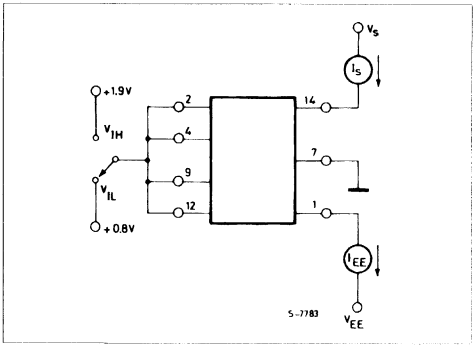


Figure 6 : Switching Response.

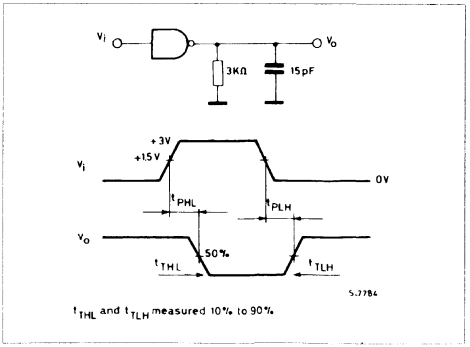


Figure 7 : Transfer Characteristics vs. Power Supply Voltage.

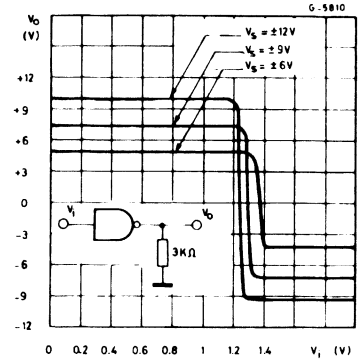


Figure 8 : Short-Circuit Output Current vs. Temperature.

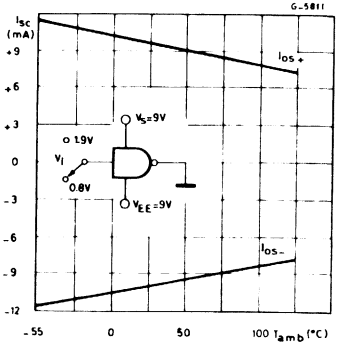


Figure 9 : Output Slew-Rate Load Capacitance.

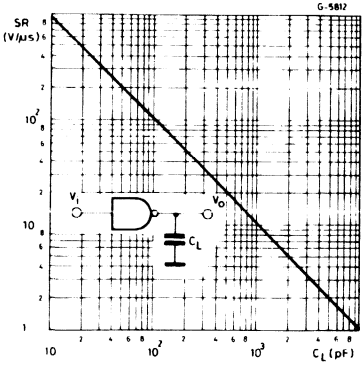


Figure 10 : Output Voltage and Current-Limiting Characteristics.

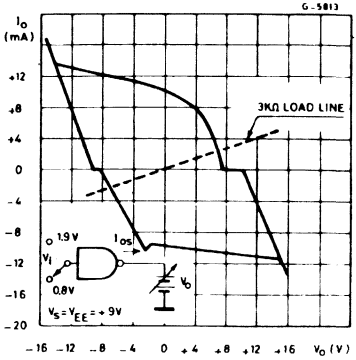
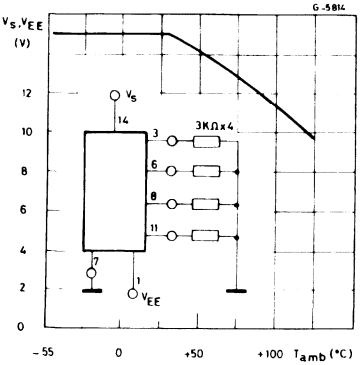


Figure 11 : Maximum Operating Temperature vs. Power-Supply Voltage.



APPLICATION INFORMATION

The Electronic Industries Association (EIA) has released the RS232C specification detailing the requirements for the interface between data processing equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS232C defined levels. The RS232C requirements as applied to drivers are discussed herein.

The required driver voltages are defined as between 5 and 15 V in magnitude and are positive for a logic "0" and negative for a logic "1". These voltages are so defined when the drivers are terminated with a 3000 to 7000Ω resistor. The MC1488 meets this voltage requirement by converting a DTL/TTL logic level into RS232C levels with one stage of inversion.

The RS232C specification further requires that during transitions, the driver output slew rate must not exceed 30 V per µs. The inherent slew rate of the MC1488 is much too fast for this requirement. The current limited output of the device can be used to control this slew rate by connecting a capacitor to each driver output. The required capacitor can be easily determined by using the relationship $C = I_{OS} \times \Delta T / \Delta V$ from which Figure 12 is derived. Accordingly, a 330 pF capacitor on each output will guarantee a worst case slew rate of 30 V per µs.

The interface driver is also required to withstand an accidental short to any other conductor in an interconnecting cable. The worst possible signal on any conductor would be another driver using a plus or minus 15 V, 500 mA source. The MC1488 is designed to indefinitely withstand such a short to all four outputs in a package as long as the power-supply voltages are greater than 9.0 V (i.e., VS ≥ 9.0 V ; $V_{EE} \leq$ - 9.0 V). In some power-supply designs, a loss of system power causes a low impedance on the power-supply outputs. When this occurs, a low impedance to ground would exist at the power inputs to the MC1488 effectively shorting the 300Ω output resistor to ground. If **all four outputs** were then shorted to plus or minus 15 V, the power dissipation in these resistors would be excessive. Therefore, if the system is designed to permit low impedances to ground at the power-suppies of the drivers, a diode should be placed in each power-supply lead to prevent over-heating in this fault condition. These two diodes, as shown in Figure 13, could be used to decouple all the driver packages in a system. (These same diodes will allow the MC1488 to withstand momentary shorts to the ±15 V limits specified in the earlier Standard RS232B). The addition of the diodes also permits the MC1488 to withstand faults with power-supplies of less than the 9.0 V stated above.

The maximum short-circuit current allowable under fault conditions is more than guaranteed by the previously mentioned 10 mA output current limiting.

Figure 12 : Slew Rate vs. Capacitance for I_{SC} = 10mA.

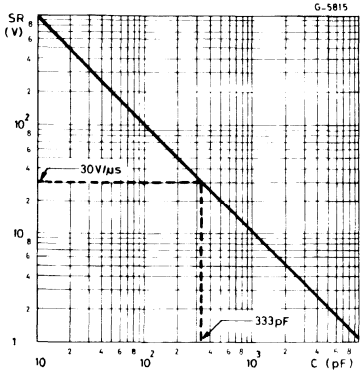
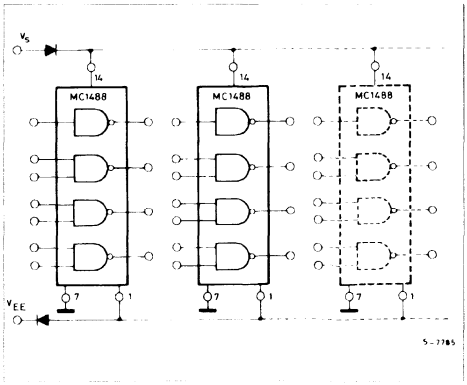


Figure 13 : Power Supply Protection to Meet Power-off Fault Conditions.



OTHER APPLICATION

The MC1488 is an extremely versatile line driver with a miriad of possible applications. Several features of the drivers enhance this versatility :

1. Output Current Limiting - this enables the circuit designer to define the ouptut voltage levels independent of power-supplies and can be accomplished by diode clamping of the output pins.

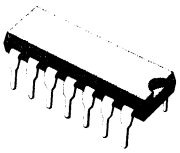
2. Power-Supply Range - as can be seen from the schematic drawing of the drivers, the positive and negative driving elements of the device are essentially independent and do not require matching power-supplies. In fact, the positive supply can very from a minimum seven volts (required for driving the negative pulldown section) to the maximum specified 15 V. The negative supply can vary from approximately - 2.5 V to the minimum specified - 15 V. The MC1488 will drive the ouptut to within 2 V of the positive or negative supplies as long as the current output limits are not exceeded. The combination of the current-limiting and supply-voltage features allow a wide combination of possible outputs within the same quad package.

SGS-THOMSON
MICROELECTRONICS

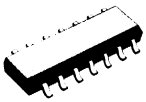
MC1489
MC1489A

QUAD LINE RECEIVERS

- INPUT RESISTANCE –3.0 K to 7.0 KΩ
- INPUT SIGNAL RANGE – ± 30 V
- INPUT THRESHOLD HYSTERESIS BUILT-IN
- RESPONSE CONTROL :
  a) LOGIC THRESHOLD SHIFTING
  b) INPUT NOISE FILTERING



DIP-14
(Plastic (0.25) and Ceramic)



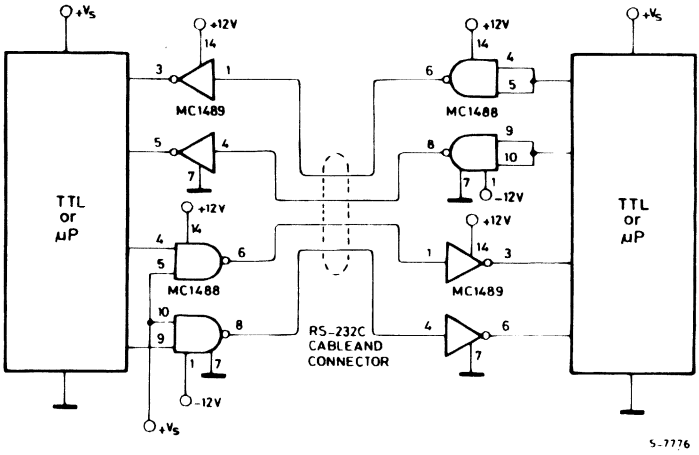
SO-14J

ORDER CODES : MC1489L, MC1489AL
(DIP–14 Ceramic)
MC1489P, MC1489AP
(DIP–14 Plastic)
MC1489D, MC1489AD (SO-14)

DESCRIPTION

The MC1489 monolithic quad line receivers are designed to interface data therminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

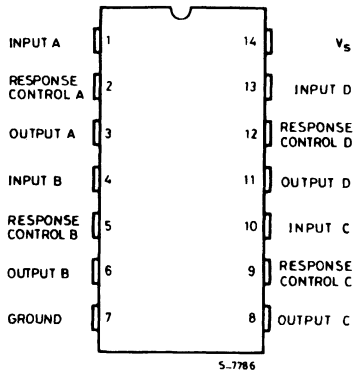
TYPICAL APPLICATION : RS232C Data Transmission



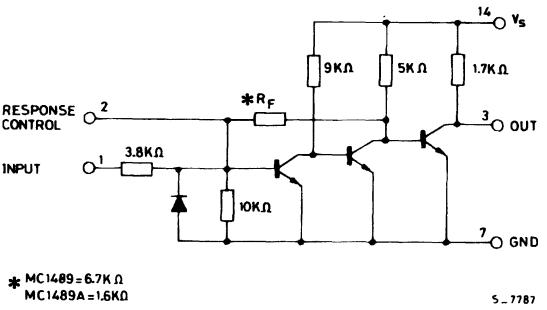
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Power Supply Voltage	10	V
V_I	Input Voltage Range	± 30	V
I_{OL}	Output Load Current	20	mA
P_{tot}	Power Dissipation	1	W
T_{amb}	Operating Ambient Temperature	0 to 75	°C
T_{stg}	Storage Temperature Range	– 65 to 150	°C

CONNECTION DIAGRAMS (top view)



SCHEMATIC DIAGRAM (1/4 of circuit shown)



ELECTRICAL CHARACTERISTICS (Response control pin is open V_S = 5 V (± 10%) T_{amb} = 0 to 75 °C unless otherwise specified)

Symbol	Parameter	Test Condtions	Min.	Typ.	Max.	Unit
I_{IH}	Positive Input Current	V_{IH} = 25 V V_{IH} = 3 V	3.6 0.43		8.3	mA
I_{IL}	Negative Input Current	V_{IL} = 25 V V_{IL} = 3 V	3.6 0.43		8.3	mA
V_{IH}	Input Turn-on Threshold Voltage	T_{amb} = 25 ° C $V_{OL} \leq$ 0.45 I_L = 10 mA for **MC1489** for **MC1489A**	1 1.75	 1.95	1.5 2.25	V
V_{IL}	Input Turn-off Threshold Voltage	T_{amb} = 25 ° C $V_{OH} \geq$ 2.5 V I_L = 0.5 mA	0.75		1.25	V
V_{OH}	Ouptut Voltage High	V_{IH} = 0.75 V I_L = – 0.5 mA I_L = 0.5 mA Input Open Circuit	2.5 2.5	4 4	5 5	V V
V_{OL}	Output Voltage Low	V_{IL} = 3 V I_L = 10 mA		0.2	0.45	V
I_{OS}	Output Short Circuit Current			3	4	mA
I_{CC}	Power Supply Current	All gates "on" I_O = 0 mA V_{IH} = 5 V		16	26	mA
P_C	Power Consumption	V_{IH} = 5 V		80	130	mW

SWITCHING CHARACTERISTICS (V_S = 5 V, T_{amb} = 25 ° C, see Fig. 1)

Symbol	Parameter	Test Condtions	Min.	Typ.	Max.	Unit
t_{PLH}	Propagation delay Time	R_L = 3.9 KΩ		25	85	ns
t_{TLH}	Rise Time	R_L = 3.9 KΩ		120	175	ns
t_{PHL}	Propagation Delay Time	R_L = 390 Ω		25	50	ns
t_{THL}	Fall Time	R_L = 390 Ω		10	20	ns

TEST CIRCUITS

Figure 1 : Switching Response.

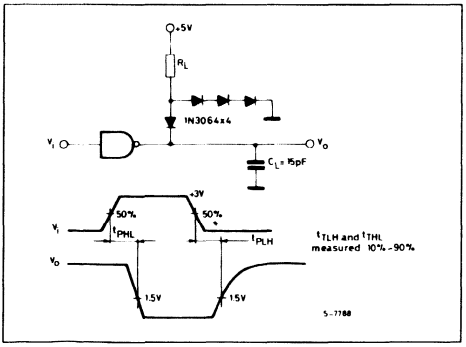
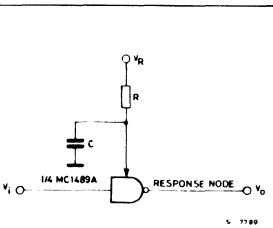


Figure 2 : Response Control Node.



C, capacitor is for noise filtering
R, resistor is for threshold shifting

Figure 3 : Input Current.

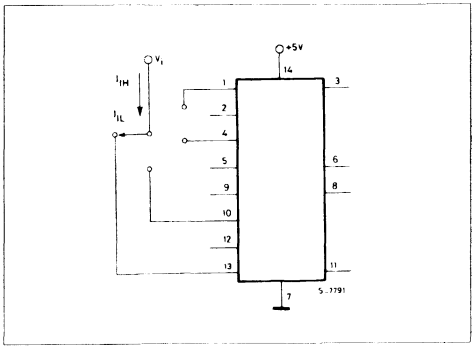


Figure 4 : Output Short-Circuit Current.

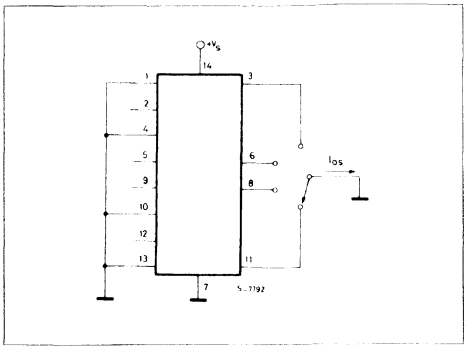


Figure 5 : Output Voltage and Input Threshold Voltage.

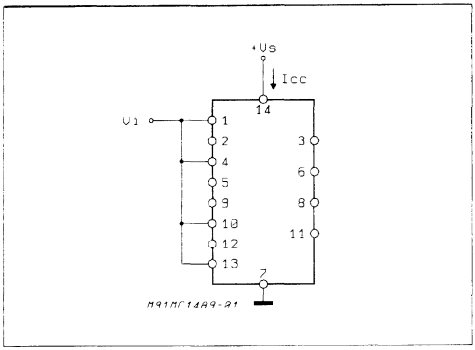
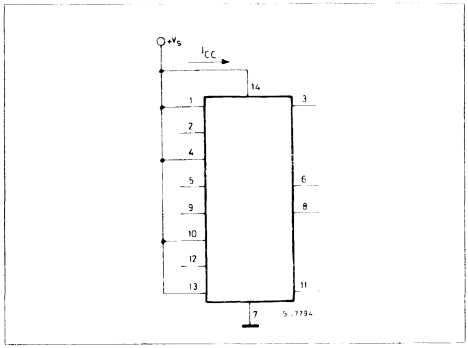


Figure 6 : Power Supply Current.



TYPICAL CHARACTERISTICS (V_S = 5 V, T_{amb} = 25 °C unless otherwise specified)

Figure 7 : Input Current.

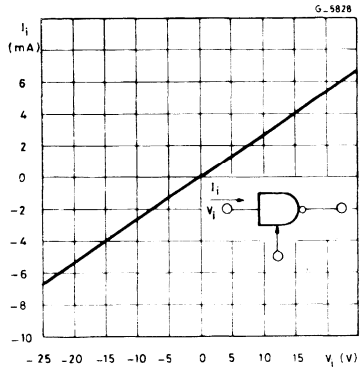


Figure 8 : MC1489 Input Threshold Voltage Adjustament.

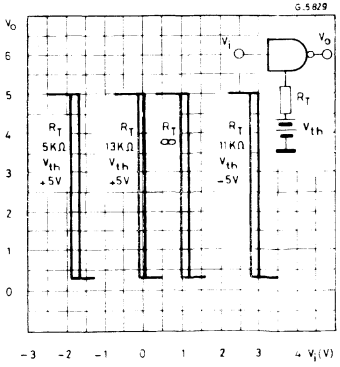


Figure 9 : MC1489A Input Threshold Voltage Adjustment.

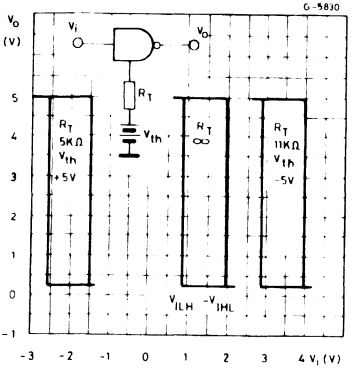


Figure 10 : Input Threshold Voltage vs. Temperature.

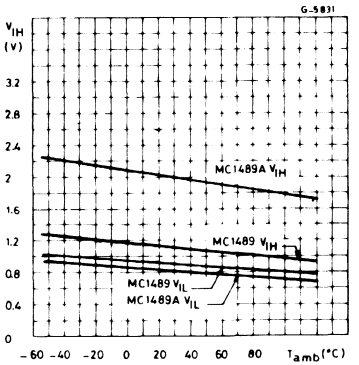
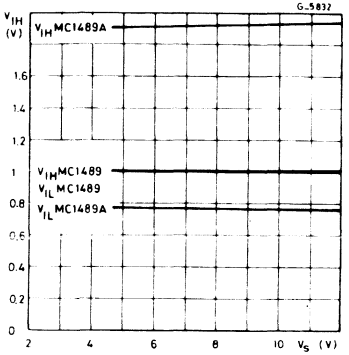


Figure 11 : Input Threshold vs. Power-Supply Voltage.



APPLICATION INFORMATION

GENERAL INFORMATION

The Electronic Industries Association (EIA) has released the RS-232C specification detailing the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS-232C defined levels. The RS-232C requirements as applied to receivers are discussed herein.

The required input impedance is defined as between 3000 Ω and 7000 Ω for input voltages between 3.0 and 25 V in magnitude ; and any voltage on the receiver input in an open circuit condition must be less than 2.0 V in magnitude. The MC1489 circuits meet these requirements with a maximum open circuit voltage of one V_{BE}.

The receiver shall detect a voltage between - 3.0 and - 25 V as a Logic "1" and inputs between + 3.0 and + 2.5 V as a Logic "0". On some interchange leads, an open circuit of power "OFF" condition (300 Ω or more to ground) shall be decoded as an "OFF" condition or Logic "1". For the reason, the input hysteresis thresholds of the MC1489 circuits are all above ground. Thus an open or grounded input will cause the same output as a negative or Logic "1" input.

DEVICE CHARACTERISTICS

The MC1489 interface receivers have internal feedback from the second stage to the input stage providing input hysteresis for noise rejection. The MC1489 input has typical turn-on voltage of 1.25 V and turn-off of 1.0 V for a typical hysteresis of 250 mV. The MC1489A has typical turn-on of 1.95 V and turn-off of 0.8 V for typically 1.15 V of hysteresis.

Each receiver section has an external response control node in addition to the input and output pins, thereby allowing the designer to vary the input threshold voltage levels. A resistor can be connected between this node and and an external power supply. Figure 2, 4 and 5 illustrate the input threshold voltage shift possible through this technique.

This response node can also be used for the filtering of the high-frequency, high-energy noise pulses. Figure 8 and 9 show typical noise-pulse rejection for external capacitors of various sizes.

These two operations on the response node can be combined or used individually for may combinations of interfacing applications. The MC1489 circuits are particularly useful for interfacing between MOS circuits and MDTL/MTTL logic systems. In this application, the input threshold voltages are adjusted. (with the appropiate supply and resistor values) to fall in the center of the MOS voltage logic levels. (See Figure 10).

The response node may also be used as the receiver input as long as the designer realizes that he may not drive this node with a low impedance source to a voltage greater than one diode above ground or less than one diode below ground. This feature is demonstrated in Figure 11 where two receivers are slaved to the same line that must still meet the RS-232C impedance requirement.

Figure 12 : Typical Turn-on Threshold vs. Capacitance from Response Control Pin to GND.

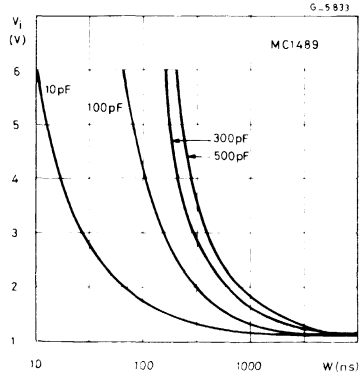


Figure 13 : Typical Turn-on Threshold vs. Capacitance from Response Control Pin to GND.

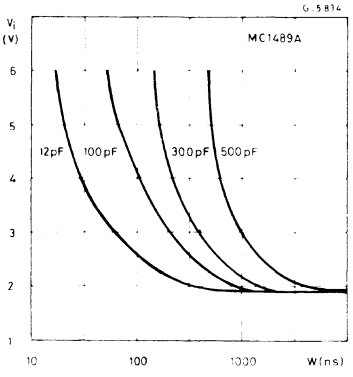
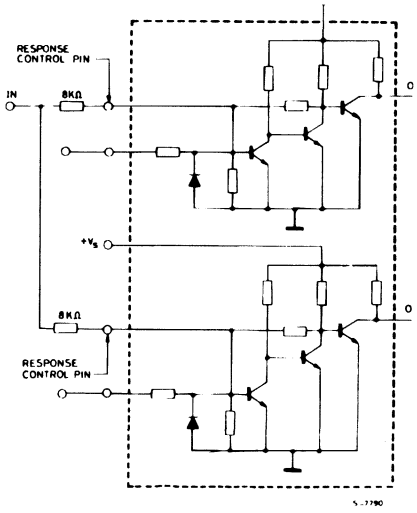


Figure 14: Typical Paralleling of Two MC1489/A Receivers to Meet RS-232C.

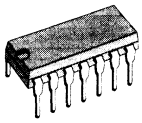


SGS-THOMSON MICROELECTRONICS

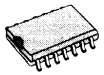
MC3303
MC3403 - MC3503

LOW POWER QUAD BIPOLAR OPERATIONAL AMPLIFIERS

- SHORT-CIRCUIT PROTECTED OUTPUTS
- CLASS AB OUTPUT STAGE FOR MINIMAL CROSSOVER DISTORTION
- SINGLE SUPPLY OPERATION : + 3 V TO + 36V
- DUAL SUPPLIES : ±1.5V TO ±18V
- LOW INPUT BIAS CURRENT : 500nA MAX
- INTERNALLY COMPENSATED
- SIMILAR PERFORMANCE TO POPULAR UA741



N
DIP14
(Plastic Package)
J
CERDIP14
(Cerdip Package)



D
SO14
(Plastic Micropackage)

DESCRIPTION

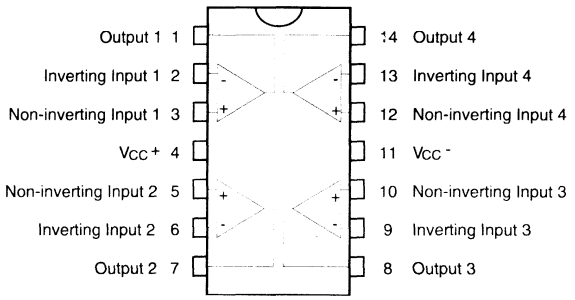
The MC3403 is a low-cost, quad operational amplifier with true differential inputs. The device has electrical characteristics similar to the popular UA741. However the MC3403, has several distinct advantages over standard operational amplifier types in single supply applications. The quad amplifier can operate at supply voltages as low as 3.0 volts or as high as 36 volts with quiescent currents about one third of those associated with the UA741 (on a per amplifier basis). The common-mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications.

ORDER CODES

Part Number	Temperature Range	Package		
		N	J	D
MC3303	–40°C, +105°C	•	•	•
MC3403	0°C, +70°C	•	•	•
MC3503	–55°C, +125°C	•	•	•
Examples : MC3503J, MC3403N				

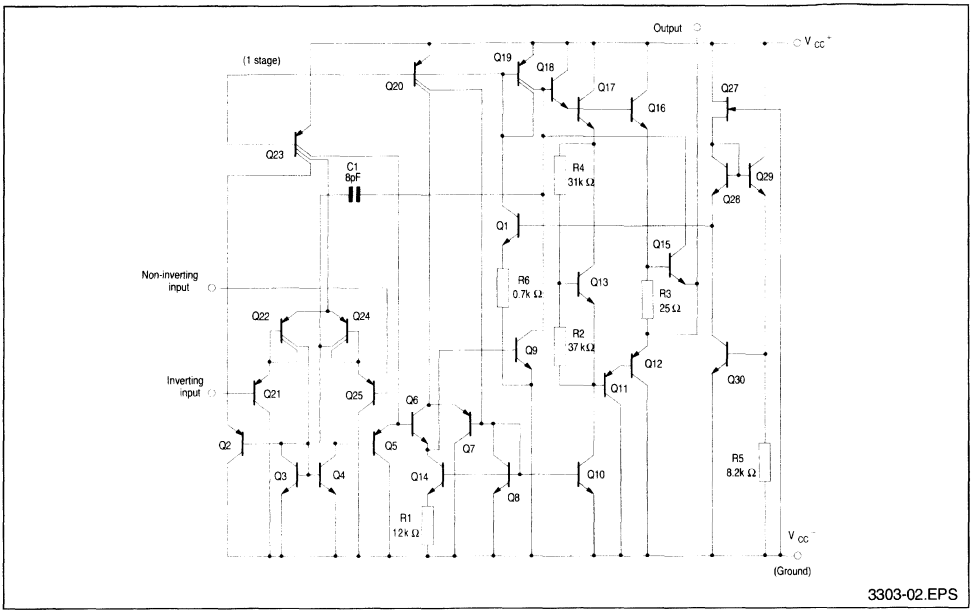
3303-01.TBL

PIN CONNECTIONS (top view)

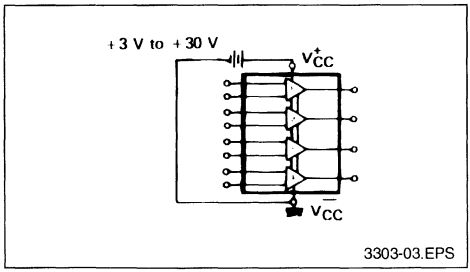


3303-01.EPS

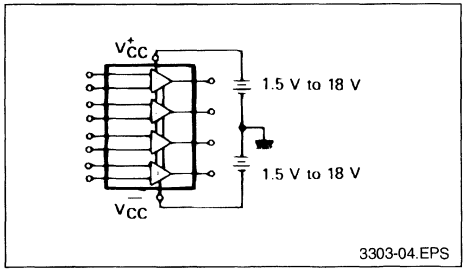
SCHEMATIC DIAGRAM (each amplifier)



SINGLE SUPPLY



DUAL SUPPLIES



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	MC3503	MC3403	MC3303	Unit
V_{CC}	Supply Voltage	±18 or 36	±18 or 36	±18 or 36	V
V_{id}	Differential Input Voltage	±36	±36	±36	V
V_i	Input Voltage (note 1)	±18	±18	±18	V
–	Output Short-circuit Duration (note 2)	Infinite			–
P_{tot}	Power Dissipation	500	500	500	mW
T_{oper}	Operating Free-air Temperature Range	–55 to +125	0 to +70	–40 to +105	°C
T_{stg}	Storage Temperature Range	–65 to +150	–65 to +150	–65 to +150	°C

Notes : 1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Any of the amplifier outputs can be shorted to ground indefinitely ; however more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

ELECTRICAL CHARACTERISTICS

V_{CC} = ±15V, T_{amb} = +25°C, (unless otherwise specified)

Symbol	Parameter		MC3303 - MC3403 MC3503			Unit
			Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage ($R_S \leq 10k\Omega$) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$			1	5 6	mV
I_{IO}	Input Offset Current T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$			2	50 200	nA
I_{ib}	Input Bias Current T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$			40	500 800	nA
A_{vd}	Large Signal Voltage Gain (V_O = ±10V, R_L = 2kΩ) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		50 25	200		V/mV
SVR	Supply Voltage Rejection Ratio ($R_S \leq 10k\Omega$) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		77 77	90		dB
I_{CC}	Supply Current, all Amp, no Load T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	MC3503 MC3503		2.8	7 4 8 5	mA
V_{icm}	Input Common Mode Voltage Range T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		− 15 − 15		+ 13 + 13	V
CMR	Common Mode Rejection Ratio ($R_S \leq 10k\Omega$) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		70 70	90		dB
I_{OS}	Output Short-circuit Current		10	30	45	mA
± V_{opp}	Output Voltage Swing T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	R_L = 10kΩ R_L = 2kΩ R_L = 2kΩ R_L = 10kΩ	12 10 10 12	13.5 13		V
SR	Slew Rate (V_I = ±10V R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)		0.35	0.5		V/µs
t_r, t_f	Rise Time and Fall Time (V_O = ± 20mV, R_L = 2kΩ, C_L = 100pF T_{amb} = 25°C, unity gain)			0.18		µs
K_{OV}	Overshoot (V_I = ± 20mV, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)			10		%
Z_I	Input Impedance		0.3	1		MΩ
Z_O	Output Impedance			75		Ω
B_{om}	Power Bandwidth (R_L = 2kΩ, C_L = 100pF, A_v = 1, T_{amb} = 25°C, V_O = 2V_{pp}, THD ≤ 5%)			9		kHz
B	Unity Gain Bandwidth (V_O = 10mV, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)			1		MHz
GBP	Gain Bandwidth Product (V_O = 10mV, R_L = 2kΩ, C_L = 100pF, f = 100kHz, T_{amb} = 25°C)		0.7	1		MHz
THD	Total Harmonic Distortion (f = 1kHz, A_v = 20dB, R_L = 2kΩ, V_O = 2V_{pp}, C_L = 100pF, T_{amb} = 25°C)			0.02		%
e_n	Equivalent Input Noise Voltage (f = 1kHz, R_s = 100Ω)			43		$\frac{nV}{\sqrt{Hz}}$

3303-03.TBL

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	MC3303 - MC3403 - MC3503			Unit
		Min.	Typ.	Max.	
Øm	Phase Margin		60		Degrees
DV_{IO}	Input Offset Voltage Drift $T_{min.} \leq T_{amb} \leq T_{max.}$		10		µV/°C
DI_{IO}	Input Offset Current Drift $T_{min.} \leq T_{amb} \leq 25°C$		50		pA/°C
V_{O1}/V_{O2}	Channel Separation		120		dB

3303-04.TBL

ELECTRICAL CHARACTERISTICS

$V_{CC}^+ = 5V$, $V_{CC}^- =$ Ground, $T_{amb} = 25°C$ (unless otherwise specified)

Symbol	Parameter	MC3303 - MC3403 - MC3503			Unit
		Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage ($R_S \leq 10k\Omega$) $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$		1	5 6	mV
I_{IO}	Input Offset Current $T_{amb} = 25°C$ $T_{min.} \leq T_{amb} \leq T_{max.}$		2	50 200	nA
I_{ib}	Input Bias Current $T_{amb} = 25°C$ $T_{min.} \leq T_{amb} \leq T_{max.}$		40	500 800	nA
A_{vd}	Large Signal Voltage Gain ($V_O = 1.4$ to $2.4V$, $R_L = 2k\Omega$) $T_{amb} = 25°C$ $T_{min.} \leq T_{amb} \leq T_{max.}$	10 5	200		V/mV
SVR	Supply Voltage Rejection Ratio ($R_S \leq 10k\Omega$) $T_{amb} = 25°C$ $T_{min.} \leq T_{amb} \leq T_{max.}$	77 77	90		dB
I_{CC}	Supply Current (All Amp) MC3503		2.5	7 4	mA
V_{opp}	Output Voltage Range ($R_L = 10k\Omega$) $V_{CC} = +5V$ $+5 \leq V_{CC} \leq +30V$	3.3 V_{CC}^+-2V	3.5 V_{CC}^+-1.7V		V

3303-05.TBL

CIRCUIT DESCRIPTION

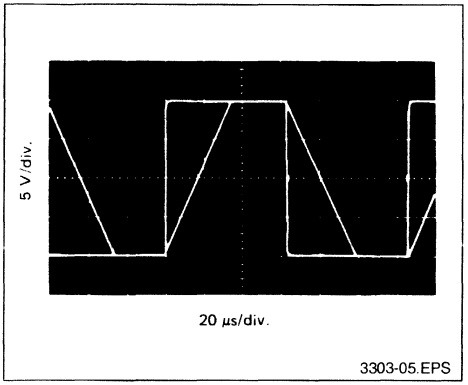
The MC3403 is made using four internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input devices Q24 and Q22 with input buffer transistors Q25 and Q21 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance a smaller compensation capacitor (only 8pF) can be employed, thus saving chip area.

The transconductance reduction is accomplished by splitting the collectors of Q24 and Q22. Another feature of this input stage is that the input common-mode range can include the negative supply of ground, in single supply operation, without saturation either the input devices or the differential to single-ended converter.

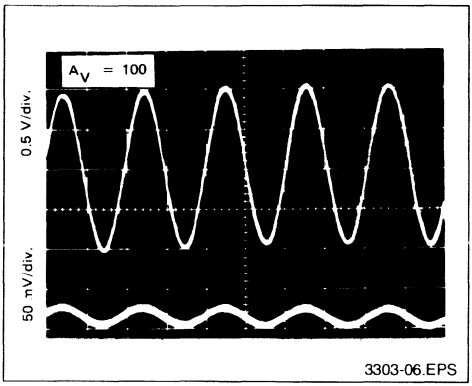
The second stage consists of a standard current source load amplifier stage. The output stage is unique because it allows the output to swing to ground in single supply operation and yet does not exhibit any crossover distortion in split supply operations. This is possible because class AB operation is utilized.

Each amplifier is biased from an internal voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

TYPICAL PERFORMANCE CURVES



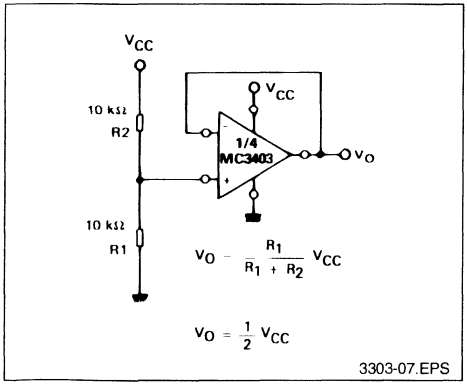
3303-05.EPS



3303-06.EPS

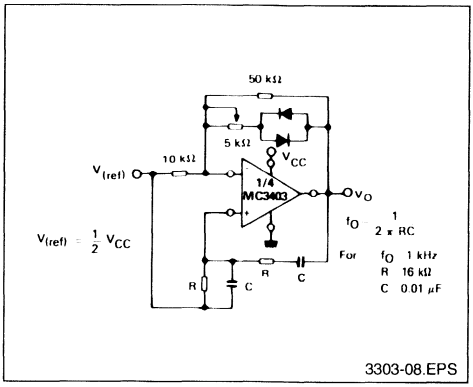
APPLICATION INFORMATION

VOLTAGE REFERENCE



3303-07.EPS

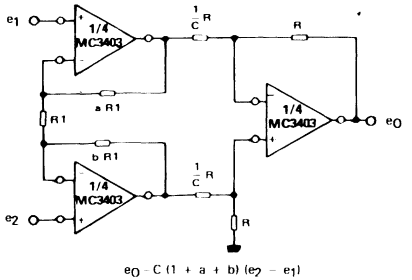
WIEN BRIDGE OSCILLATOR



3303-08.EPS

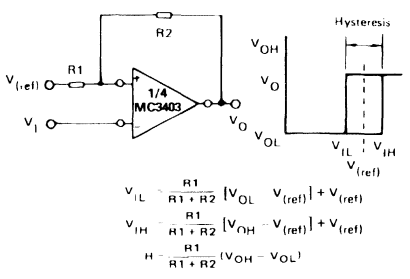
APPLICATION INFORMATION (continued)

HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER



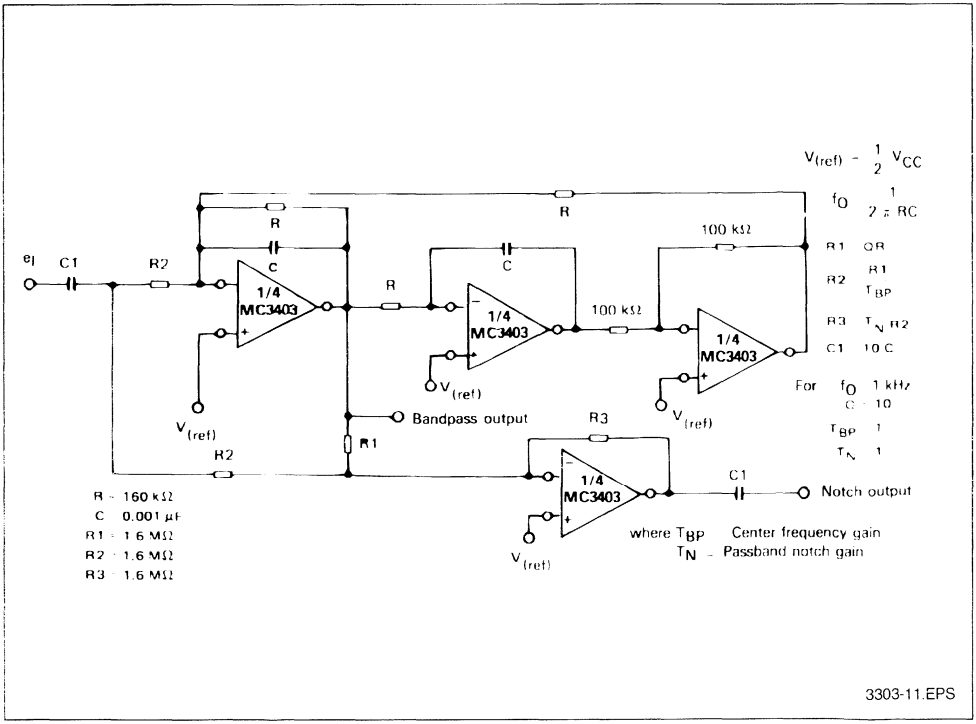
3303-09.EPS

COMPARATOR WITH HYSTERESIS



3303-10.EPS

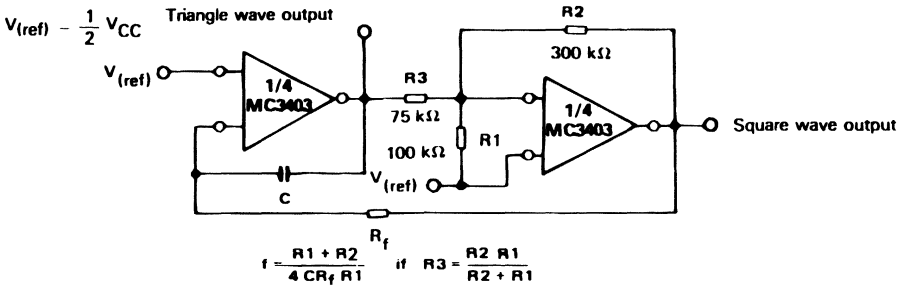
BI-QUAD FILTER



3303-11.EPS

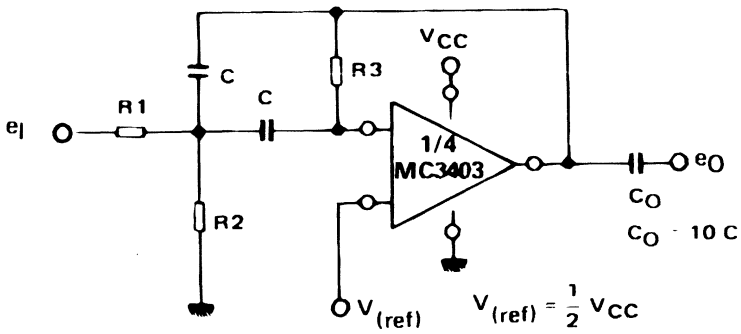
APPLICATION INFORMATION (continued)

FUNCTION GENERATOR



3303-12.EPS

MULTIPLE FEEDBACK BANDPASS FILTER



3303-13.EPS

Given f_o = Center frequency choose values f_o, C then

$$R3 = \frac{Q}{\pi f_o C}$$

A (f_o) = Gain at center frequency

$$R1 = \frac{R3}{2A(f_o)}$$

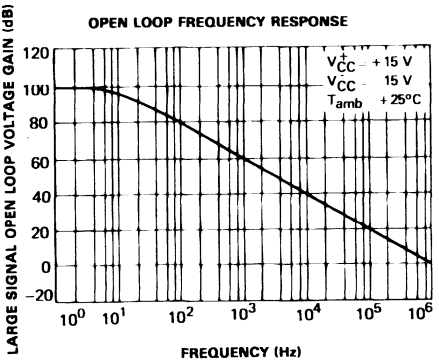
$$R2 = \frac{R1\ R5}{4Q^2\ R1 - R5}$$

For less than 10% error from operational amplifier

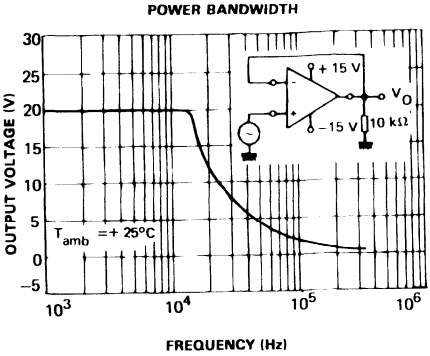
$\frac{Q_o f_o}{BW} < 0.1$ where f_o and BW are expressed in Hz

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters

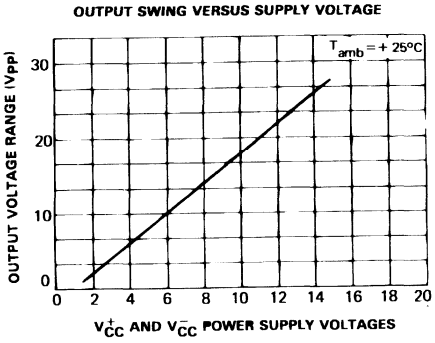
TYPICAL PERFORMANCE CURVES



3303-14.EPS



3303-15.EPS



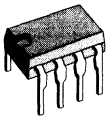
3303-16.EPS

SGS-THOMSON MICROELECTRONICS

MC4558
MC4558I

WIDE BANDWIDTH DUAL BIPOLAR OPERATIONAL AMPLIFIERS

- INTERNALLY COMPENSATED
- SHORT-CIRCUIT PROTECTION
- GAIN AND PHASE MATCH BETWEEN AMPLIFIERS
- LOW POWER CONSUMPTION
- PIN TO PIN COMPATIBLE WITH MC1458/LM358
- GAIN BANDWIDTH PRODUCT (at 100kHz) 5.5MHz



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

J
CERDIP8
(Cerdip Package)

H
TO99
(Metal Can)

DESCRIPTION

The MC4558 is a high performance monolithic dual operational amplifier.

The circuit combines all the outstanding features of the MC1458 and, in addition, possesses three times the unity gain bandwidth of the industry standard.

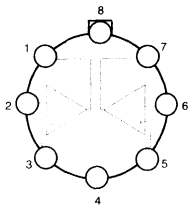
ORDER CODES

Part Number	Temperature Range	Package			
		H	N	J	D
MC4558C	0°C, +70°C	•	•	•	•
MC4558I	-40°C, +105°C	•	•	•	•
Example : MC4558CN					

4558-01.TBL

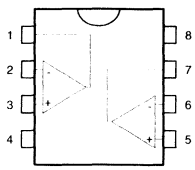
PIN CONNECTIONS (top views)

TO99



4558-01.EPS

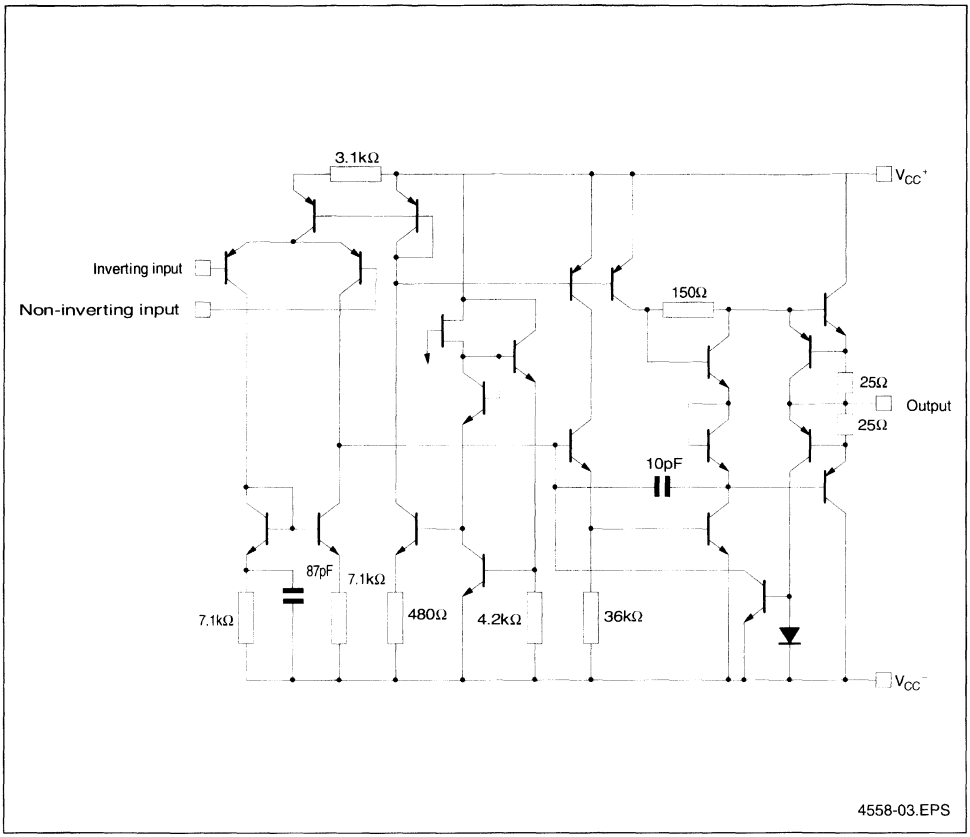
DIP8/CERDIP8
SO8



4558-02.EPS

1 – Output 1
2 – Inverting input 1
3 – Non-inverting input 1
4 – V_{CC}^-
5 – Non-inverting input 2
6 – Inverting input 2
7 – Output 2
8 – V_{CC}^+

SCHEMATIC DIAGRAM (1/2 MC4558)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	MC4558I	MC4558C	Unit
V_{CC}	Supply Voltage	±22	±22	V
V_i	Input Voltage	±15	±15	V
V_{id}	Differential Input Voltage	±30	±30	V
P_{tot}	Power Dissipation	680	680	mW
	Output Short-circuit Duration	Infinite		
T_{oper}	Operating Free-air Temperature Range	–40 to +105	0 to +70	°C
T_{stg}	Storage Temperature Range	–65 to +150	–65 to +150	°C

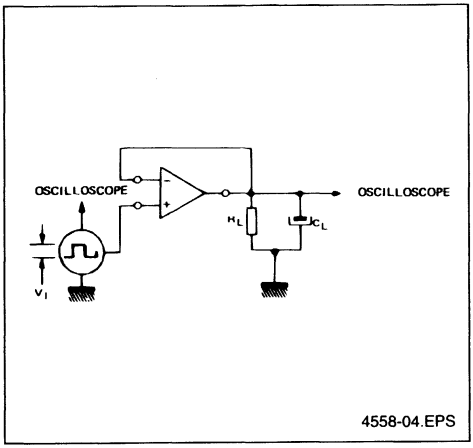
ELECTRICAL CHARACTERISTICS

V_{CC} = ±15V, T_{amb} = 25°C (unless otherwise specified)

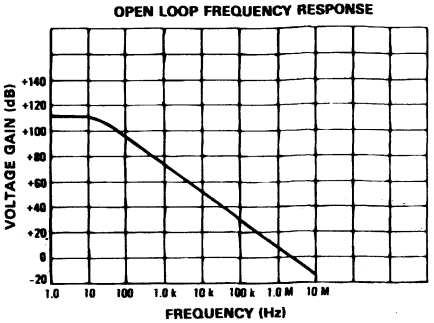
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage ($R_S \leq 10\ k\Omega$) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		1	5 6	mV
I_{io}	Input Offset Current T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		20	100 200	nA
I_{ib}	Input Bias Current T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		50	400 500	nA
A_{vd}	Large Signal Voltage Gain (V_O = ±10V, R_L = 2kΩ) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	50 25	200		V/mV
SVR	Supply Voltage Rejection Ratio ($R_S \leq 10k\Omega$) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	77 77	90		dB
I_{CC}	Supply Current, all Amp, no Load T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		2.3	4.5 6	mA
V_{icm}	Input Common Mode Voltage Range T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	±12 ±12			V
CMR	Common-mode Rejection Ratio ($R_S \leq 10k\Omega$) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	70 70	90		dB
I_{os}	Output Short-circuit Current	10	20	40	mA
V_o	Output Voltage Swing T_{amb} = 25°C, R_L = 10kΩ R_L = 2kΩ $T_{min} \leq T_{amb} \leq T_{max}$, R_L = 10kΩ R_L = 2kΩ	±12 ±10 ±12 ±10	±14 ±13		V
SR	Slew Rate (V_I = ±10V, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)	1.5	2.2		V/µs
t_r	Rise Time (V_I = ±20mV, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)		0.3		µs
K_{OV}	Overshoot (V_I = ±20 mV, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)		15		%
R_i	Input Resistance	0.3	2		MΩ
C_i	Input Capacitance		1.4		pF
R_O	Output Resistance		75		Ω
f_T	Transition Frequency		2.8		MHz
GBP	Gain Bandwidth Product (V_I = 10mV, R_L = 2kΩ, C_L = 100pF, f = 100kHz, T_{amb} = 25°C)		5.5		MHz
THD	Total Harmonic Distorsion (f = 1kHz, A_v = 20dB, R_L = 2kΩ, V_o = $2V_{pp}$, C_L = 100pF, T_{amb} = 25°C)		0.008		%
e_n	Equivalent Input Noise Voltage (f = 1kHz, R_s = 100Ω)		12		$\frac{nV}{\sqrt{Hz}}$
V_{O1}/V_{O2}	Channel Separation		120		dB

4558-03.TBL

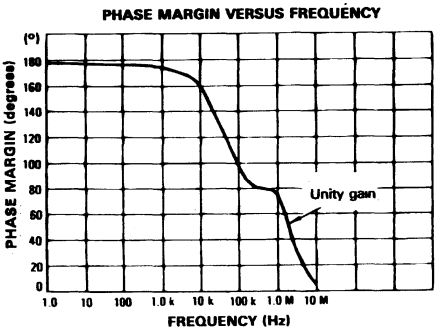
TRANSIENT RESPONSE TEST CIRCUIT



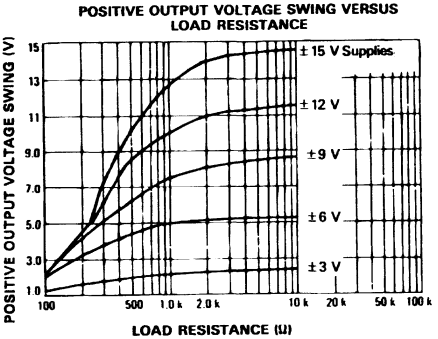
4558-04.EPS



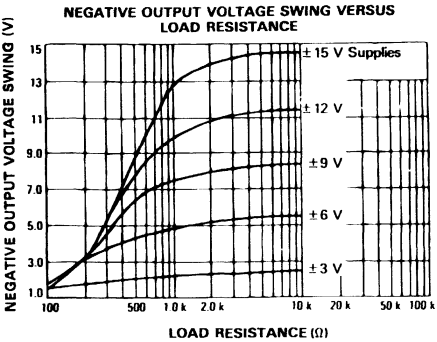
4558-05.EPS



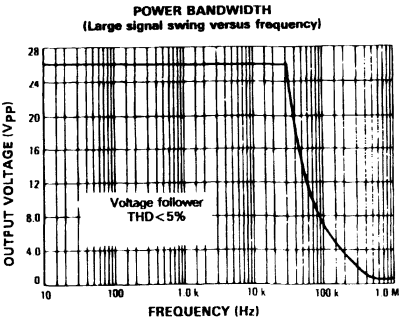
4558-06.EPS



4558-07.EPS



4558-08.EPS



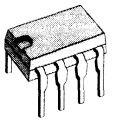
4558-09.EPS

SGS-THOMSON MICROELECTRONICS

MC33001/A/B
MC34001/A/B
MC35001/A/B

GENERAL PURPOSE SINGLE JFET OPERATIONAL AMPLIFIERS

- LOW POWER CONSUMPTION
- WIDE COMMON-MODE (UP TO V_{CC}^+) AND DIFFERENTIAL VOLTAGE RANGE
- LOW INPUT BIAS AND OFFSET CURRENT
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J-FET INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : 16V/µs (typ)



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

H
TO99
(Metal Can)

DESCRIPTION

These circuits are high speed J-FET input single operational amplifiers incorporating well matched, high voltage J-FET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low input bias and offset current, and low offset voltage temperature coefficient.

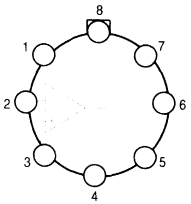
ORDER CODES

Part Number	Temperature	Package		
		H	N	D
MC34001/A/B	0°C, +70°C	•	•	•
MC33001/A/B	-40°C, +105°C	•	•	•
MC35001/A/B	-55°C, +125°C	•	•	•

33001-01.TBL

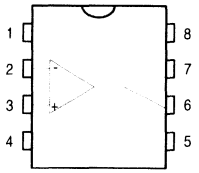
PIN CONNECTIONS (top views)

TO99



33001-01.EPS

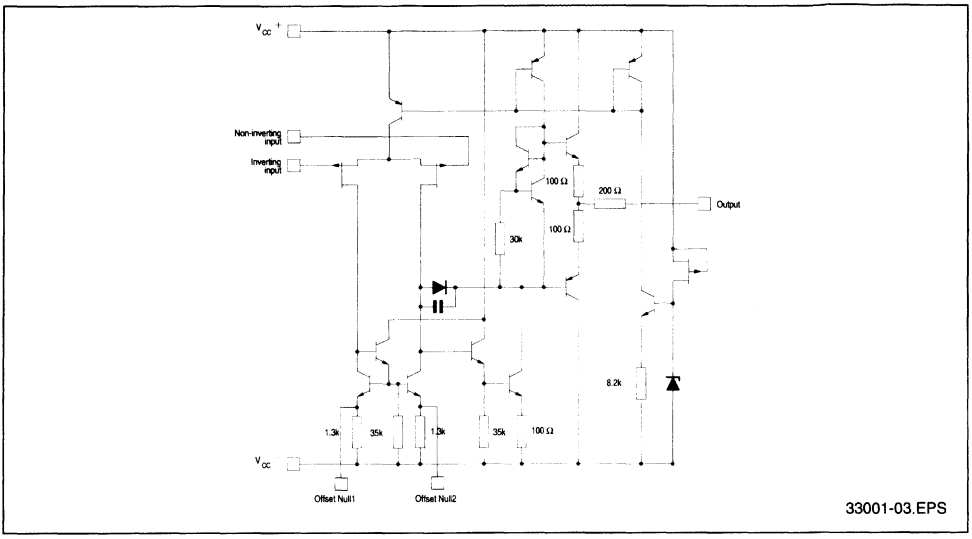
DIP8/SO8



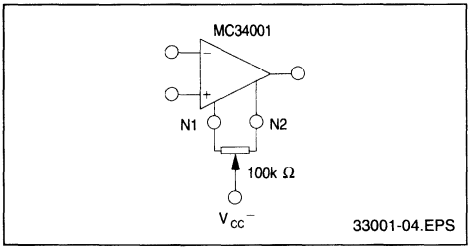
33001-02.EPS

1 - Input Offset Null 1
2 - Inverting input
3 - Non-inverting input
4 - V_{CC}^-
5 - Input Offset Null 2
6 - Output
7 - V_{CC}^+
8 - N.C.

SCHEMATIC DIAGRAM



INPUT OFFSET VOLTAGE NULL CIRCUITS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage - (note 1)		±18	V
V_i	Input Voltage - (note 3)		±15	V
V_{id}	Differential Input Voltage - (note 2)		±30	V
P_{tot}	Power Dissipation		680	mW
	Output Short-circuit Duration (note 4)		Infinite	
T_{oper}	Operating Free Air Temperature Range	MC34001, A, B MC33001, A, B MC35001, A, B	0 to 70 –40 to 105 –55 to 125	°C
T_{stg}	Storage Temperature Range		–65 to 150	°C

Notes :
1. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.
2. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and /or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

ELECTRICAL CHARACTERISTICS

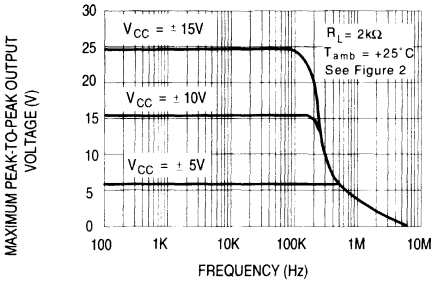
V_{CC} = ±15V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	MC35001A,B MC33001A,B MC34001A,B			MC35001 MC33001 MC34001			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage ($R_S \leq 10k\Omega$)							mV
	T_{amb} = 25°C					3	10	
	MC35001B, MC34001B, MC33001B		3	5				
	MC35001A, MC34001A, MC33001A		0.4	2				
	$T_{min} \leq T_{amb} \leq T_{max}$						13	
	MC35001B, MC34001B, MC33001B			7				
	MC35001A, MC34001A, MC33001A			4				
DV_{io}	Input Offset Voltage Drift		10			10		µV/°C
I_{io}	Input Offset Current *							
	T_{amb} = 25°C		5	100		5	100	pA
	$T_{min} \leq T_{amb} \leq T_{max}$			4			4	nA
I_{ib}	Input Bias Current *							
	T_{amb} = 25°C		20	200		20	200	pA
	$T_{min} \leq T_{amb} \leq T_{max}$			20			20	nA
A_{vd}	Large Signal Voltage Gain (R_L = 2kΩ, V_O = ±10V)							V/mV
	T_{amb} = 25°C	50	200		25	200		
	$T_{min} \leq T_{amb} \leq T_{max}$	25			15			
SVR	Supply Voltage Rejection Ratio ($R_S \leq 10k\Omega$)							dB
	T_{amb} = 25°C	80	86		70	86		
	$T_{min} \leq T_{amb} \leq T_{max}$	80			70			
I_{CC}	Supply Current, no Load							mA
	T_{amb} = 25°C		1.4	2.5		1.4	2.5	
	$T_{min} \leq T_{amb} \leq T_{max}$			2.8			2.8	
V_{icm}	Input Common Mode Voltage Range	±11	+15 -12		±11	+15 -12		V
CMR	Common Mode Rejection Ratio ($R_S \leq 10k\Omega$)							dB
	T_{amb} = 25°C	80	86		70	86		
	$T_{min} \leq T_{amb} \leq T_{max}$	80			70			
Ios	Output Short-circuit Current							mA
	T_{amb} = 25°C	10	40	60	10	40	60	
	$T_{min} \leq T_{amb} \leq T_{max}$	10		60	10		60	
$\pm V_{OPP}$	Output Voltage Swing							V
	T_{amb} = 25°C R_L = 2kΩ	10	12		10	12		
	R_L = 10kΩ	12	13.5		12	13.5		
	$T_{min} \leq T_{amb} \leq T_{max}$ R_L = 2kΩ	10			10			
	R_L = 10kΩ	12			12			
SR	Slew Rate (V_{in} = 10V, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)	12	16		12	16		V/µs
t_r	Rise Time (V_{in} = 20mV, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)		0.1			0.1		µs
Kov	Overshoot (V_{in} = 20mV, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)		10			10		%
GBP	Gain Bandwidth Product (f = 100kHz, T_{amb} = 25°C, V_{in} = 10mV, R_L = 2kΩ, C_L = 100pF)	2.5	4		2.5	4		MHz
R_i	Input Resistance		10^{12}			10^{12}		Ω
THD	Total Harmonic Distortion (f = 1kHz, A_V = 20dB, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, V_O = $2V_{PP}$)		0.01			0.01		%
e_n	Equivalent Input Noise Voltage (f = 1kHz, R_s = 100Ω)		15			15		nV/√Hz
Øm	Phase Margin		45			45		Degrees

* The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature.

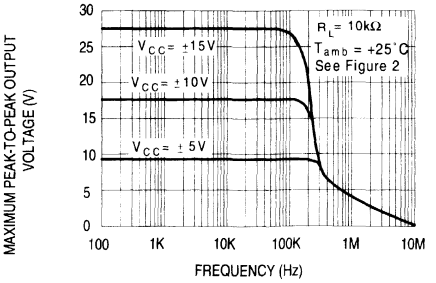
33001-03.TBL

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



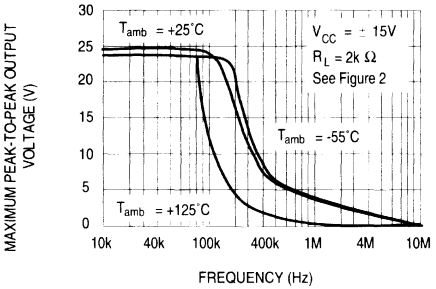
33001-05.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



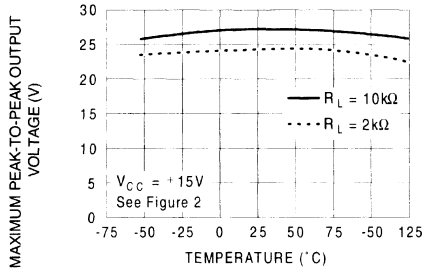
33001-06.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



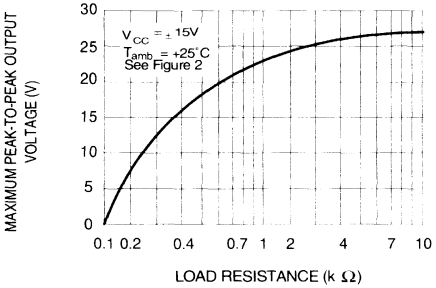
33001-07.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREE AIR TEMP.



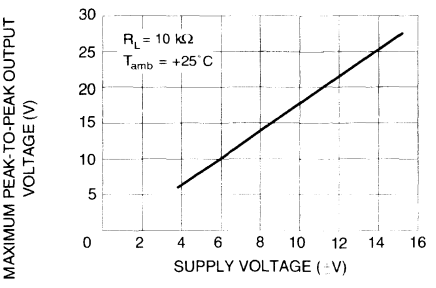
33001-08.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS LOAD RESISTANCE



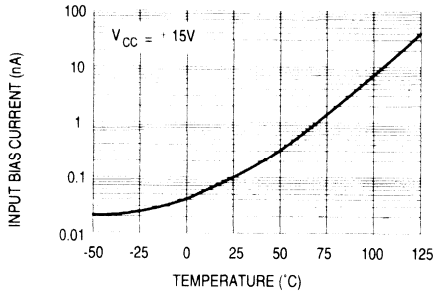
33001-09.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS SUPPLY VOLTAGE



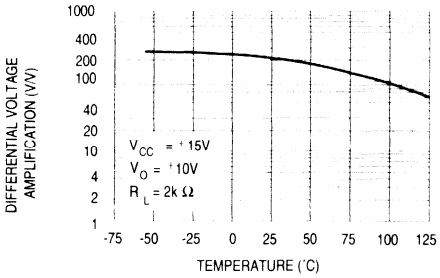
33001-10.EPS

INPUT BIAS CURRENT VERSUS FREE AIR TEMPERATURE



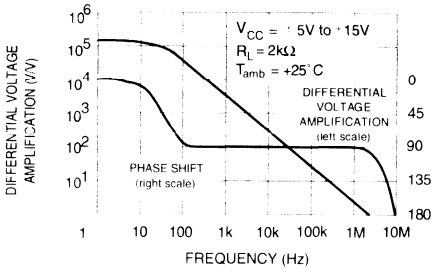
33001-11.EPS

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION VERSUS FREE AIR TEMPERATURE



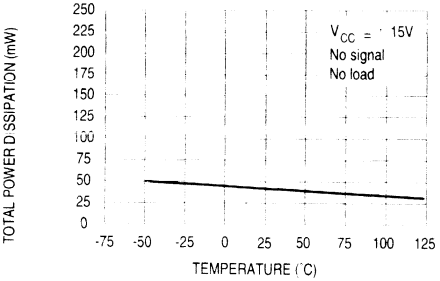
33001-12.EPS

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT VERSUS FREQUENCY



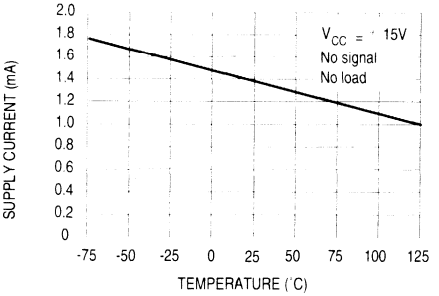
33001-13.EPS

TOTAL POWER DISSIPATION VERSUS FREE AIR TEMPERATURE



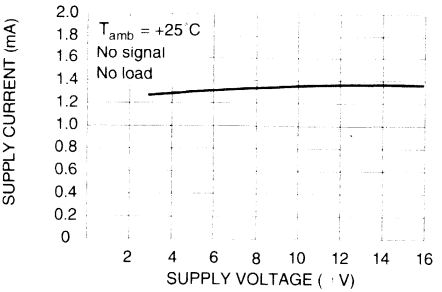
33001-14.EPS

SUPPLY CURRENT PER AMPLIFIER VERSUS FREE AIR TEMPERATURE



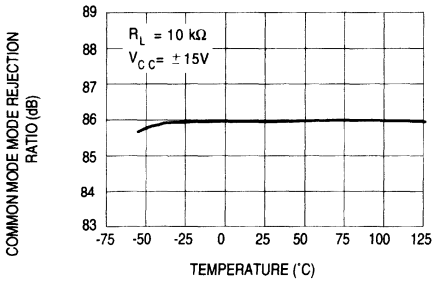
33001-15.EPS

SUPPLY CURRENT PER AMPLIFIER VERSUS SUPPLY VOLTAGE



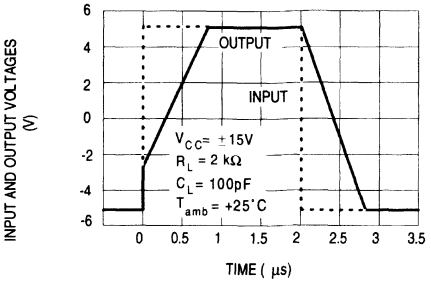
33001-16.EPS

COMMON MODE REJECTION RATIO VERSUS FREE AIR TEMPERATURE



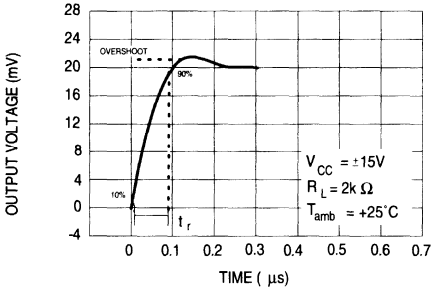
33001-17.EPS

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



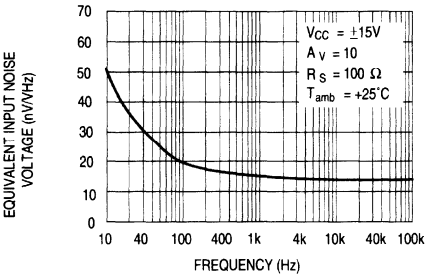
33001-18.EPS

OUTPUT VOLTAGE VERSUS ELAPSED TIME



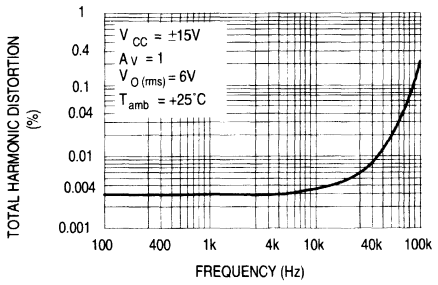
33001-19.EPS

EQUIVALENT INPUT NOISE VOLTAGE VERSUS FREQUENCY



33001-20.EPS

TOTAL HARMONIC DISTORTION VERSUS FREQUENCY



33001-21.EPS

PARAMETER MEASUREMENT INFORMATION

Figure 1 : Voltage Follower

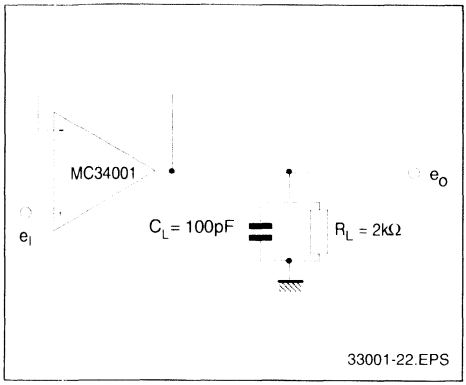
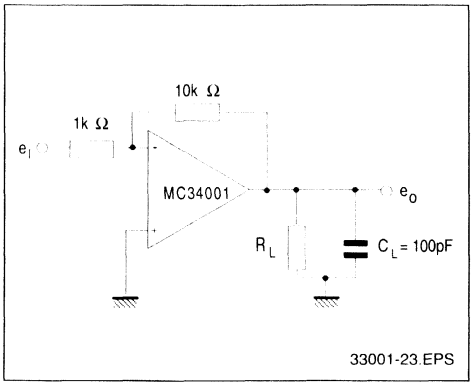
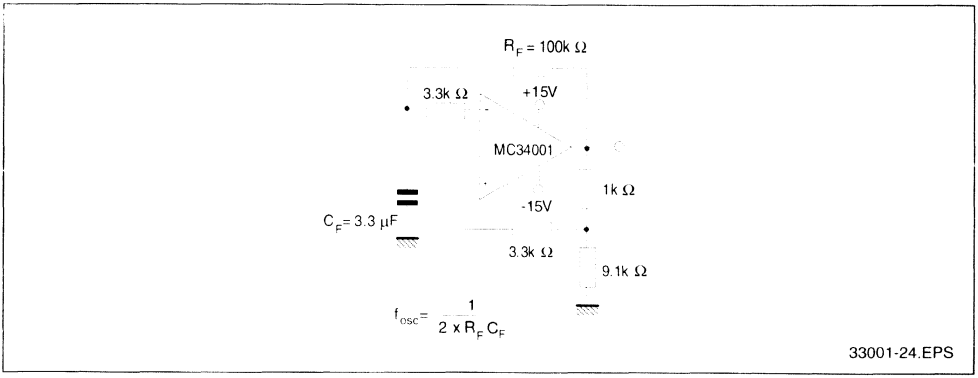


Figure 2 : Gain-of-10 Inverting Amplifier

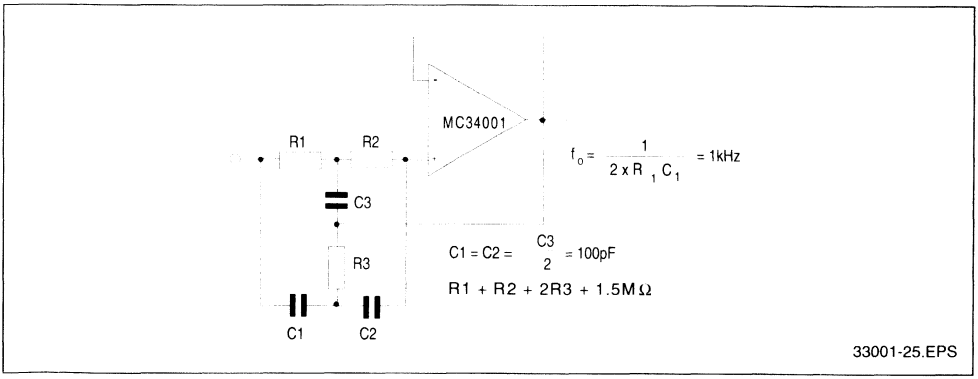


TYPICAL APPLICATIONS

(0.5Hz) SQUARE WAVE OSCILLATOR



HIGH Q NOTCH FILTER

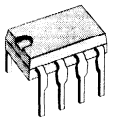


SGS-THOMSON MICROELECTRONICS

MC33002/A/B
MC34002/A/B
MC35002/A/B

GENERAL PURPOSE DUAL JFET OPERATIONAL AMPLIFIERS

- LOW POWER CONSUMPTION
- WIDE COMMON-MODE (UP TO V_{CC}^+) AND DIFFERENTIAL VOLTAGE RANGE
- LOW INPUT BIAS AND OFFSET CURRENT
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J-FET INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : 16V/µs (typ)



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

H
TO99
(Metal Can)

DESCRIPTION

These circuits are high speed J-FET input dual operational amplifiers incorporating well matched, high voltage J-FET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low input bias and offset current, and low offset voltage temperature coefficient.

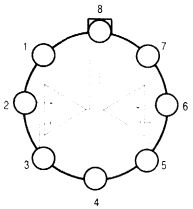
ORDER CODES

Part Number	Temperature	Package		
		H	N	D
MC34002/A/B	0°C, +70°C	•	•	•
MC33002/A/B	-40°C, +105°C	•	•	•
MC35002/A/B	-55°C, +125°C	•	•	•

33002-01.TBL

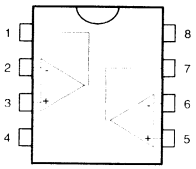
PIN CONNECTIONS (top views)

TO99



33002-01.EPS

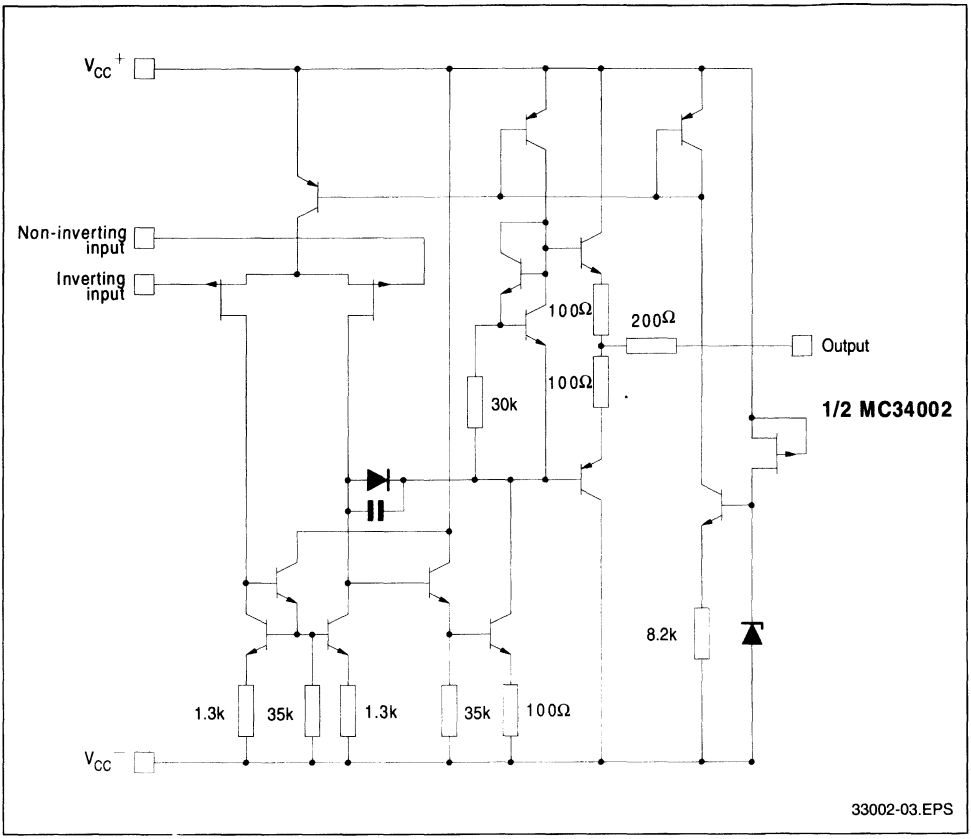
DIP8/SO8



33002-02.EPS

1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^-
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - V_{CC}^+

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage - (note 1)		±18	V
V_I	Input Voltage - (note 3)		±15	V
V_{id}	Differential Input Voltage - (note 2)		±30	V
P_{tot}	Power Dissipation		680	mW
	Output Short-circuit Duration (note 4)		Infinite	
T_{oper}	Operating Free Air Temperature Range	MC34002, A, B MC33002, A, B MC35002, A, B	0 to 70 –40 to 105 –55 to 125	°C
T_{stg}	Storage Temperature Range		–65 to 150	°C

Notes :
1. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.
2. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and /or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

ELECTRICAL CHARACTERISTICS

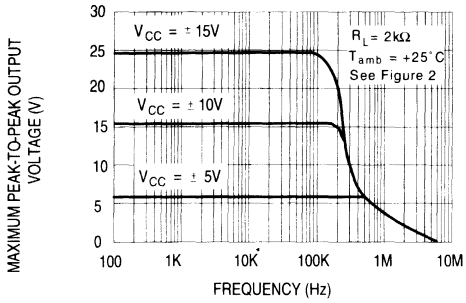
V_{CC} = ±15V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	MC35002A,B MC33002A,B MC34002A,B			MC35002 MC33002 MC34002			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage (R_S ≤10kΩ)							mV
	T_{amb} = 25°C					3	10	
	MC35002B, MC34002B, MC33002B		3	5				
	MC35002A, MC34002A, MC33002A		1	2				
	$T_{min.} \le T_{amb} \le T_{max.}$						13	
	MC35002B, MC34002B, MC33002B			7				
	MC35002A, MC34002A, MC33002A			4				
DV_{io}	Input Offset Voltage Drift		10			10		µV/°C
I_{io}	Input Offset Current *							
	T_{amb} = 25°C		5	50		5	100	pA
	$T_{min.} \le T_{amb} \le T_{max.}$			4			4	nA
I_{ib}	Input Bias Current *							
	T_{amb} = 25°C		20	200		20	200	pA
	$T_{min.} \le T_{amb} \le T_{max.}$			20			20	nA
A_{vd}	Large Signal Voltage Gain (R_L = 2kΩ, V_O = ±10V)							V/mV
	T_{amb} = 25°C	50	200		25	200		
	$T_{min.} \le T_{amb} \le T_{max.}$	25			15			
SVR	Supply Voltage Rejection Ratio (R_S ≤ 10kΩ)							dB
	T_{amb} = 25°C	80	86		70	86		
	$T_{min.} \le T_{amb} \le T_{max.}$	80			70			
I_{CC}	Supply Current, per Amp, no Load							mA
	T_{amb} = 25°C		1.4	2.5		1.4	2.5	
	$T_{min.} \le T_{amb} \le T_{max.}$			2.8			2.8	
V_{icm}	Input Common Mode Voltage Range	±11	+15 -12		±11	+15 -12		V
CMR	Common Mode Rejection Ratio (R_S ≤ 10kΩ)							dB
	T_{amb} = 25°C	80	86		70	86		
	$T_{min.} \le T_{amb} \le T_{max.}$	80			70			
Ios	Output Short-circuit Current							mA
	T_{amb} = 25°C	10	40	60	10	40	60	
	$T_{min.} \le T_{amb} \le T_{max.}$	10		60	10		60	
$\pm V_{OPP}$	Output Voltage Swing							V
	T_{amb} = 25°C R_L = 2kΩ	10	12		10	12		
	R_L = 10kΩ	12	13.5		12	13.5		
	$T_{min.} \le T_{amb} \le T_{max.}$ R_L = 2kΩ	10			10			
	R_L = 10kΩ	12			12			
SR	Slew Rate (V_{in} = 10V, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)	12	16		12	16		V/µs
t_r	Rise Time (V_{in} = 20mV, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)		0.1			0.1		µs
K_{OV}	Overshoot (V_{in} = 20mV, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)		10			10		%
GBP	Gain Bandwidth Product (f = 100kHz, T_{amb} = 25°C, V_{in} = 10mV, R_L = 2kΩ, C_L = 100pF)	2.5	4		2.5	4		MHz
R_i	Input Resistance		10^{12}			10^{12}		Ω
THD	Total Harmonic Distortion (f = 1kHz, A_V = 20dB, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, V_O = $2V_{PP}$)		0.01			0.01		%
e_n	Equivalent Input Noise Voltage (f = 1kHz, R_S = 100Ω)		15			15		$\frac{nV}{\sqrt{Hz}}$
Øm	Phase Margin		45			45		Degrees
V_{O1}/V_{O2}	Channel Separation (A_{vd} = 100)		120			120		dB

* The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature.

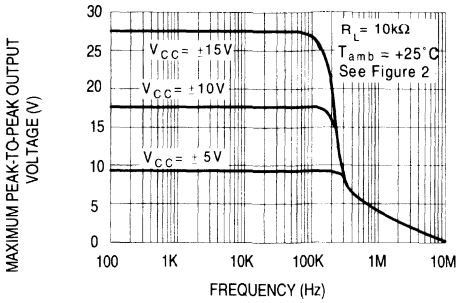
33002-03.TBL

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



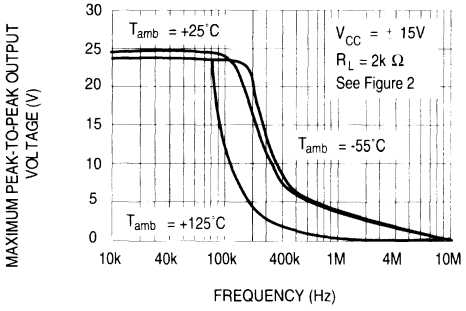
33002-04.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



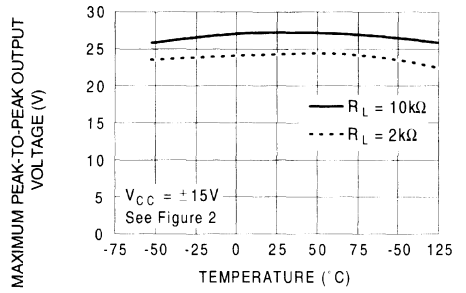
33002-05.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



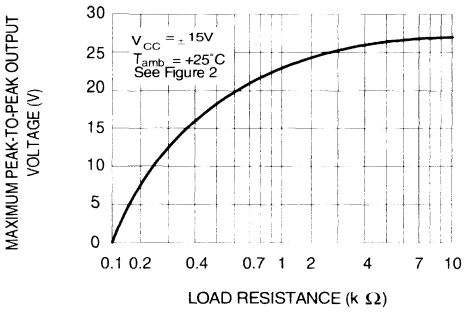
33002-06.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREE AIR TEMP.



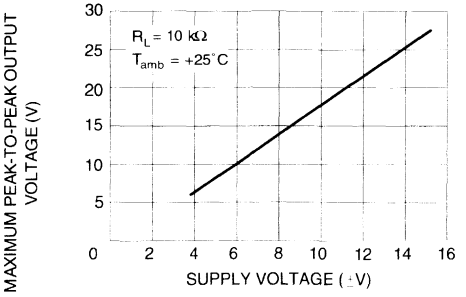
33002-07.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS LOAD RESISTANCE



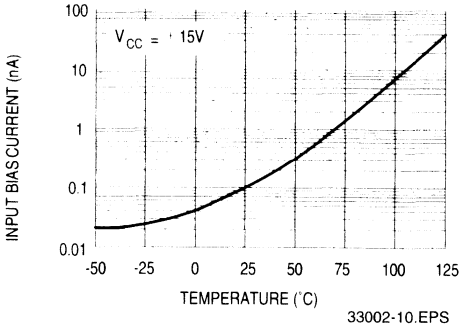
33002-08.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS SUPPLY VOLTAGE



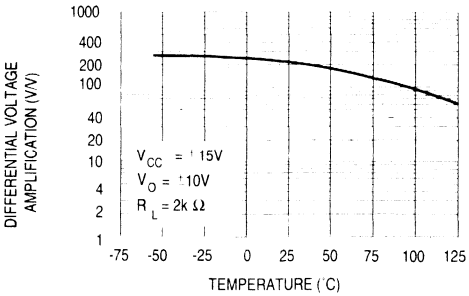
33002-09.EPS

INPUT BIAS CURRENT VERSUS FREE AIR TEMPERATURE



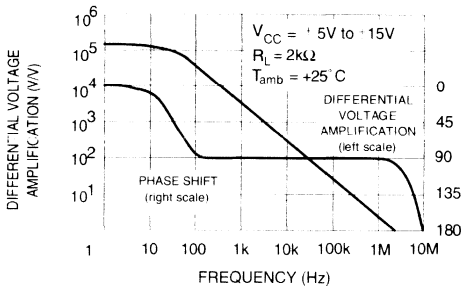
33002-10.EPS

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION VERSUS FREE AIR TEMPERATURE



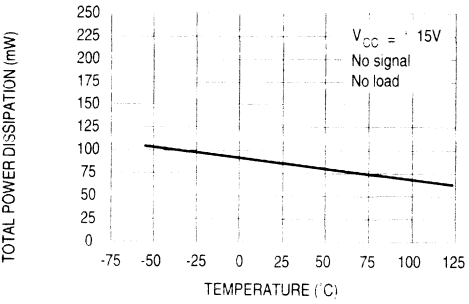
33002-11.EPS

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT VERSUS FREQUENCY



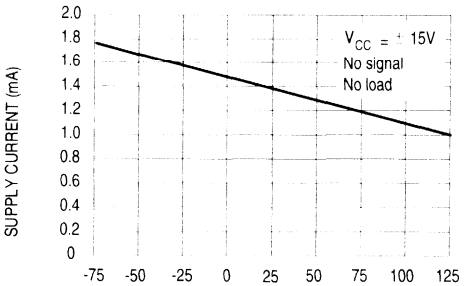
33002-12 EPS

TOTAL POWER DISSIPATION VERSUS FREE AIR TEMPERATURE



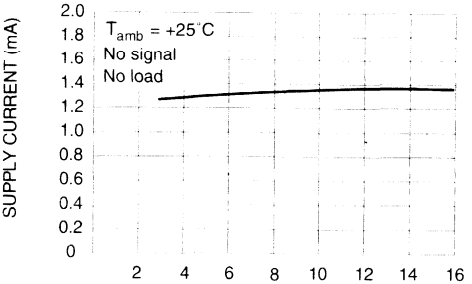
33002-13 EPS

SUPPLY CURRENT PER AMPLIFIER VERSUS FREE AIR TEMPERATURE



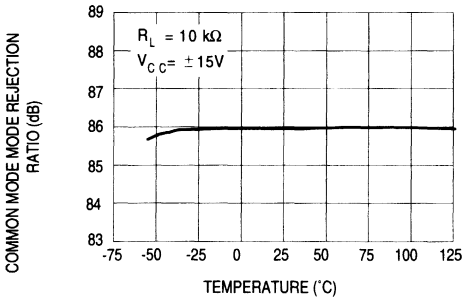
33002-14.EPS

SUPPLY CURRENT PER AMPLIFIER VERSUS SUPPLY VOLTAGE



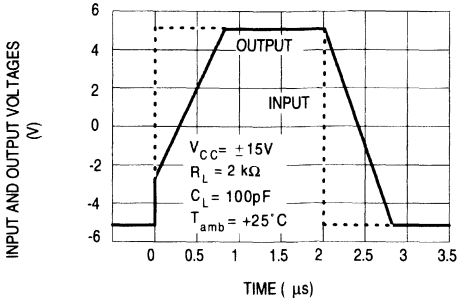
33002-15.EPS

COMMON MODE REJECTION RATIO VERSUS FREE AIR TEMPERATURE



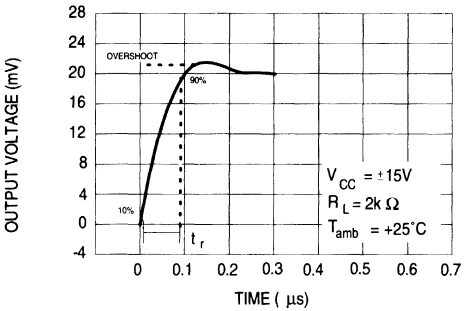
33002-16.EPS

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



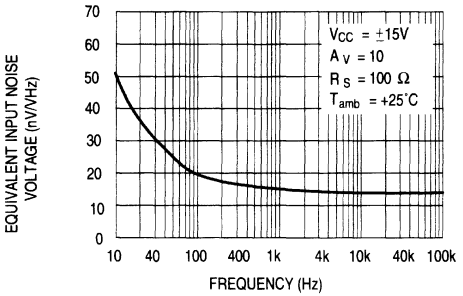
33002-17.EPS

OUTPUT VOLTAGE VERSUS ELAPSED TIME



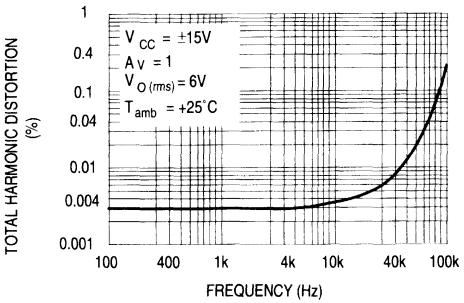
33002-18.EPS

EQUIVALENT INPUT NOISE VOLTAGE VERSUS FREQUENCY



33002-19.EPS

TOTAL HARMONIC DISTORTION VERSUS FREQUENCY



33002-20.EPS

PARAMETER MEASUREMENT INFORMATION

Figure 1 : Voltage Follower

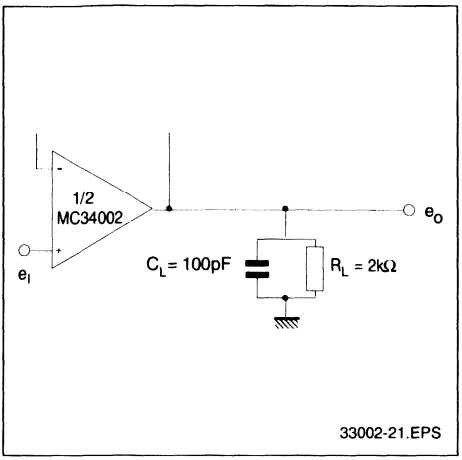
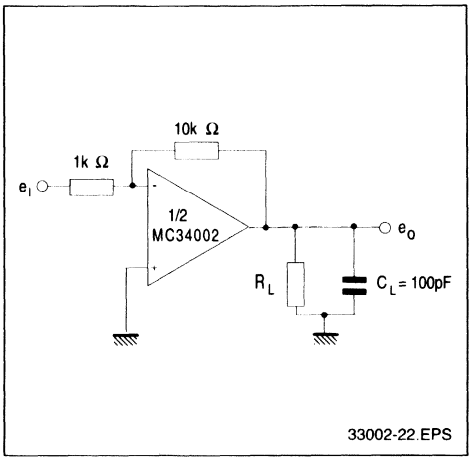
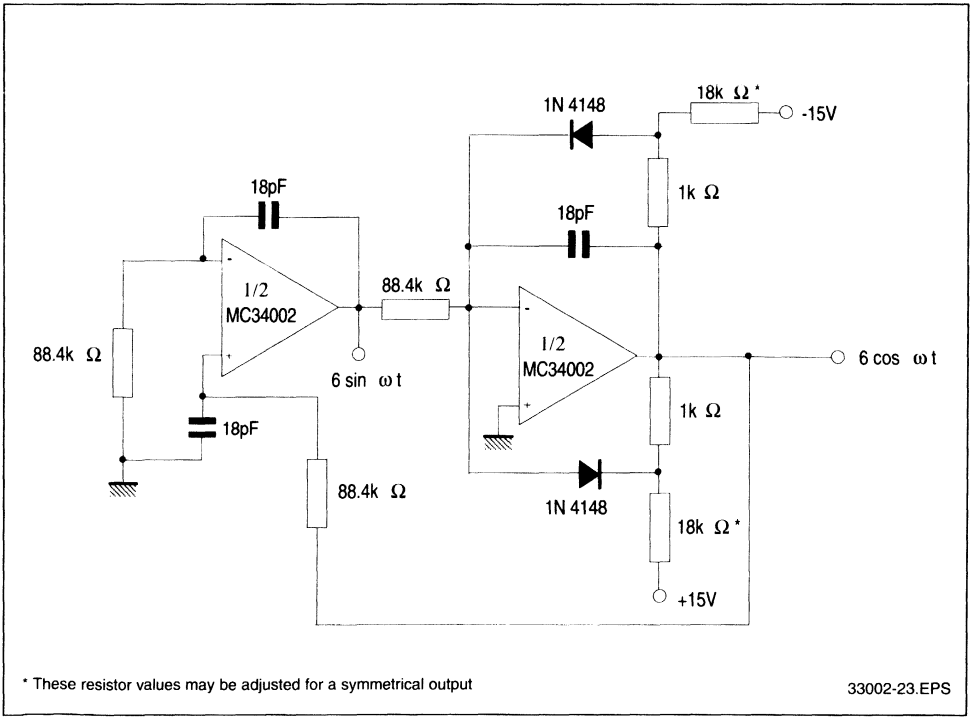


Figure 2 : Gain-of-10 Inverting Amplifier



TYPICAL APPLICATION

100KHz QUADRUPLE OSCILLATOR



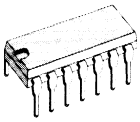
* These resistor values may be adjusted for a symmetrical output

SGS-THOMSON MICROELECTRONICS

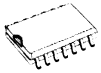
MC33004/A/B
MC34004/A/B
MC35004/A/B

GENERAL PURPOSE QUAD J-FET OPERATIONAL AMPLIFIERS

- LOW POWER CONSUMPTION
- WIDE COMMON-MODE (UP TO V_{CC}^+) AND DIFFERENTIAL VOLTAGE RANGE
- LOW INPUT BIAS AND OFFSET CURRENT
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J-FET INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : 16V/µs (typ)



N
DIP14
(Plastic Package)



D
SO14
(Plastic Micropackage)

DESCRIPTION

These circuits are high speed J-FET input quad operational amplifiers incorporating well matched, high voltage J-FET and bipolar transistors in a monolithic integrated circuit.

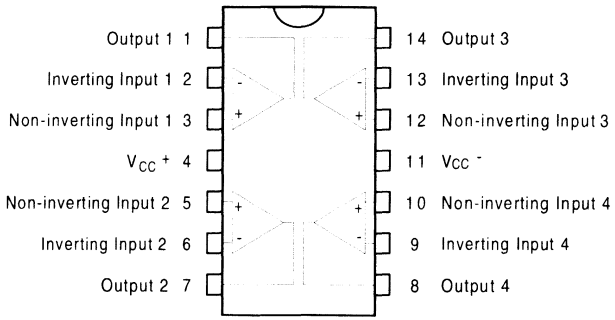
The devices feature high slew rates, low input bias and offset current, and low offset voltage temperature coefficient.

ORDER CODES

Part Number	Temperature	Package	
		N	D
MC34004/A/B	0°C, +70°C	•	•
MC33004/A/B	−40°C, +105°C	•	•
MC35004/A/B	−55°C, +125°C	•	•

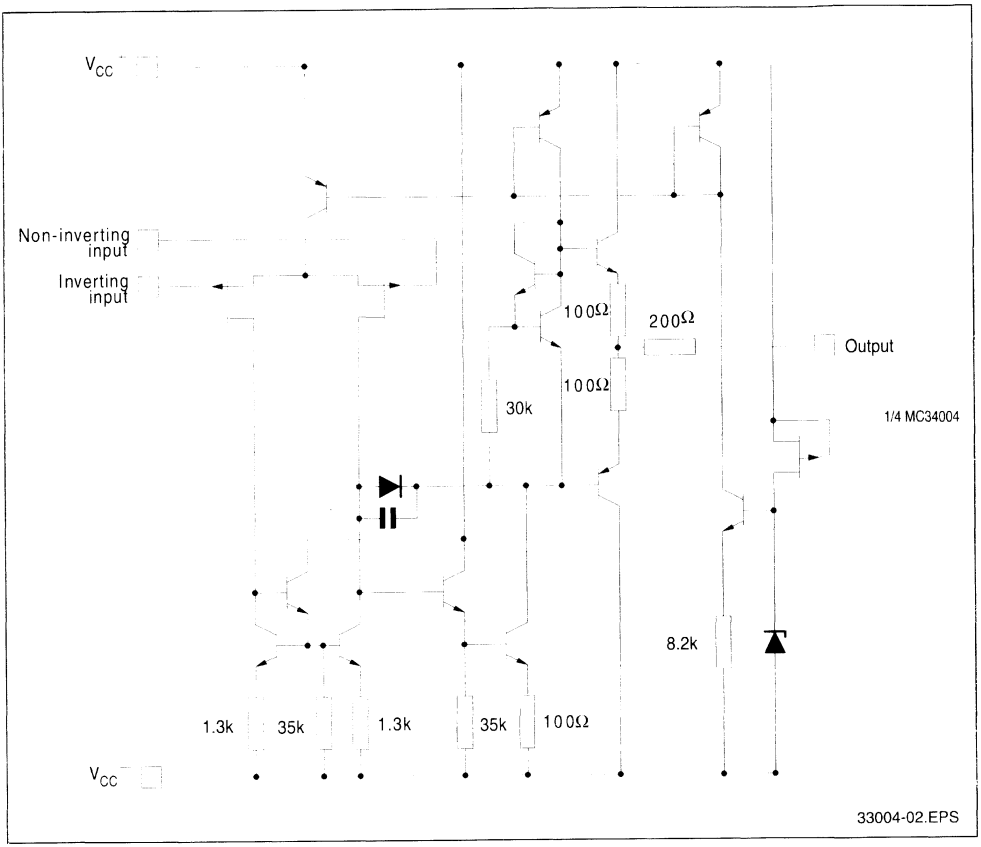
33004-01.TBL

PIN CONNECTIONS (top view)



33004-01.EPS

SCHEMATIC DIAGRAM (each amplifier)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage - (note 1)		±18	V
V_I	Input Voltage - (note 3)		±15	V
V_{id}	Differential Input Voltage - (note 2)		±30	V
P_{tot}	Power Dissipation		680	mW
	Output Short-circuit Duration (note 4)		Infinite	
T_{oper}	Operating Free Air Temperature Range	MC34004, A, B MC33004, A, B MC35004, A, B	0 to 70 –40 to 105 –55 to 125	°C
T_{stg}	Storage Temperature Range		–65 to 150	°C

Notes :
1. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.
2. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and /or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

ELECTRICAL CHARACTERISTICS

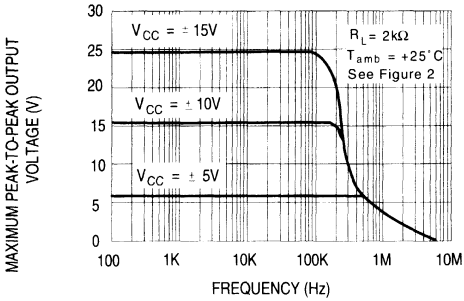
V_{CC} = ±15V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	MC35004A,B MC33004A,B MC34004A,B			MC35004 MC33004 MC34004			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage ($R_S \leq 10k\Omega$) T_{amb} = 25°C MC35004B, MC34004B, MC33004B MC35004A, MC34004A, MC33004A $T_{min.} \leq T_{amb} \leq T_{max.}$ MC35004B, MC34004B, MC33004B MC35004A, MC34004A, MC33004A		 3 1 	 5 2 7 4		 3 	 10 13 	mV
DV_{io}	Input Offset Voltage Drift		10			10		µV/°C
I_{io}	Input Offset Current * T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		5	50 4		5	100 4	pA nA
I_{ib}	Input Bias Current * T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		20	200 20		20	200 20	pA nA
A_{vd}	Large Signal Voltage Gain (R_L = 2kΩ, V_O = ±10V) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	50 25	200		25 15	200		V/mV
SVR	Supply Voltage Rejection Ratio ($R_S \leq 10k\Omega$) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	80 80	86		70 70	86		dB
I_{CC}	Supply Current, per Amp, no Load T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		1.4	2.5 2.8		1.4	2.5 2.8	mA
V_{icm}	Input Common Mode Voltage Range	±11	+15 -12		±11	+15 -12		V
CMR	Common Mode Rejection Ratio ($R_S \leq 10k\Omega$) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	80 80	86		70 70	86		dB
Ios	Output Short-circuit Current T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	10 10	40	60 60	10 10	40	60 60	mA
$\pm V_{OPP}$	Output Voltage Swing T_{amb} = 25°C R_L = 2kΩ R_L = 10kΩ $T_{min.} \leq T_{amb} \leq T_{max.}$ R_L = 2kΩ R_L = 10kΩ	 10 12 10 12	 12 13.5 	 	 10 12 10 12	 12 13.5 	 	V
SR	Slew Rate (V_{in} = 10V, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)	12	16		12	16		V/µs
t_r	Rise Time (V_{in} = 20mV, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)		0.1			0.1		µs
K_{OV}	Overshoot (V_{in} = 20mV, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)		10			10		%
GBP	Gain Bandwidth Product (f = 100kHz, T_{amb} = 25°C, V_{in} = 10mV, R_L = 2kΩ, C_L = 100pF)	2.5	4		2.5	4		MHz
R_i	Input Resistance		10^{12}			10^{12}		Ω
THD	Total Harmonic Distortion (f = 1kHz, A_V = 20dB, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, V_O = $2V_{PP}$)		0.01			0.01		%
e_n	Equivalent Input Noise Voltage (f = 1kHz, R_S = 100Ω)		15			15		$\frac{nV}{\sqrt{Hz}}$
Øm	Phase Margin		45			45		Degrees
V_{O1}/V_{O2}	Channel Separation (A_{vd} = 100)		120			120		dB

The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature.

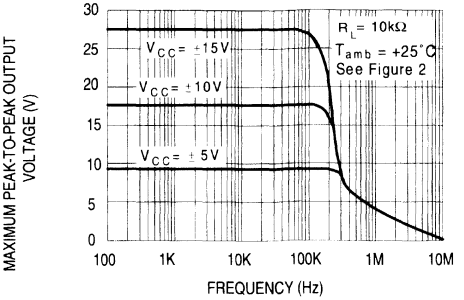
33004-03.TBL

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



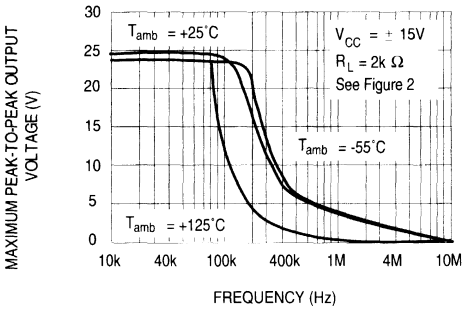
33004-03.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



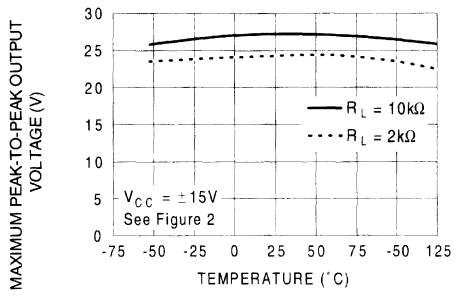
33004-04.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



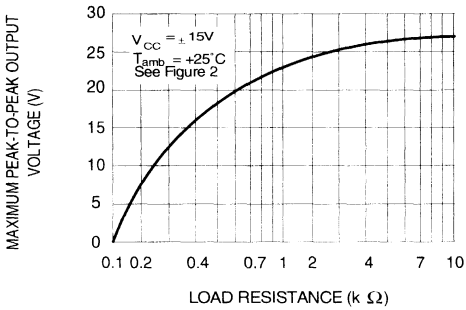
33004-05.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREE AIR TEMP.



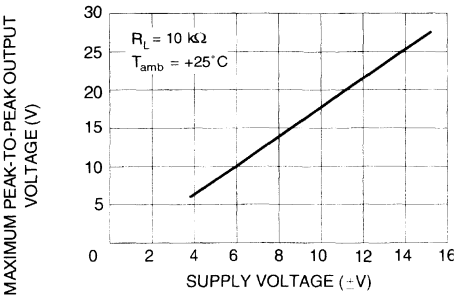
33004-06.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS LOAD RESISTANCE



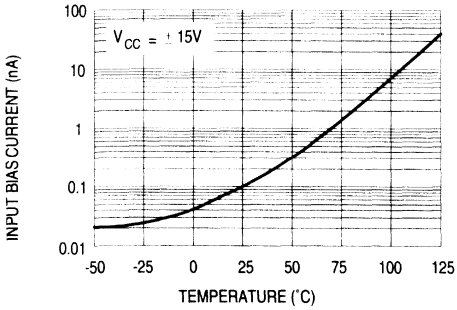
33004-07.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS SUPPLY VOLTAGE



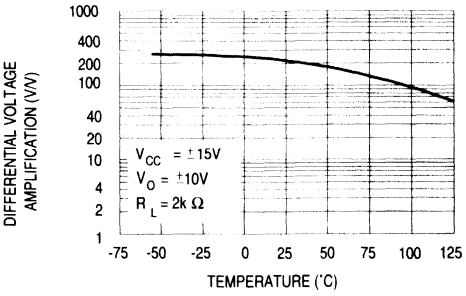
33004-08.EPS

INPUT BIAS CURRENT VERSUS FREE AIR TEMPERATURE



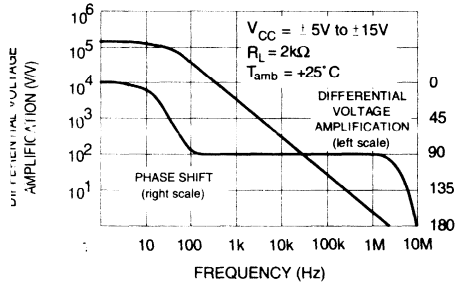
33004-09.EPS

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION VERSUS FREE AIR TEMPERATURE



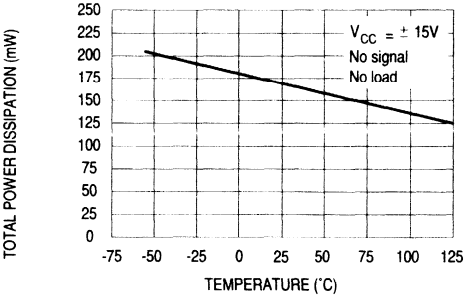
33004-10.EPS

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT VERSUS FREQUENCY



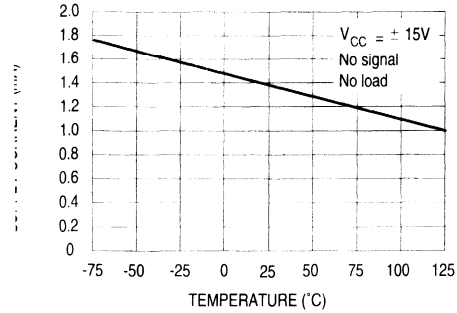
33004-11.EPS

TOTAL POWER DISSIPATION VERSUS FREE AIR TEMPERATURE



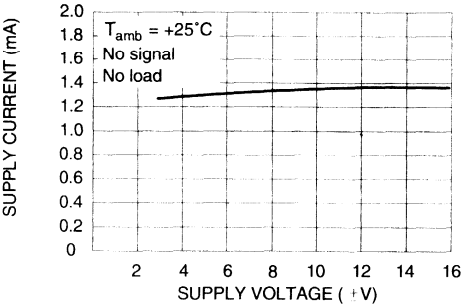
33004-12.EPS

SUPPLY CURRENT PER AMPLIFIER VERSUS FREE AIR TEMPERATURE



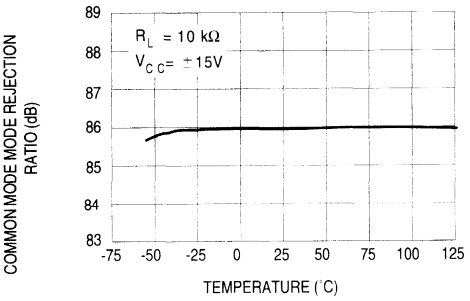
33004-13.EPS

SUPPLY CURRENT PER AMPLIFIER VERSUS SUPPLY VOLTAGE



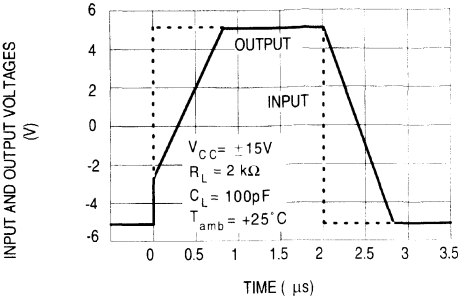
33004-14.EPS

COMMON MODE REJECTION RATIO VERSUS FREE AIR TEMPERATURE



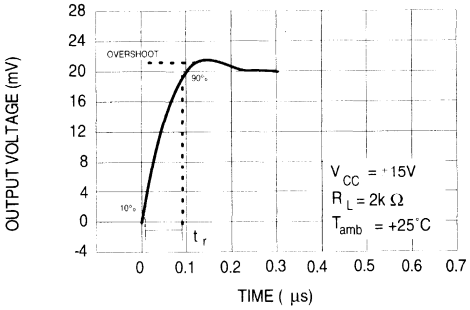
33004-15.EPS

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



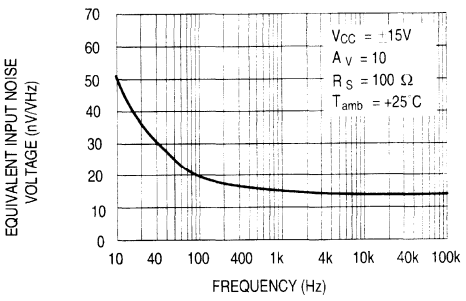
33004-16.EPS

OUTPUT VOLTAGE VERSUS ELAPSED TIME



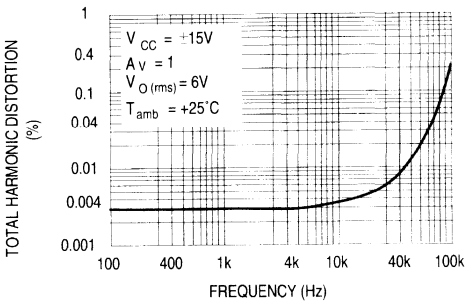
33004-17.EPS

EQUIVALENT INPUT NOISE VOLTAGE VERSUS FREQUENCY



33004-18.EPS

TOTAL HARMONIC DISTORTION VERSUS FREQUENCY



33004-19.EPS

PARAMETER MEASUREMENT INFORMATION

Figure 1 : Voltage Follower

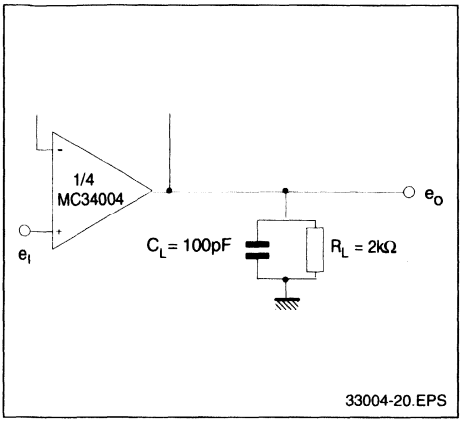
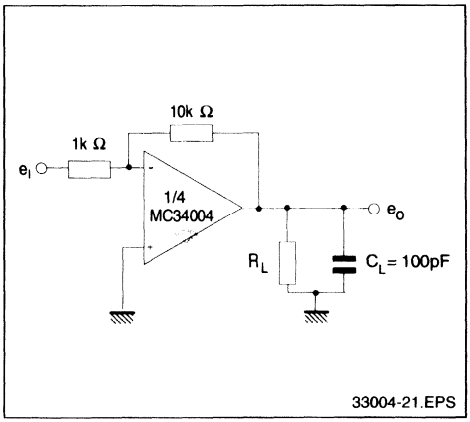
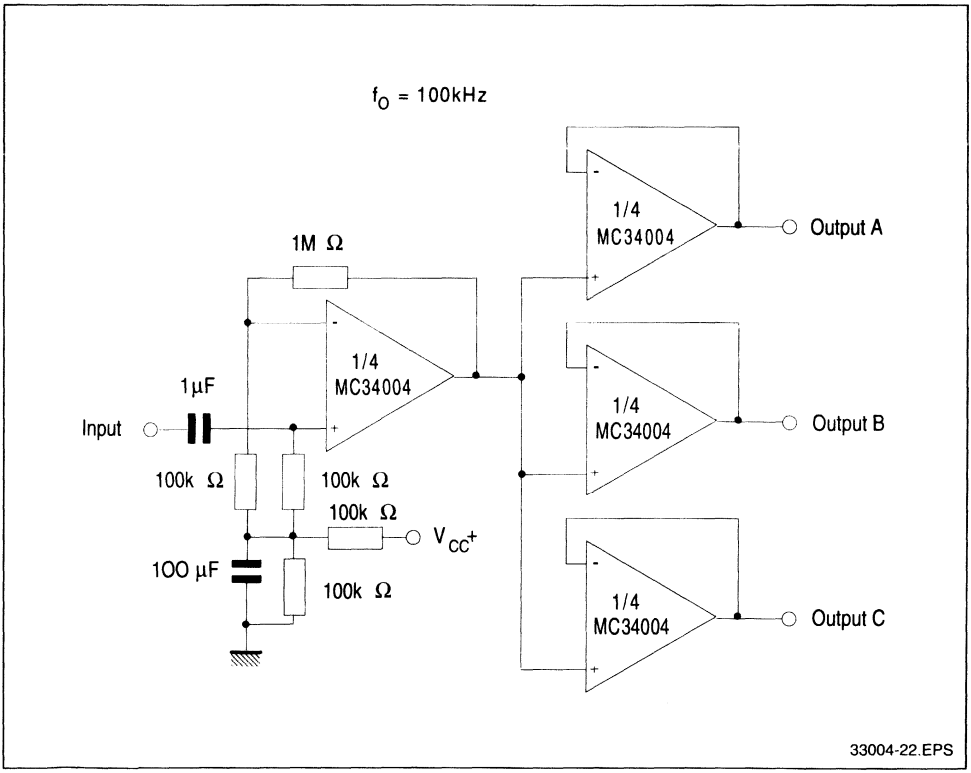


Figure 2 : Gain-of-10 Inverting Amplifier



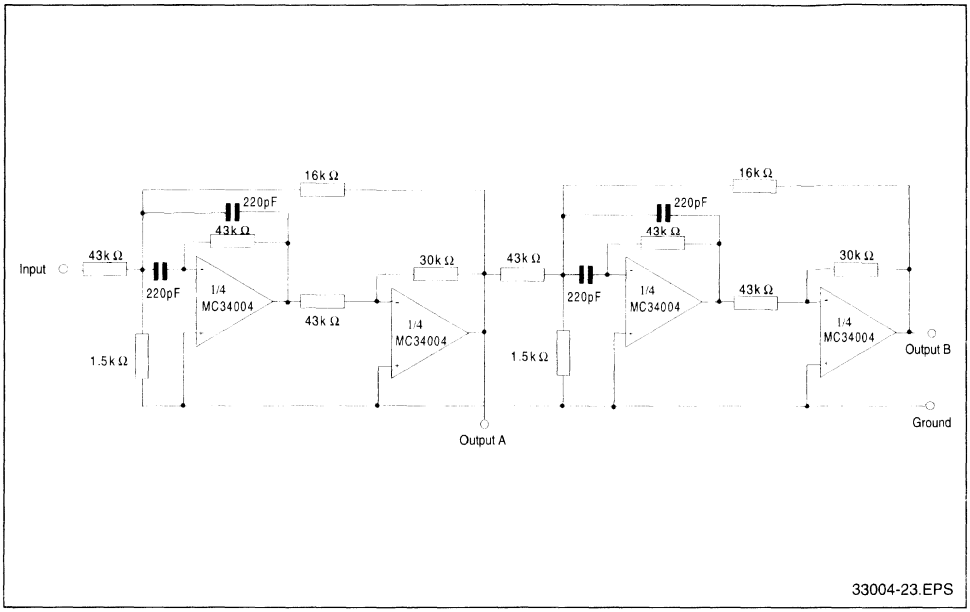
TYPICAL APPLICATIONS

AUDIO DISTRIBUTION AMPLIFIER



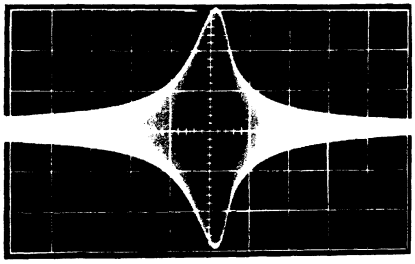
TYPICAL APPLICATIONS (continued)

POSITIVE FEEDBACK BANDPASS FILTER



33004-23.EPS

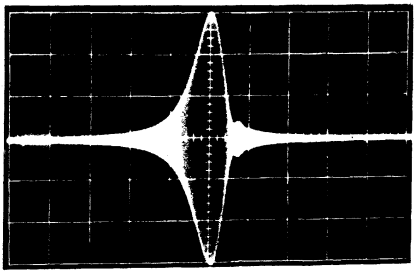
OUTPUT A



33004-24.EPS

SECOND ORDER BANDPASS FILTER
fo = 100kHz ; Q = 30 ; Gain = 4

OUTPUT B



33004-25.EPS

CASCADED BANDPASS FILTER
fo = 100kHz ; Q = 69 ; Gain = 16

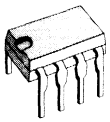
SGS-THOMSON MICROELECTRONICS

MC33078

LOW NOISE DUAL OPERATIONAL AMPLIFIERS

PRELIMINARY DATA

- LOW VOLTAGE NOISE : 4.5nV$\sqrt{Hz}$
- HIGH GAIN BANDWIDTH PRODUCT : 15MHz
- HIGH SLEW RATE : 7.0V/µs
- LOW DISTORTION : 0.002%
- LARGE OUTPUT VOLTAGE SWING : +14.3V/-14.6V
- LOW INPUT OFFSET VOLTAGE
- EXCELLENT FREQUENCY STABILITY
- ESD PROTECTION 2000V



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

DESCRIPTION

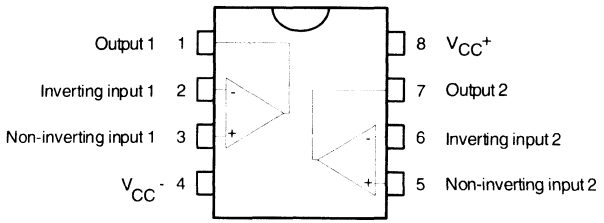
The MC33078 is a monolithic dual operational amplifier dedicated to audio applications. The MC33078 offers low voltage noise (4.5nV$\sqrt{Hz}$) and high frequency performances (15MHz gain bandwidth product, 7V/µs slew rate).
In addition the MC33078 has a very low distortion (0.002%) and excellent phase/gain margins.
The output stage allows a large output voltage swing and symmetrical source and sink currents.

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
MC33078	-40, +105°C	•	•

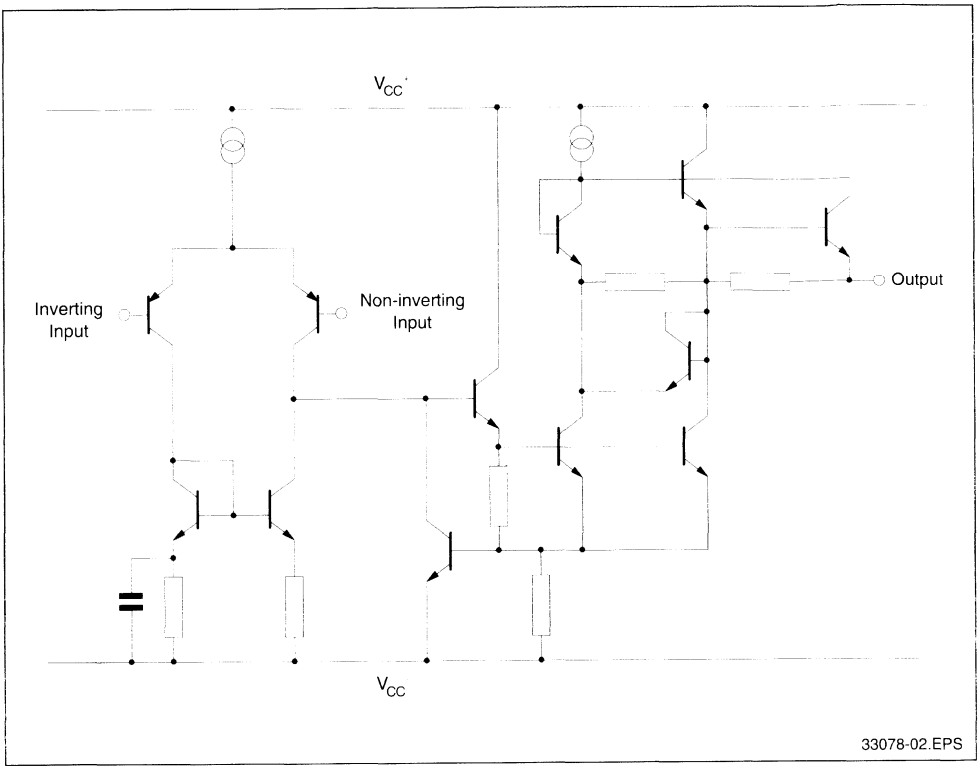
33078-01.TBL

PIN CONNECTIONS (top view)



33078-01.EPS

SCHEMATIC DIAGRAM (1/2 MC33078)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (V_{CC}^+ to V_{CC}^-)	+36	V
V_{id}	Differential Input Voltage - (note 1)	30	V
V_i	Input Voltage - (note 1)	±15	V
	Output Short-Circuit Duration - (note 2)	Infinite	
T_{oper}	Operating Free-air Temperature Range	-40, to +105	°C
T_j	Maximum Junction Temperature	+150	°C
T_{stg}	Storage Temperature	-65 to +150	°C
P_{tot}	Maximum Power Dissipation - (note 2)	500	mW

Notes : 1. Either or both input voltages must not exceed the magnitude of V_{CC}^+ or V_{CC}^-
2. Power dissipation must be considered to ensure maximum junction temperature (T_j) is not exceeded

ELECTRICAL CHARACTERISTICS

V_{CC}^+ = +15V, V_{CC}^- = -15V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage (R_S = 10Ω, V_o = 0V, V_{ic} = 0V) T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$		0.15	2 3	mV
DV_{io}	Input Offset Voltage Drift (R_S = 10Ω, V_{ic} = 0V, V_o = 0V, $T_{min.} \le T_{amb} \le T_{max.}$)		2		µV/°C
I_{io}	Input Offset Current (V_{ic} = 0V, V_O = 0V) T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$		10	150 175	nA
I_{ib}	Input Bias Current (V_{ic} = 0V, V_O = 0V) T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$		250	750 800	nA
V_{icm}	Common Mode Input Voltage Range (ΔV_{IO} = 5mV, V_O = 0V)	±13	±14		V
A_{vd}	Large Signal Voltage Gain (R_L = 2kΩ, V_O = ±10V) T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$	90 85	100		dB
$\pm V_{opp}$	Output Voltage Swing (V_{id} = ±1V) R_L = 600Ω R_L = 600Ω R_L = 2.0kΩ R_L = 2.0kΩ R_L = 10kΩ R_L = 10kΩ	 13.2 13.5 	 12.2 -12.7 14 -14.2 14.3 -14.6	 -13.2 -14	V
CMR	Common Mode Rejection Ratio (V_{ic} = ±13V)	80	100		dB
SVR	Supply Voltage Rejection Ratio (V_{CC}^+ / V_{CC}^- = +15V / -15V to +5V / -5V)	80	105		dB
I_o	Output Short Circuit Current (V_{id} = ±1V, Output to Ground) Source Sink	 15 20	 29 37		mA
I_{CC}	Supply current (V_O = 0V, All Amplifiers) T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$		4	5 5.5	mA
SR	Slew Rate (V_i = -10V to +10V, R_L = 2kΩ, C_L = 100pF, A_V = +1)	5	7		V/µs
GBP	Gain Bandwidth Product (f = 100kHz, R_L = 2kΩ, C_L = 100pF)	10	15		MHz
B	Unity Gain Bandwidth (Open loop)		9		MHz
A_m	Gain Margin (R_L = 2kΩ) C_L = 0pF C_L = 100pF		-11 -6		dB
Øm	Phase Margin (R_L = 2kΩ) C_L = 0pF C_L = 100pF		55 30		Degrees
e_n	Equivalent Input Noise Voltage (R_S = 100Ω, f = 1kHz)		4.5		$\frac{nV}{\sqrt{Hz}}$
i_n	Equivalent Input Noise current (f = 1kHz)		0.5		$\frac{pA}{\sqrt{Hz}}$
THD	Total Harmonic Distortion (R_L = 2kΩ, f = 20Hz to 20kHz, V_O = $3V_{rms}$, A_V = +1)		0.002		%
V_{O1}/V_{O2}	Channel Separation (f = 20Hz to 20kHz)		120		dB
FPB	Full Power Bandwidth (V_O = $27V_{pp}$, R_L = 2kΩ, THD ≤ 1%)		120		kHz
Z_o	Output Impedance (V_O = 0V, f = 9MHz)		37		Ω
R_i	Input Resistance (V_{ic} = 0V)		175		kΩ
C_i	Input Capacitance (V_{ic} = 0V)		12		pF

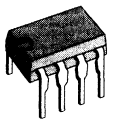
33078-03.TBL

SGS-THOMSON MICROELECTRONICS

MC33171 - MC35171

LOW POWER SINGLE BIPOLAR OPERATIONAL AMPLIFIERS

- GOOD CONSUMPTION/SPEED RATIO : ONLY 200µA FOR 2.1MHz, 2V/µs
- SINGLE (OR DUAL) SUPPLY OPERATION FROM +4V TO +44V (±2V TO ±22V)
- WIDE INPUT COMMON MODE VOLTAGE RANGE INCLUDING V_{CC}^-
- LOW LEVEL OUTPUT VOLTAGE CLOSE TO V_{CC}^-: 100mV TYPICAL
- PIN TO PIN COMPATIBLE WITH STANDARD SINGLE OP AMPs



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

DESCRIPTION

The MC33171 series are single bipolar operational amplifiers offering both low consumption (200µA) and good speed (2.1MHz, 2V/µs).

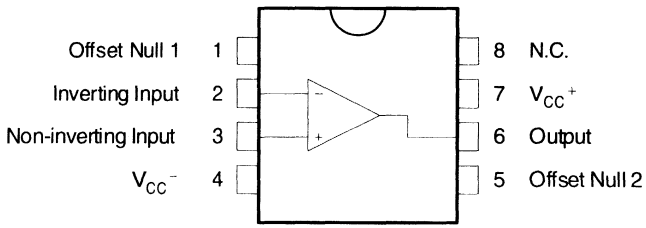
Moreover the Input Common Mode Range extends down to the lower supply rail, allowing single supply operation from +4V to +44V.

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
MC33171	-40°C, +105°C	•	•
MC35171	-55°C, +125°C	•	•
Example: MC33171N			

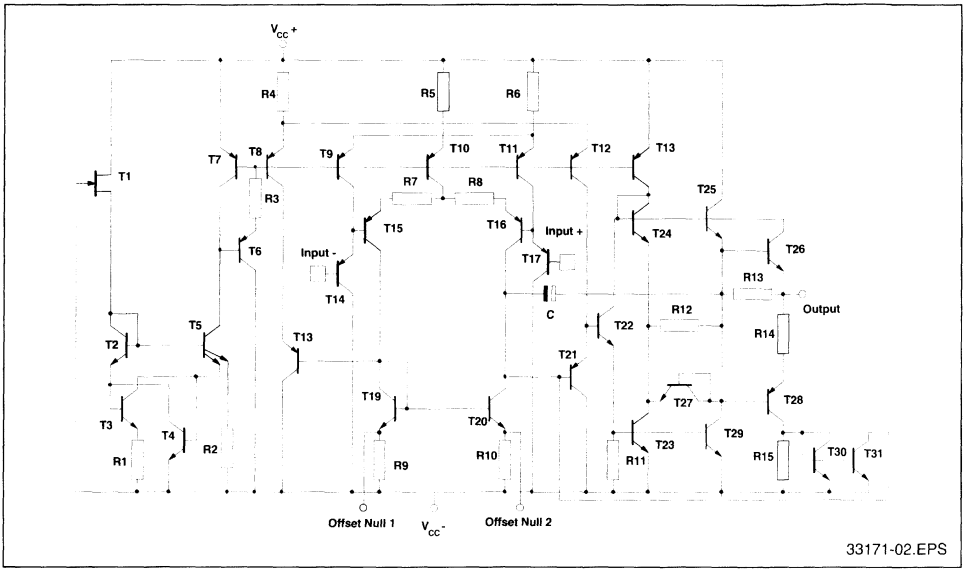
33171-01.TBL

PIN CONNECTIONS (top view)

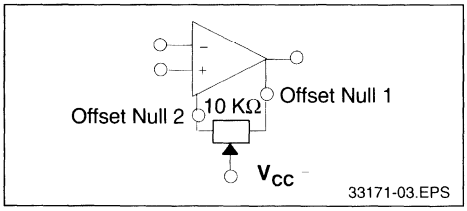


33171-01.EPS

SCHEMATIC DIAGRAM



INPUT OFFSET VOLTAGE NULL CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		±22	V
V_{id}	Differential Input Voltage		(Note 1)	V
V_i	Input Voltage		(Note 1)	V
	Output Short Circuit Duration		Indefinite	s
T_{oper}	Operating Temperature Range	MC33171 MC35171	-40 to 105 -55 to 125	°C
T_j	Junction Temperature		150	°C
T_{stg}	Storage Temperature		-65 to 150	°C

Note 1: Either or both input voltages must not exceed the magnitude of V_{CC}.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage Range	±2 to ±22	V

ELECTRICAL CHARACTERISTICS

V_{CC} = ±15V, R_L connected to Ground, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage V_{CC} = ±15V, V_{cm} = 0V V_{CC}^+ = 5V, V_{CC}^- = 0V, V_{cm} = 0V V_{CC}^+ = 5V, V_{cm} = 0V, $T_{min.} \le T_{amb} \le T_{max.}$		 1 1	 4.5 5 6.5	mV
DV_{io}	Input Offset Voltage Drift		10		µV/°C
I_{io}	Input Offset Current (V_{cm} = 0V) $T_{min.} \le T_{amb} \le T_{max.}$		5	20 40	nA
I_{ib}	Input Bias Current (V_{cm} = 0V) $T_{min.} \le T_{amb} \le T_{max.}$		20	100 200	nA
A_{vd}	Large Signal Voltage Gain (R_L = 10kΩ, V_O = ±10V) $T_{min.} \le T_{amb} \le T_{max.}$	50 25	100		V/mV
V_{OH}	High Level Output Voltage V_{CC}^+ = 5V, V_{CC}^- = 0V, R_L = 10kΩ V_{CC} = ±15V, R_L = 10kΩ V_{CC} = ±15V, R_L = 10kΩ, $T_{min.} \le T_{amb} \le T_{max.}$	 3.5 13.6 13.3	 4.2 14.2		V
V_{OL}	Low Level Output Voltage V_{CC}^+ = 5V, V_{CC}^- = 0V, R_L = 10kΩ V_{CC} = ±15V, R_L = 10kΩ V_{CC} = ±15V, R_L = 10kΩ, $T_{min.} \le T_{amb} \le T_{max.}$		 0.1 -14	 0.15 -13.6 -13.3	V
I_{sc}	Output Short Circuit Current (V_{id} = 1V, V_O = 0V) Source Sink	 3 15	 6 27		mA
V_{icm}	Input Common Mode Voltage Range $T_{min.} \le T_{amb} \le T_{max.}$	0 to V_{CC}^- 1.8 0 to V_{CC}^- 2.2			V
CMR	Common Mode Rejection Ratio (V_i = $V_{icm\ min.}$)	80	100		dB
SVR	Supply Voltage Rejection Ratio (V_{CC} = ±5 to ±15V)	80	100		dB
I_{CC}	Supply Current V_{CC}^+ = 5V, V_{CC}^- = 0V, no load V_{CC} = ±15V, no load V_{CC} = ±15V, no load, $T_{min.} \le T_{amb} \le T_{max.}$		 200 220	 250 250 300	µA
SR	Slew Rate (V_i = ±10V, R_L = 10kΩ, C_L = 100pF)	1.4	2		V/µs
GBP	Gain Bandwidth Product (R_L = 10kΩ, C_L = 100pF, f = 100kHz)	1.4	2.1		MHz
∅m	Phase Margin (R_L = 10kΩ, C_L = 100pF)		45		Degrees
e_n	Equivalent Input Noise Voltage (f = 1kHz)		29		$\frac{nV}{\sqrt{Hz}}$
THD	Total Harmonic Distortion		0.05		%

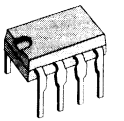
33171-04.TBL

SGS-THOMSON MICROELECTRONICS

MC33172 - MC35172

LOW POWER DUAL BIPOLAR OPERATIONAL AMPLIFIERS

- GOOD CONSUMPTION/SPEED RATIO : ONLY 200µA/Amp FOR 2.1MHz, 2V/µs
- SINGLE (OR DUAL) SUPPLY OPERATION FROM +4V TO +44V (±2V TO ±22V)
- WIDE INPUT COMMON MODE VOLTAGE RANGE INCLUDING V_{CC}^-
- LOW LEVEL OUTPUT VOLTAGE CLOSE TO V_{CC}^- : 100mV TYPICAL
- PIN TO PIN COMPATIBLE WITH STANDARD DUAL OP AMPs



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

DESCRIPTION

The MC33172 series are dual bipolar operational amplifiers offering both low consumption (200µA/Amp) and good speed (2.1MHz, 2V/µs).

Moreover the Input Common Mode Range extends down to the lower supply rail, allowing single supply operation from +4V to +44V.

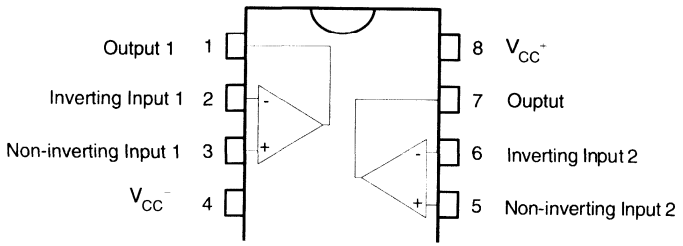
ORDER CODES

Part Number	Temperature Range	Package	
		N	D
MC33172	-40°C, +105°C	•	•
MC35172	-55°C, +125°C	•	•

Example: MC33172N

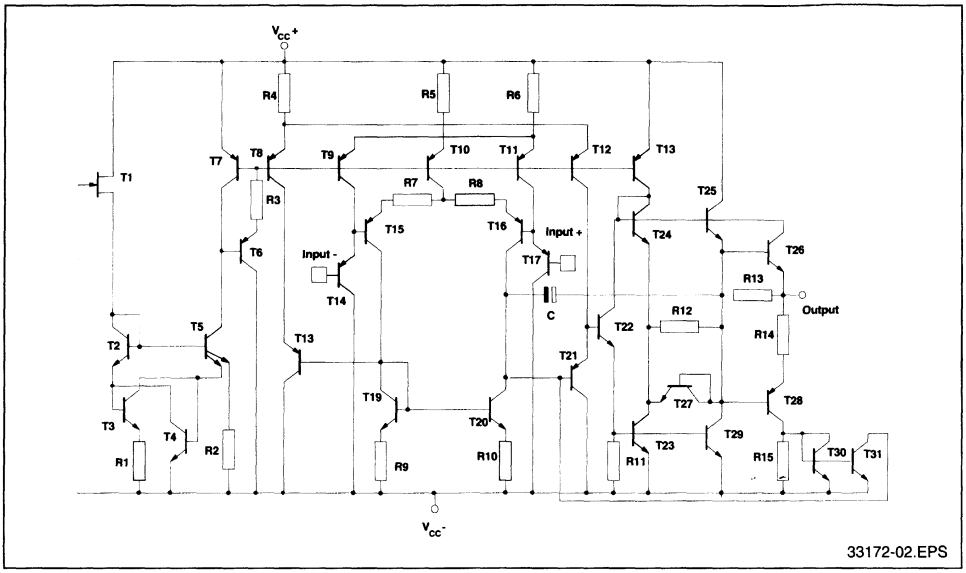
33172-01.TBL

PIN CONNECTIONS (top view)



33172-01.EPS

SCHEMATIC DIAGRAM (for 1/2 MC33172)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		±22	V
V_{id}	Differential Input Voltage		(Note 1)	V
V_i	Input Voltage		(Note 1)	V
	Output Short Circuit Duration		Indefinite	s
T_{oper}	Operating Temperature Range	MC33172 MC35172	-40 to 105 -55 to 125	°C
T_j	Junction Temperature		150	°C
T_{stg}	Storage Temperature		-65 to 150	°C

Note 1: Either or both input voltages must not exceed the magnitude of V_{CC}.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage Range	±2 to ±22	V

ELECTRICAL CHARACTERISTICS

V_{CC} = ±15V, R_L connected to Ground, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage V_{CC} = ± 15V, V_{cm} = 0V V_{CC}^+ = 5V, V_{CC}^- = 0V, V_{cm} = 0V V_{CC} = ±15V, V_{cm} = 0V, $T_{min.} \le T_{amb} \le T_{max.}$		 1 1	 4.5 5 6.5	mV
DV_{io}	Input Offset Voltage Drift		10		µV/°C
I_{io}	Input Offset Current (V_{cm} = 0V) $T_{min.} \le T_{amb} \le T_{max.}$		5	20 40	nA
I_{ib}	Input Bias Current (V_{cm} = 0V) $T_{min.} \le T_{amb} \le T_{max.}$		20	100 200	nA
A_{vd}	Large Signal Voltage Gain (R_L = 10kΩ, V_O = ±10V) $T_{min.} \le T_{amb} \le T_{max.}$	50 25	100		V/mV
V_{OH}	High Level Output Voltage V_{CC}^+ = 5V, V_{CC}^- = 0V, R_L = 10kΩ V_{CC} = ±15V, R_L = 10kΩ V_{CC} = ±15V, R_L = 10kΩ, $T_{min.} \le T_{amb} \le T_{max.}$	 3.5 13.6 13.3	 4.2 14.2		V
V_{OL}	Low Level Output Voltage V_{CC}^+ = 5V, V_{CC}^- = 0V, R_L = 10kΩ V_{CC} = ±15V, R_L = 10kΩ V_{CC} = ±15V, R_L = 10kΩ, $T_{min.} \le T_{amb} \le T_{max.}$		 0.1 -14	 0.15 -13.6 -13.3	V
I_{sc}	Output Short Circuit Current (V_{id} = 1V, V_O = 0V) Source Sink	 3 15	 6 27		mA
V_{icm}	Input Common Mode Voltage Range $T_{min.} \le T_{amb} \le T_{max.}$	0 to Vcc-1.8 0 to Vcc-2.2			V
CMR	Common Mode Rejection Ratio (V_i = $V_{icm\ min.}$)	80	100		dB
SVR	Supply Voltage Rejection Ratio (V_{CC} = ± 5 to ±15V)	80	100		dB
I_{CC}	Supply Current (Per Amplifier) V_{CC}^+ = 5V, V_{CC}^- = 0V, no load V_{CC} = ±15 V, no load V_{CC} = ±15V, no load, $T_{min.} \le T_{amb} \le T_{max.}$		 200 220	 250 250 300	µA
SR	Slew Rate (V_i = ±10V, R_L = 10kΩ, C_L = 100pF)	1.4	2		V/µs
GBP	Gain Bandwidth Product (R_L = 10kΩ, C_L = 100pF, f = 100kHz)	1.4	2.1		MHz
∅m	Phase Margin (R_L = 10kΩ, C_L = 100pF)		45		Degrees
e_n	Equivalent Input Noise Voltage (f = 1kHz)		29		$\frac{nV}{\sqrt{Hz}}$
THD	Total Harmonic Distortion		0.05		%
V_{O1}/V_{O2}	Channel Separation		120		dB

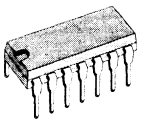
33172-04.TBL

SGS-THOMSON MICROELECTRONICS

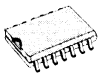
MC33174 - MC35174

LOW POWER QUAD BIPOLAR OPERATIONAL AMPLIFIERS

- GOOD CONSUMPTION/SPEED RATIO : ONLY 200µA/Amp FOR 2.1MHz, 2V/µs
- SINGLE (OR DUAL) SUPPLY OPERATION FROM +4V TO +44V (±2V TO ±22V)
- WIDE INPUT COMMON MODE VOLTAGE RANGE INCLUDING V_{CC}^-
- LOW LEVEL OUTPUT VOLTAGE CLOSE TO V_{CC}^-: 100mV TYPICAL
- PIN TO PIN COMPATIBLE WITH STANDARD QUAD OP AMPs
- ESD PROTECTION



N
DIP14
(Plastic Package)



D
SO14
(Plastic Micropackage)

DESCRIPTION

The MC33174 series are quad bipolar operational amplifiers offering both low consumption (200µA/Amp) and good speed (2.1MHz, 2V/µs). Moreover the Input Common Mode Range extends down to the lower supply rail, allowing single supply operation from +4V to +44V.

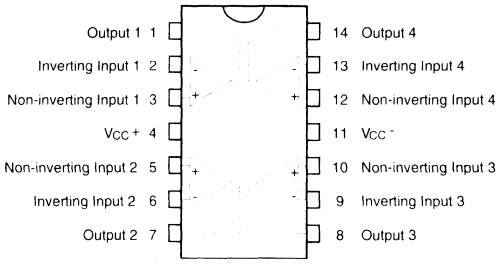
ORDER CODES

Part Number	Temperature Range	Package	
		N	D
MC33174	-40°C, +105°C	•	•
MC35174	-55°C, +125°C	•	•

Example: MC33174N

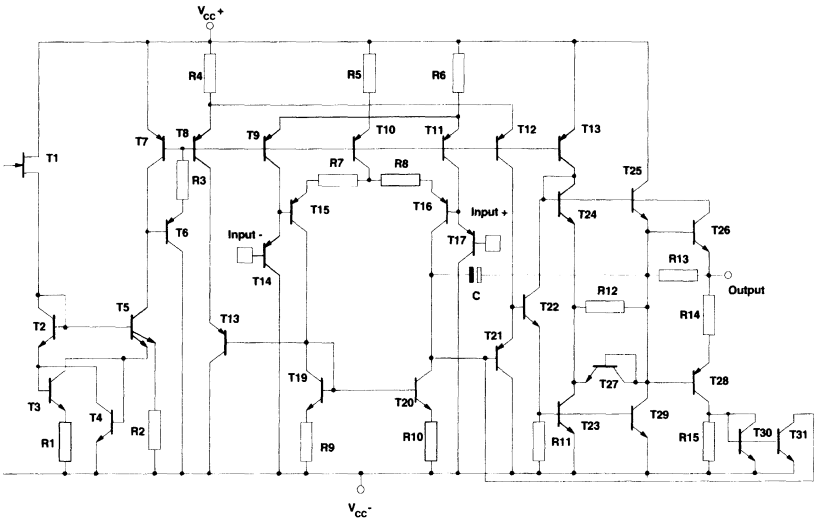
33174-01.TBL

PIN CONNECTIONS (top view)



33174-01.EPS

SCHEMATIC DIAGRAM (for 1/4 MC33174)



33174-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		±22	V
V_{id}	Differential Input Voltage		(Note 1)	V
V_i	Input Voltage		(Note 1)	V
	Output Short Circuit Duration		Indefinite	s
T_{oper}	Operating Temperature Range	MC33174 MC35174	-40 to 105 -55 to 125	°C
T_j	Junction Temperature		150	°C
T_{stg}	Storage Temperature		-65 to 150	°C

Note 1: Either or both input voltages must not exceed the magnitude of V_{CC}.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage Range	±2 to ±22	V

ELECTRICAL CHARACTERISTICS

V_{CC} = ±15V, R_L connected to Ground, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage V_{CC} = ±15V, V_{cm} = 0V V_{CC}^+ = 5V, V_{CC}^- = 0V V_{cm} = 0V V_{CC} = ±15V, V_{cm} = 0V $T_{min.} \le T_{amb} \le T_{max.}$		 1 1	 4.5 5 6.5	mV
DV_{io}	Input Offset Voltage Drift		10		µV/°C
I_{io}	Input Offset Current (V_{cm} = 0V) $T_{min.} \le T_{amb} \le T_{max.}$		5	20 40	nA
I_{ib}	Input Bias Current (V_{cm} = 0V) $T_{min.} \le T_{amb} \le T_{max.}$		20	100 200	nA
A_{vd}	Large Signal Voltage Gain (R_L = 10kΩ, V_O = ±10V) $T_{min.} \le T_{amb} \le T_{max.}$	50 25	100		V/mV
V_{OH}	High Level Output Voltage V_{CC}^+ = 5V, V_{CC}^- = 0V, R_L = 10kΩ V_{CC} = ±15V, R_L = 10kΩ V_{CC} = ±15V, R_L = 10kΩ, $T_{min.} \le T_{amb} \le T_{max.}$	 3.5 13.6 13.3	 4.2 14.2		V
V_{OL}	Low Level Output Voltage V_{CC}^+ = 5V, V_{CC}^- = 0V, R_L = 10kΩ V_{CC} = ±15V, R_L = 10kΩ V_{CC} = ±15V, R_L = 10kΩ, $T_{min.} \le T_{amb} \le T_{max.}$		 0.1 -14	 0.15 -13.6 -13.3	V
I_{sc}	Output Short Circuit Current (V_{id} = 1V, V_O = 0V) Source Sink	 3 15	 6 27		mA
V_{icm}	Input Common Mode Voltage Range $T_{min.} \le T_{amb} \le T_{max.}$	0 to Vcc-1.8 0 to Vcc-2.2			V
CMR	Common Mode Rejection Ratio (V_i = $V_{icm\ min.}$)	80	100		dB
SVR	Supply Voltage Rejection Ratio (V_{CC} = ±5 to ±15V)	80	100		dB
I_{CC}	Supply Current (Per Amplifier) V_{CC}^+ = 5V, V_{CC}^- = 0V, no load V_{CC} = ±15V, no load V_{CC} = ±15V, no load, $T_{min.} \le T_{amb} \le T_{max.}$		 200 220	 250 250 300	µA
SR	Slew Rate (V_i = ±10V, R_L = 10kΩ, C_L = 100pF)	1.4	2		V/µs
GBP	Gain Bandwidth Product (R_L = 10kΩ, C_L = 100pF, f = 100kHz)	1.4	2.1		MHz
∅m	Phase Margin (R_L = 10kΩ, C_L = 100pF)		45		Degrees
e_n	Equivalent Input Noise Voltage (f = 1kHz)		29		$\frac{nV}{\sqrt{Hz}}$
THD	Total Harmonic Distortion		0.05		%
V_{O1}/V_{O2}	Channel Separation		120		dB

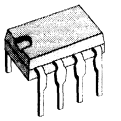
33174-04.TBL

SGS-THOMSON MICROELECTRONICS

NE555
SA555 - SE555

GENERAL PURPOSE SINGLE BIPOLAR TIMERS

- LOW TURN OFF TIME
- MAXIMUM OPERATING FREQUENCY GREATER THAN 500kHz
- TIMING FROM MICROSECONDS TO HOURS
- OPERATES IN BOTH ASTABLE AND MONOSTABLE MODES
- HIGH OUTPUT CURRENT CAN SOURCE OR SINK 200mA
- ADJUSTABLE DUTY CYCLE
- TTL COMPATIBLE
- TEMPERATURE STABILITY OF 0.005% PER°C



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

J
CERDIP8
(Cerdip Package)

H
TO99
(Metal Can)

DESCRIPTION

The NE555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA. The NE555 is available in plastic and ceramic minidip package and in a 8-lead micropackage and in metal can package version.

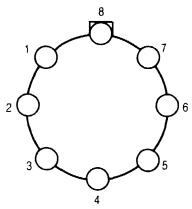
ORDER CODES

Part Number	Temperature Range	Package			
		H	N	J	D
NE555	0°C, 70°C	•	•	•	•
SA555	-40°C, 105°C	•	•	•	•
SE555	-55°C, 125°C	•	•	•	•

555-01.TBL

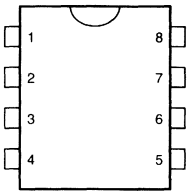
PIN CONNECTIONS (top views)

TO99



555-01.EPS

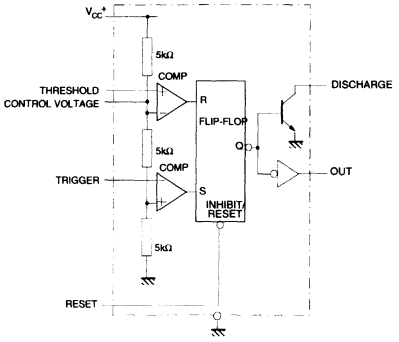
DIP8/CERDIP8
SO8



555-02.EPS

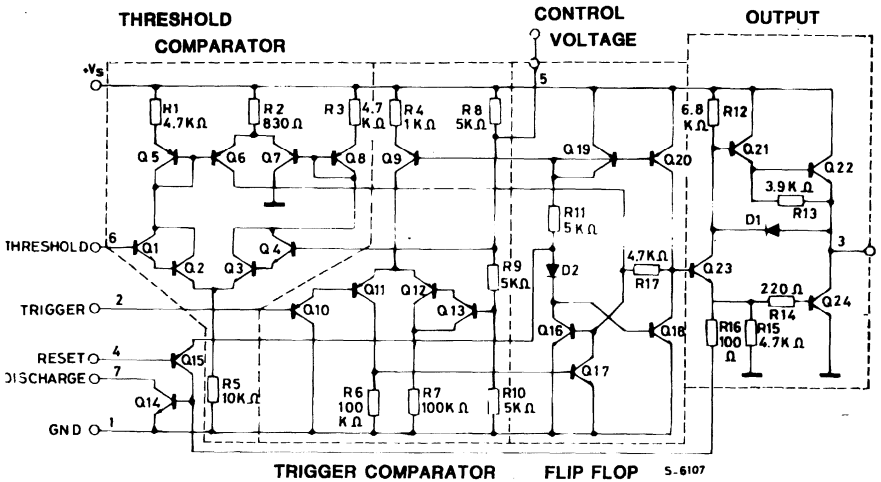
1 - GND
2 - Trigger
3 - Output
4 - Reset
5 - Control voltage
6 - Threshold
7 - Discharge
8 - V_{CC}

BLOCK DIAGRAM



555-03.EPS

SCHEMATIC DIAGRAM



555-04.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{cc}	Supply Voltage		18	V
T_{oper}	Operating Free Air Temperature Range	for NE555 for SA555 for SE555	0 to 70 –40 to 105 –55 to 125	°C
T_j	Junction Temperature		150	°C
T_{stg}	Storage Temperature Range		–65 to 150	°C

555-02.TRI

OPERATING CONDITIONS

Symbol	Parameter	SE555	NE555 - SA555	Unit
V_{CC}	Supply Voltage	4.5 to 18	4.5 to 16	V
V_{th}, V_{trig}, V_{cl}, V_{reset}	Maximum Input Voltage	V_{CC}	V_{CC}	V

555-03.TBL

ELECTRICAL CHARACTERISTICS

T_{amb} = +25°C, V_{CC} = +5V to +15V (unless otherwise specified)

Symbol	Parameter	SE555			NE555 - SA555			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{CC}	Supply Current (R_L ∞) (- note 1)							mA
	Low State V_{CC} = +5V		3	5		3	6	
	V_{CC} = +15V		10	12		10	15	
	High State V_{CC} = 5V		2			2		
	Timing Error (monostable) (R_A = 2k to 100kΩ, C = 0.1µF)							
	Initial Accuracy - (note 2)		0.5	2		1	3	%
	Drift with Temperature		30	100		50		ppm/°C
	Drift with Supply Voltage		0.05	0.2		0.1	0.5	%/V
	Timing Error (astable) (R_A, R_B = 1kΩ to 100kΩ, C = 0.1µF, V_{CC} = +15V)							
	Initial Accuracy - (note 2)		1.5			2.25		%
	Drift with Temperature		90			150		ppm/°C
	Drift with Supply Voltage		0.15			0.3		%/V
V_{CL}	Control Voltage level							V
	V_{CC} = +15V	9.6	10	10.4	9	10	11	
	V_{CC} = +5V	2.9	3.33	3.8	2.6	3.33	4	
V_{th}	Threshold Voltage							V
	V_{CC} = +15V	9.4	10	10.6	8.8	10	11.2	
	V_{CC} = +5V	2.7	3.33	4	2.4	3.33	4.2	
I_{th}	Threshold Current - (note 3)		0.1	0.25		0.1	0.25	µA
V_{trig}	Trigger Voltage							V
	V_{CC} = +15V	4.8	5	5.2	4.5	5	5.6	
	V_{CC} = +5V	1.45	1.67	1.9	1.1	1.67	2.2	
I_{trig}	Trigger Current (V_{trig} = 0V)		0.5	0.9		0.5	2.0	µA
V_{reset}	Reset Voltage - (note 4)	0.4	0.7	1	0.4	0.7	1	V
I_{reset}	Reset Current							mA
	V_{reset} = +0.4V		0.1	0.4		0.1	0.4	
	V_{reset} = 0V		0.4	1		0.4	1.5	
V_{OL}	Low Level Output Voltage							V
	V_{CC} = +15V, $I_{O(sink)}$ = 10mA		0.1	0.15		0.1	0.25	
	$I_{O(sink)}$ = 50mA		0.4	0.5		0.4	0.75	
	$I_{O(sink)}$ = 100mA		2	2.2		2	2.5	
	$I_{O(sink)}$ = 200mA		2.5			2.5		
	V_{CC} = +5V, $I_{O(sink)}$ = 8mA		0.1	0.25		0.3	0.4	
	$I_{O(sink)}$ = 5mA		0.05	0.2		0.25	0.35	
V_{OH}	High Level Output Voltage							V
	V_{CC} = +15V, $I_{O(source)}$ = 200mA		12.5			12.5		
	$I_{O(source)}$ = 100mA	13	13.3		12.75	13.3		
	V_{CC} = +5V, $I_{O(source)}$ = 100mA	3	3.3		2.75	3.3		

555-04.TBL

Notes : 1. Supply current when output is high is typically 1mA less.
2. Tested at V_{CC} = +5V and V_{CC} = +15V.
3. This will determine the maximum value of R_A + R_B for +15V operation the max total is R = 20MΩ and for 5V operation, the max total R = 3.5MΩ.

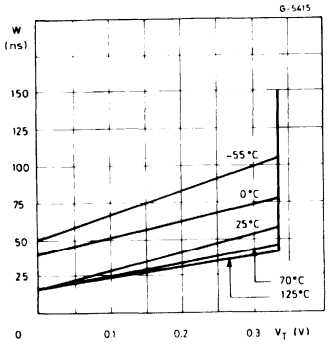
ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	SE555			NE555 - SA555			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
$I_{dis(off)}$	Discharge Pin Leakage Current (output high) (V_{dis} = 10V)		20	100		20	100	nA
$V_{dis(sat)}$	Discharge pin Saturation Voltage (output low) - (note 5) V_{CC} = +15V, I_{dis} = 15mA V_{CC} = +5V, I_{dis} = 4.5mA		 180 80	 480 200		 180 80	 480 200	mV
t_r t_f	Output Rise Time Output Fall Time		100 100	200 200		100 100	300 300	ns
t_{off}	Turn off Time - (note 6) (V_{reset} = V_{CC})		0.5			0.5		µs

555-05.TBL

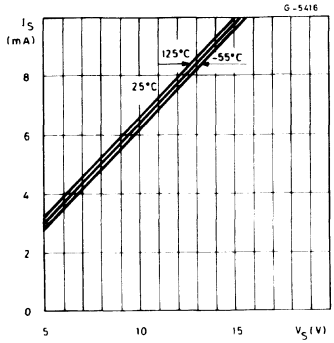
Notes : 5. No protection against excessive Pin 7 current is necessary, providing the package dissipation rating will not be exceeded.
6. Time mesaured from a positive going input pulse from 0 to 0.8x V_{CC} into the threshold to the drop from high to low of the output trigger is tied to treshold.

Figure 1 : Minimum Pulse Width Required for Trigering



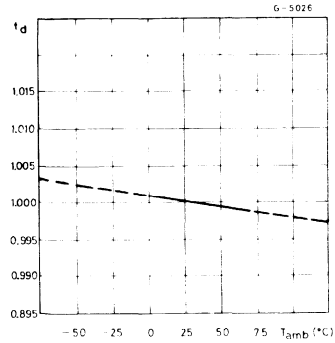
555-05.EPS

Figure 2 : Supply Current versus Supply Voltage



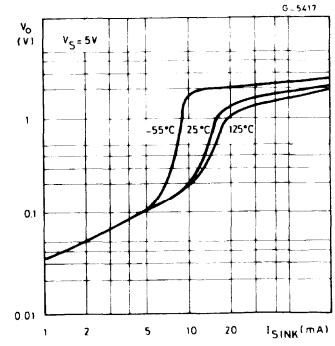
555-06.EPS

Figure 3 : Delay Time versus Temperature



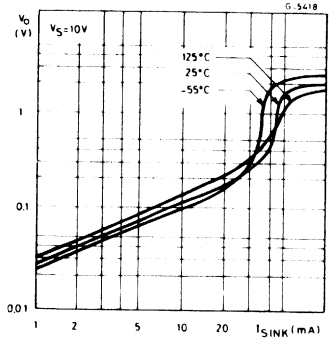
555-07.EPS

Figure 4 : Low Output Voltage versus Output Sink Current



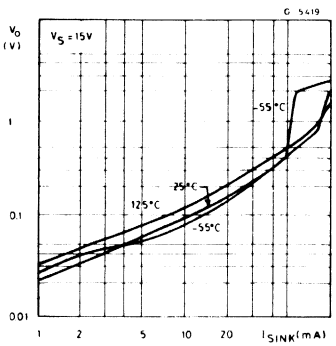
555-08.EPS

Figure 5 : Low Output Voltage versus Output Sink Current



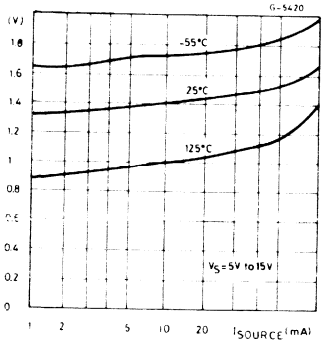
555-09.EPS

Figure 6 : Low Output Voltage versus Output Sink Current



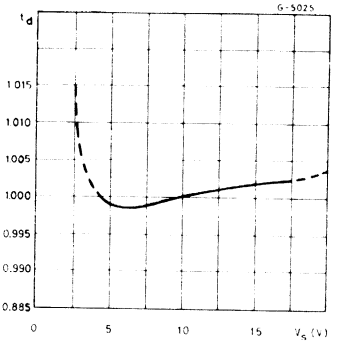
555-10.EPS

Figure 7 : High Output Voltage Drop versus Output



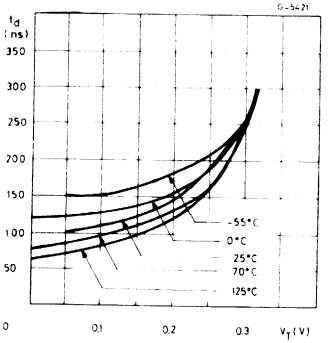
555-11.EPS

Figure 8 : Delay Time versus Supply Voltage



555-12.EPS

Figure 9 : Propagation Delay versus Voltage Level of Trigger Value



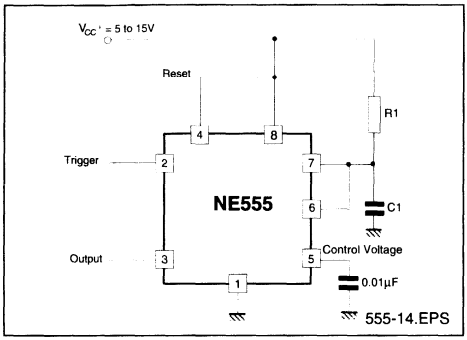
555-13.EPS

APPLICATION INFORMATION

MONOSTABLE OPERATION

In the monostable mode, the timer functions as a one-shot. Referring to figure 10 the external capacitor is initially held discharged by a transistor inside the timer.

Figure 10



The circuit triggers on a negative-going input signal when the level reaches 1/3 Vcc. Once triggered, the circuit remains in this state until the set time has elapsed, even if it is triggered again during this interval. The duration of the output HIGH state is given by $t = 1.1\ R_1C_1$ and is easily determined by figure 12.

Notice that since the charge rate and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the reset terminal (pin 4) and the trigger terminal (pin 2) during the timing cycle discharges the external capacitor and causes the cycle to start over. The timing cycle now starts on the positive edge of the reset pulse. During the time the reset pulse in applied, the output is driven to its LOW state.

When a negative trigger pulse is applied to pin 2, the flip-flop is set, releasing the short circuit across the external capacitor and driving the output HIGH. The voltage across the capacitor increases exponentially with the time constant $\tau = R_1C_1$. When the voltage across the capacitor equals 2/3 V_{cc}, the comparator resets the flip-flop which then discharge the capacitor rapidly and drivers the output to its LOW state.

Figure 11 shows the actual waveforms generated in this mode of operation.

When Reset is not used, it should be tied high to avoid any possibly or false triggering.

Figure 11

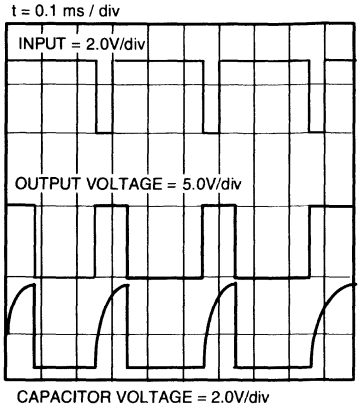
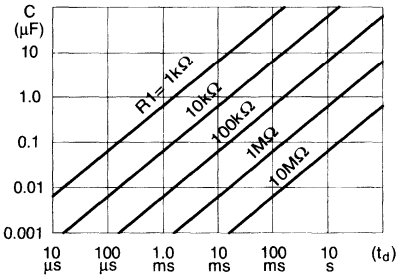


Figure 12



ASTABLE OPERATION

When the circuit is connected as shown in figure 13 (pin 2 and 6 connected) it triggers itself and free runs as a multivibrator. The external capacitor charges through R_1 and R_2 and discharges through R_2 only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

In the astable mode of operation, C_1 charges and discharges between 1/3 V_{cc} and 2/3 Vcc. As in the triggered mode, the charge and discharge times and therefore frequency are independent of the supply voltage.

Figure 13

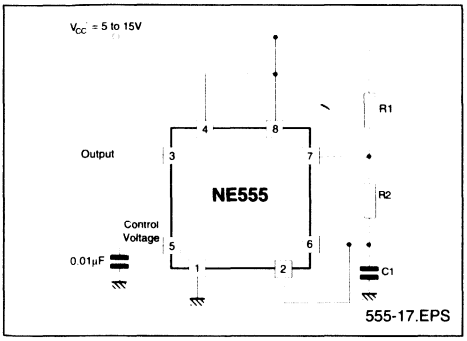


Figure 14 shows actual waveforms generated in this mode of operation.

The charge time (output HIGH) is given by :

$t_1 = 0.693 (R_1 + R_2) C_1$

and the discharge time (output LOW) by :

$t_2 = 0.693 (R_2) C_1$

Thus the total period T is given by :

$T = t_1 + t_2 = 0.693 (R_1 + 2R_2) C_1$

The frequency ofoscillation is them :

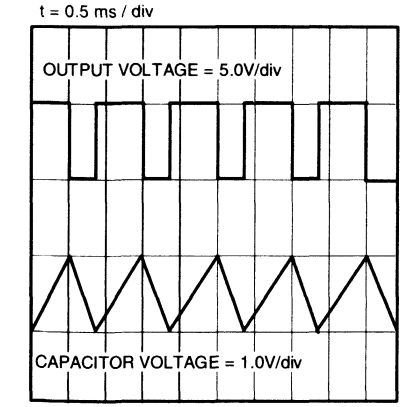
$$f = \frac{1}{T} = \frac{1.44}{(R_1 + 2R_2) C_1}$$

and may be easily found by figure 15.

The duty cycle is given by :

$$D = \frac{R_2}{R_1 + 2R_2}$$

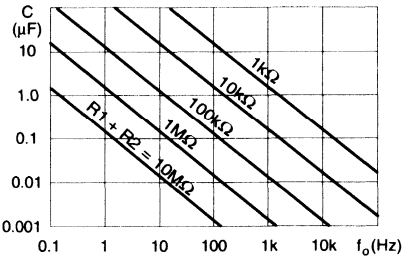
Figure 14



$R1 = R2 = 4.8k\Omega$, $C1 = 0.1\mu F$, $R_L = 1k\Omega$

555-19.EPS

Figure 15 : Free Running Frequency versus R_1, R_2 and C_1



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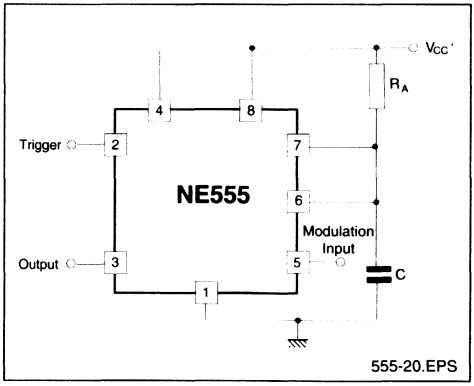
PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. Figure 16 shows the circuit.

Figure 16 : Pulse Width Modulator.



LINEAR RAMP

When the pullup resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is generated. Figure 17 shows a circuit configuration that will perform this function.

Figure 17.

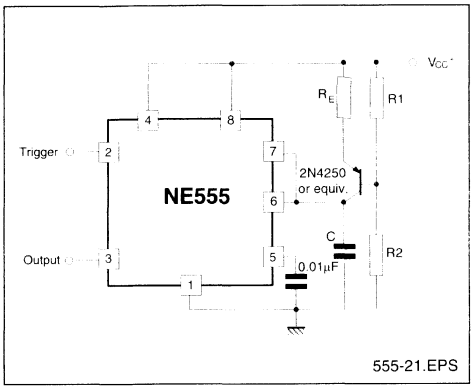
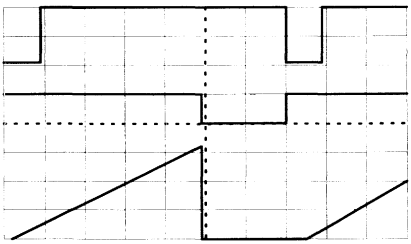


Figure 18 shows waveforms generator by the linear ramp.

The time interval is given by :

$$T = \frac{(2/3\ V_{CC}\ R_E\ (R_{1+}\ R_2)\ C}{R_1\ V_{CC} - V_{BE}\ (R_{1+}\ R_2)} \quad V_{BE} = 0.6V$$

Figure 18 : Linear Ramp.



V_{CC} = 5V
Time = 20µs/DIV
R_1 = 47kΩ
R_2 = 100kΩ
R_E = 2.7kΩ
C = 0.01µF

Top trace : input 3V/DIV
Middle trace : output 5V/DIV
Bottom trace : output 5V/DIV
Bottom trace : capacitor voltage 1V/DIV

50% DUTY CYCLE OSCILLATOR

For a 50% duty cycle the resistors R_A and R_E may be connected as in figure 19. The time preriod for the output high is the same as previous,

$t_1 = 0.693\ R_A\ C$.

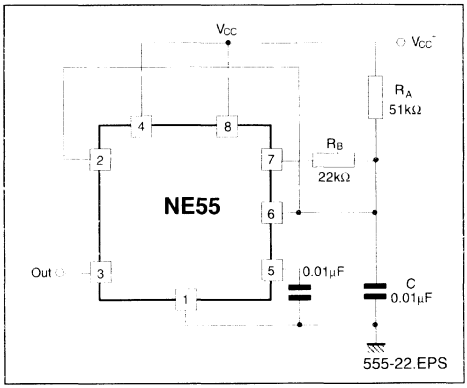
For the output low it is t_2 =

$$[(R_A R_B)/(R_A + R_B)]\ CLn\left[\frac{R_B - 2R_A}{2R_B - R_A}\right]$$

Thus the frequency of oscillation is $f = \frac{1}{t_1 + t_2}$

Note that this circuit will not oscillate if R_B is greater

Figure 19 : 50% Duty Cycle Oscillator.



than 1/2 R_A because the junction of R_A and R_B cannot bring pin 2 down to 1/3 V_{CC} and trigger the lower comparator.

ADDITIONAL INFORMATION

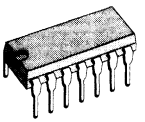
Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1µF in parallel with 1µF electrolytic.

SGS-THOMSON MICROELECTRONICS

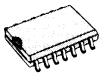
NE556
SA556 - SE556

GENERAL PURPOSE DUAL BIPOLAR TIMERS

- LOW TURN OFF TIME
- MAXIMUM OPERATING FREQUENCY GREATER THAN 500kHz
- TIMING FROM MICROSECONDS TO HOURS
- OPERATES IN BOTH ASTABLE AND MONOSTABLE MODES
- HIGH OUTPUT CURRENT CAN SOURCE OR SINK 200mA
- ADJUSTABLE DUTY CYCLE
- TTL COMPATIBLE
- TEMPERATURE STABILITY OF 0.005% PER °C



N
DIP14
(Plastic Package)
J
CERDIP14
(Cerdip Package)



D
SO14
(Plastic Micropackage)

DESCRIPTION

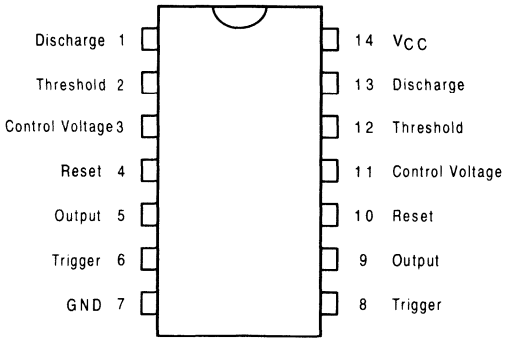
The NE556 dual monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA.

ORDER CODES

Part Number	Temperature Range	Package			
		H	N	J	D
NE556	0°C, 70°C	•	•	•	•
SA556	–40°C, 105°C	•	•	•	•
SE556	–55°C, 125°C	•	•	•	•

556-01.TBL

PIN CONNECTIONS (top view)



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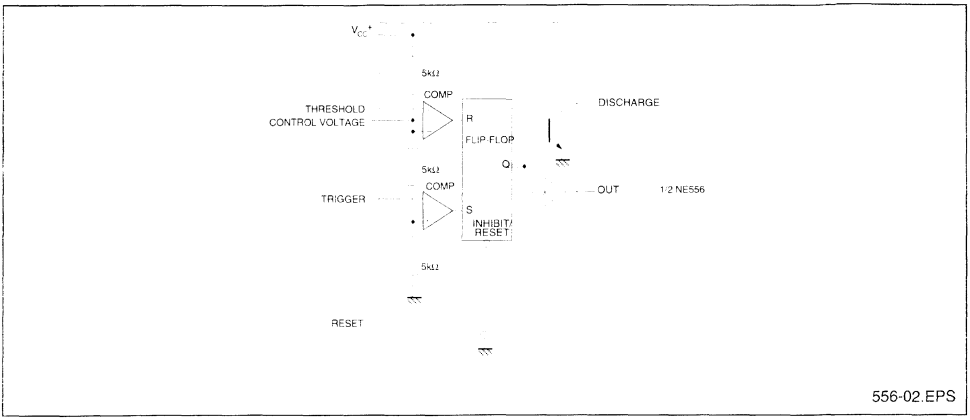
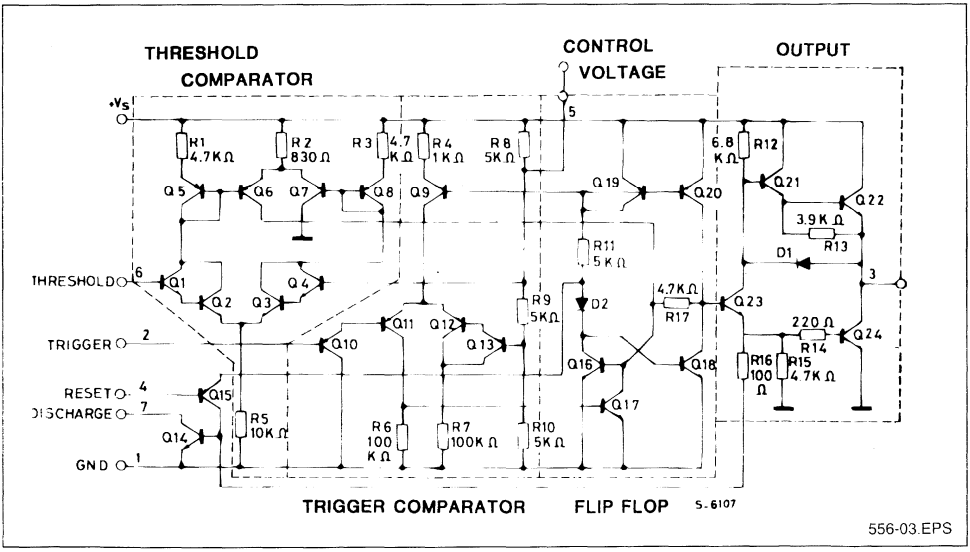
BLOCK DIAGRAM



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{cc}	Supply Voltage	for SE556 for NE556	18 16	V
T_{oper}	Operating Free Air Temperature Range	for NE556 for SA556 for SE556	0 to 70 −40 to 105 −55 to 125	°C
T_j	Junction Temperature		150	°C

OPERATING CONDITIONS

Symbol	Parameter	SE556	NE556 - SA556	Unit
V_{CC}	Supply Voltage	4.5 to 18	4.5 to 16	V
V_{th}, V_{trig}, V_{cl}, V_{reset}	Maximum Input Voltage	V_{CC}	V_{CC}	V

556-03.TBL

ELECTRICAL CHARACTERISTICS

T_{amb} = +25°C, V_{CC} = +5V to +15V (unless otherwise specified)

Symbol	Parameter	SE556			NE556 - SA556			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{CC}	Supply Current (R_L ∞) - (note 1) - (2 timers)							mA
	Low State V_{CC} = +5V		6	10		6	12	
	V_{CC} = +15V		20	24		20	30	
	High State V_{CC} = 5V		4			4		
	Timing Error (monostable)							
	(R_A = 2k to 100kΩ, C = 0.1µF)							
	Initial Accuracy - (note 2)		0.5	2		1	3	%
	Drift with Temperature		30	100		50		ppm/°C
	Drift with Supply Voltage		0.05	0.2		0.1	0.5	%/V
	Timing Error (astable)							
	(R_A, R_B = 1kΩ to 100kΩ, C = 0.1µF,							
	V_{CC} = +15V)							
	Initial Accuracy - (note 2)		1.5			2.25		%
	Drift with Temperature		90			150		ppm/°C
	Drift with Supply Voltage		0.15			0.3		%/V
V_{CL}	Control Voltage level							V
	V_{CC} = +15V	9.6	10	10.4	9	10	11	
	V_{CC} = +5V	2.9	3.33	3.8	2.6	3.33	4	
V_{th}	Threshold Voltage							V
	V_{CC} = +15V	9.4	10	10.6	8.8	10	11.2	
	V_{CC} = +5V	2.7	3.33	4	2.4	3.33	4.2	
I_{th}	Threshold Current - (note 3)		0.1	0.25		0.1	0.25	µA
V_{trig}	Trigger Voltage							V
	V_{CC} = +15V	4.8	5	5.2	4.5	5	5.6	
	V_{CC} = +5V	1.45	1.67	1.9	1.1	1.67	2.2	
I_{trig}	Trigger Current (V_{trig} = 0V)		0.5	0.9		0.5	2.0	µA
V_{reset}	Reset Voltage - (note 4)	0.4	0.7	1	0.4	0.7	1	V
I_{reset}	Reset Current							mA
	V_{reset} = +0.4V		0.1	0.4		0.1	0.4	
	V_{reset} = 0V		0.4	1		0.4	1.5	
V_{OL}	Low Level Output Voltage							V
	V_{CC} = +15V, $I_{O(sink)}$ = 10mA		0.1	0.15		0.1	0.25	
	$I_{O(sink)}$ = 50mA		0.4	0.5		0.4	0.75	
	$I_{O(sink)}$ = 100mA		2	2.2		2	2.5	
	$I_{O(sink)}$ = 200mA		2.5			2.5		
	V_{CC} = +5V, $I_{O(sink)}$ = 8mA		0.1	0.25		0.3	0.4	
	$I_{O(sink)}$ = 5mA		0.05	0.2		0.25	0.35	
V_{OH}	High Level Output Voltage							V
	V_{CC} = +15V, $I_{O(source)}$ = 200mA		12.5			12.5		
	$I_{O(source)}$ = 100mA	13	13.3		12.75	13.3		
	V_{CC} = +5V, $I_{O(source)}$ = 100mA	3	3.3		2.75	3.3		

556-4.TBL

Notes : 1. Supply current when output is high is typically 1mA less.
2. Tested at V_{CC} = +5V and V_{CC} = +15V.
3. This will determine the maximum value of R_A + R_B for +15V operation the max total is R = 20MΩ and for 5V operation, the max total R = 3.5MΩ.
4. Specified with trigger input high.

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	SE556			NE556 - SA556			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
$I_{dis(off)}$	Discharge Pin Leakage Current (output high) (V_{dis} = 10V)		20	100		20	100	nA
$V_{dis(sat)}$	Discharge pin Saturation Voltage (output low) - (note 5)							mV
	V_{CC} = +15V, I_{dis} = 15mA		180	480		180	480	
	V_{CC} = +5V, I_{dis} = 4.5mA		80	200		80	200	
t_r	Output Rise Time		100	200		100	300	ns
t_f	Output Fall Time		100	200		100	300	
t_{off}	Turn off Time - (note 6) (V_{reset} = V_{CC})		0.5			0.5		µs

556-05.TBL

Notes : 5. No protection against excessive Pin 7 current is necessary, providing the package dissipation rating will not be exceeded.
6. Time mesaured from a positive going input pulse from 0 to 0.8x V_{CC} into the threshold to the drop from high to low of the output trigger is tied to treshold.

Figure 1 : Minimum Pulse Width Required for Trigering

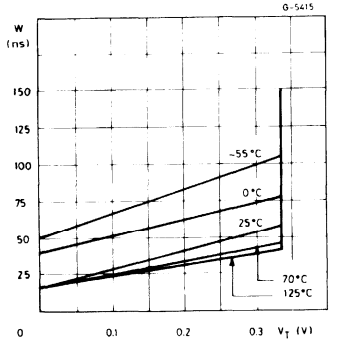


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Figure 2 : Supply Current versus Supply Voltage

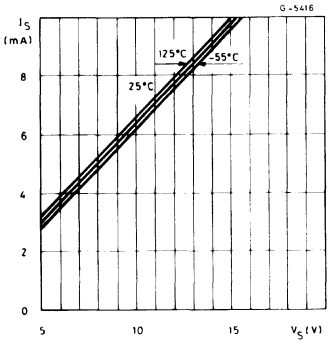

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Figure 3 : Delay Time versus Temperature

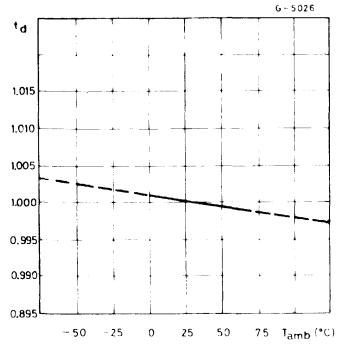

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Figure 4 : Low Output Voltage versus Output Sink Current

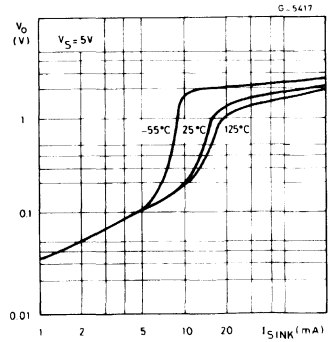

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Figure 5 : Low Output Voltage versus Output Sink Current

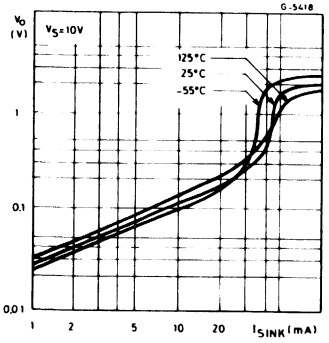

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Figure 6 : Low Output Voltage versus Output Sink Current

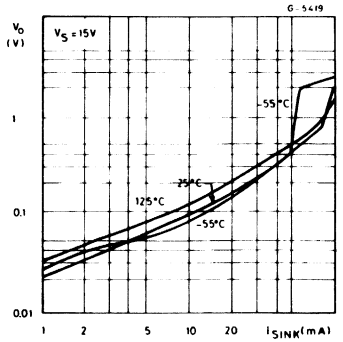

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Figure 7 : High Output Voltage Drop versus Output

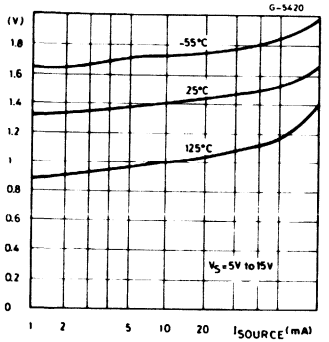

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Figure 8 : Delay Time versus Supply Voltage

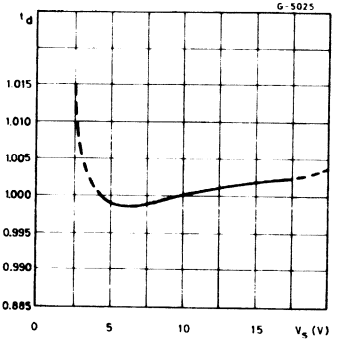

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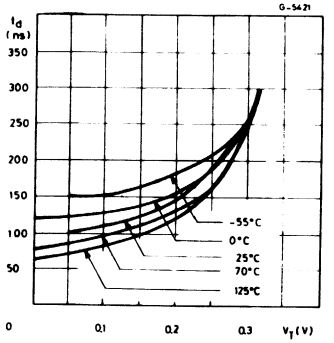
Figure 9 : Propagation Delay versus Voltage Level of Trigger Value



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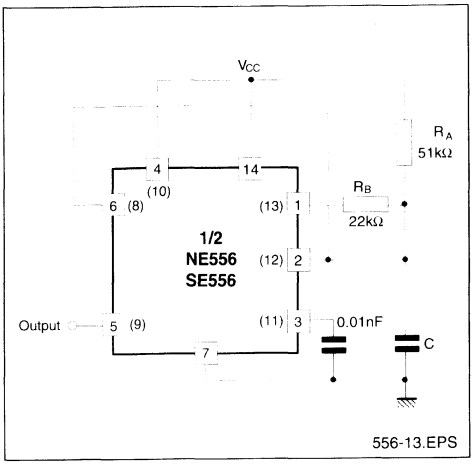
TYPICAL APPLICATION

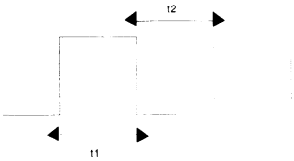
50 % DUTY CYCLE OSCILLATOR



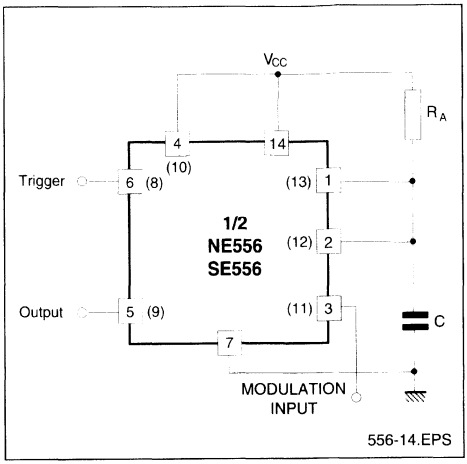
$t_1 = 0.693\ R_A.C$

$t_2 = [(R_A R_B)/(R_A + R_B)]\ CLn\left[\frac{R_B - 2R_A}{2R_B - R_A}\right]$

$f = \frac{1}{t_1 + t_2} \quad R_B < \frac{1}{2}\ R_A\ ti$

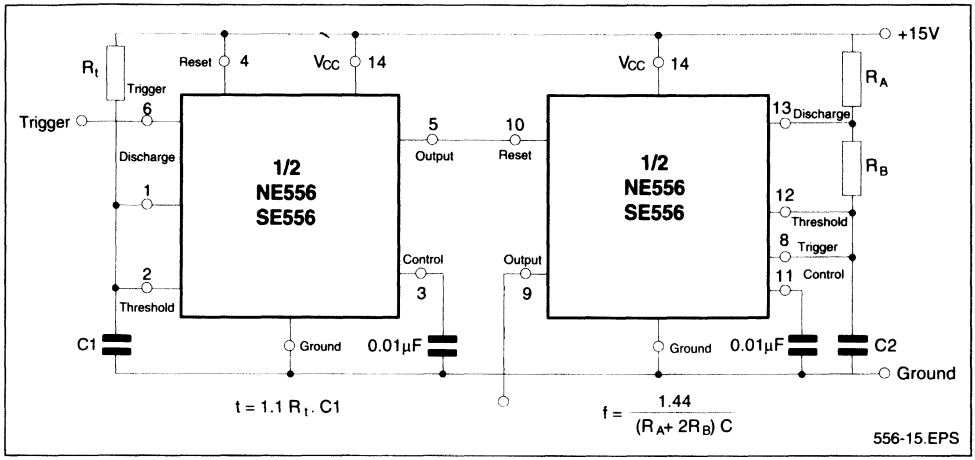


PULSE WIDTH MODULATOR

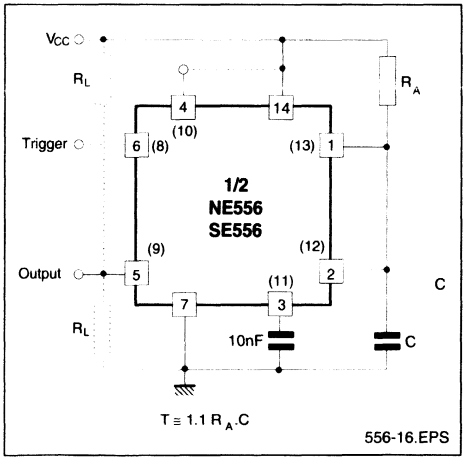


TONE BURST GENERATOR

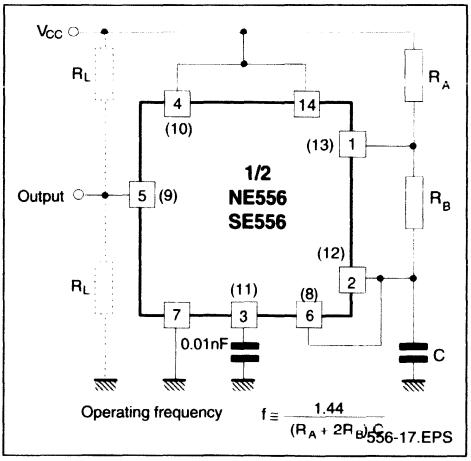
For a tone burst generator the first timer is used as a monostable and determines the tone duration when triggered by a positive pulse at pin 6. The second timer is enabled by the high output of the monostable. It is connected as an astable and determines the frequency of the tone.



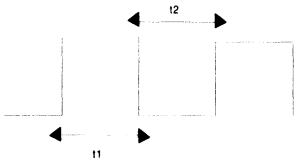
MONOSTABLE OPERATION



ASTABLE OPERATION



$t_1 = 0.693\ (R_A + R_B)\ C$ Output High
$t_2 = 0.693\ R_B C$ Output low

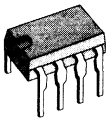


SGS-THOMSON MICROELECTRONICS

OP07C

VERY LOW OFFSET SINGLE BIPOLAR OPERATIONAL AMPLIFIERS

- EXTREMELY LOW OFFSET : 150µV MAX
- LOW INPUT BIAS CURRENT : 1.8nA
- LOW V_{io} DRIFT : 0.5µV/°C
- WIDE SUPPLY VOLTAGE RANGE : ± 3V to ± 22V



N
DIP8
(Plastic Package)

DESCRIPTION

The OP07C is a very high precision op amp with an offset voltage maximum of 150µV.

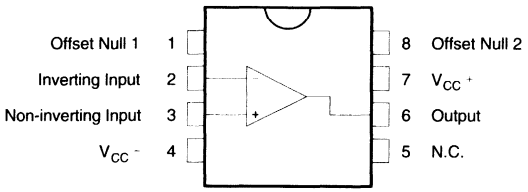
Offering also low input current (1.8nA) and high gain (400V/mV), the OP07C is particularly suitable for instrumentation applications.

ORDER CODES

Part Number	Temperature Range	Package
		N
OP07C	-40°C, +105°C	•

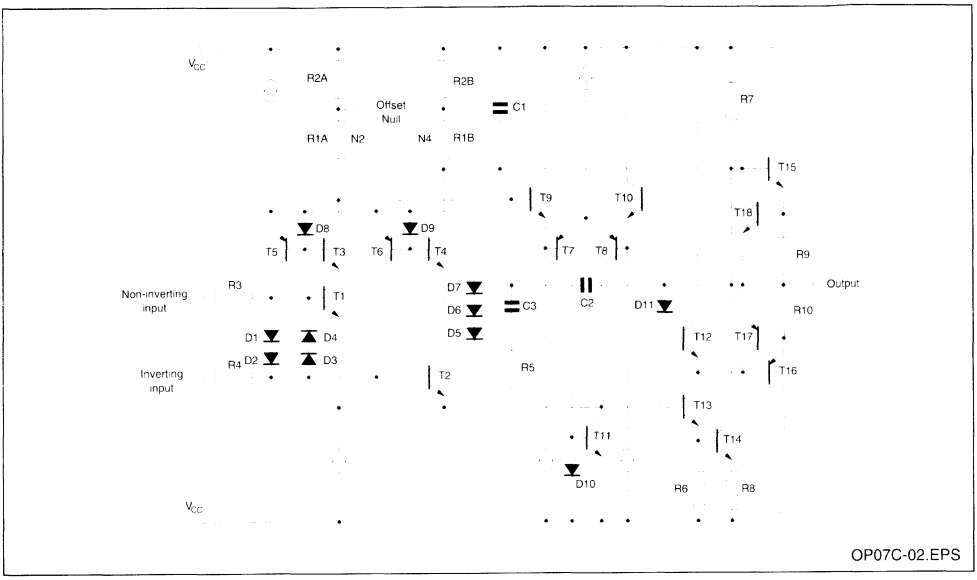
OP07C-01.TBL

PIN CONNECTIONS (top view)

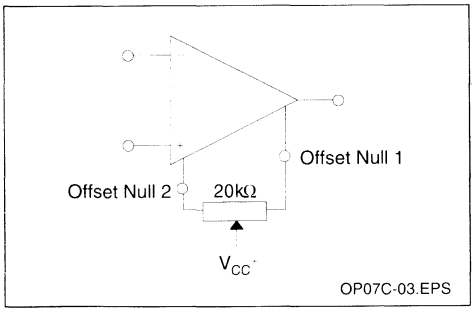


OP07C-01.EPS

SCHEMATIC DIAGRAM



INPUT OFFSET VOLTAGE NULLING CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	±22	V
V_{id}	Differential Input Voltage	±30	V
V_i	Input Voltage	±22	V
T_{oper}	Operating Temperature	-40 to +105	°C
T_{stg}	Storage Temperature	-65 to +150	°C

OP07C-02.TBL

ELECTRICAL CHARACTERISTICS

V_{CC} = ±15V, T_{amb} = +25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage 0°C ≤ T_{amb} ≤ +70°C		60	150 250	µV
	Long Term Input Offset Voltage Stability - (note 1)		0.4	2	µV/Mo
DV_{io}	Input Offset Voltage Drift		0.5	1.8	µV/°C
I_{io}	Input Offset Current 0°C ≤ T_{amb} ≤ +70°C		0.8	6 8	nA
DI_{io}	Input Offset Current Drift		15	50	pA/°C
I_{ib}	Input Bias Current 0°C ≤ T_{amb} ≤ +70°C		1.8	7 9	nA
DI_{ib}	Input Bias Current Drift		15	50	pA/°C
R_o	Open Loop Output Resistance		60		Ω
R_{id}	Differential Input Resistance		33		MΩ
R_{ic}	Common Mode Input Resistance		120		GΩ
V_{icm}	Input Common Mode Voltage Range 0°C ≤ T_{amb} ≤ +70°C	±13 ±13	±13.5		V
CMR	Common Mode Rejection Ratio (V_i = V_{icm} min) 0°C ≤ T_{amb} ≤ +70°C	 100 97	 120		dB
SVR	Supply Voltage Rejection Ratio (V_{CC} = ±3 to ±18V) 0°C ≤ T_{amb} ≤ +70°C	 90 86	 104		dB
A_{vd}	Large Signal Voltage Gain V_{CC} = ±15, R_L = 2kΩ, V_O = ±10V, 0°C ≤ T_{amb} ≤ +105°C V_{CC} = ±3V, R_L = 500Ω, V_O = ±0.5V	 120 100 100	 400 400		V/mV
V_{opp}	Output Voltage Swing R_L = 10kΩ R_L = 2kΩ R_L = 1kΩ 0°C ≤ T_{amb} ≤ +70°C R_L = 2kΩ	 ±12 ±11.5 ±11	 ±13 ±12.8 ±12 		V
SR	Slew Rate (R_L = 2kΩ, C_L = 100pF)		0.17		V/µS
GBP	Gain Bandwidth Product (R_L = 2kΩ, C_L = 100pF, f = 100kHz)		 0.5		MHz
I_{CC}	Supply Current - (no load) 0°C ≤ T_{amb} ≤ +70°C V_{CC} = ±3V		2.7 0.67	5 6 1.3	mA
e_n	Equivalent Input Noise Voltage f = 10Hz f = 100Hz f = 1kHz		 11 10.5 10	 20 13.5 11.5	$\frac{nV}{\sqrt{Hz}}$
i_n	Equivalent Input Noise Current f = 10Hz f = 100Hz f = 1kHz		 0.3 0.2 0.1	 0.9 0.3 0.2	$\frac{pA}{\sqrt{Hz}}$

OP07C-03.TBL

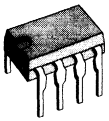
Note 1 : 1. Long Term Input Offset Voltage Stability refers to the average trend line of V_{io} vs time over extended periods after the first 30 days of operation.

SGS-THOMSON MICROELECTRONICS

OP07D

VERY LOW OFFSET SINGLE BIPOLAR OPERATIONAL AMPLIFIERS

- EXTREMELY LOW OFFSET : 150µV MAX
- LOW INPUT BIAS CURRENT : 1.8nA
- LOW V_{io} DRIFT : 0.5µV/°C
- WIDE SUPPLY VOLTAGE RANGE : ± 3V to ± 22V



N
DIP8
(Plastic Package)

DESCRIPTION

The OP07D is a very high precision op amp with an offset voltage maximum of 150µV.

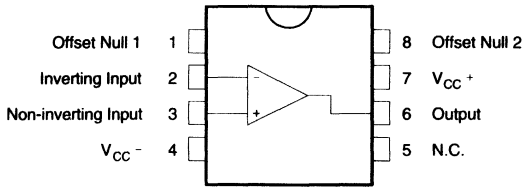
Offering also low input current (1.8nA) and high gain (400V/mV), the OP07D is particularly suitable for instrumentation applications.

ORDER CODES

Part Number	Temperature Range	Package
		N
OP07D	-40°C, +105°C	•

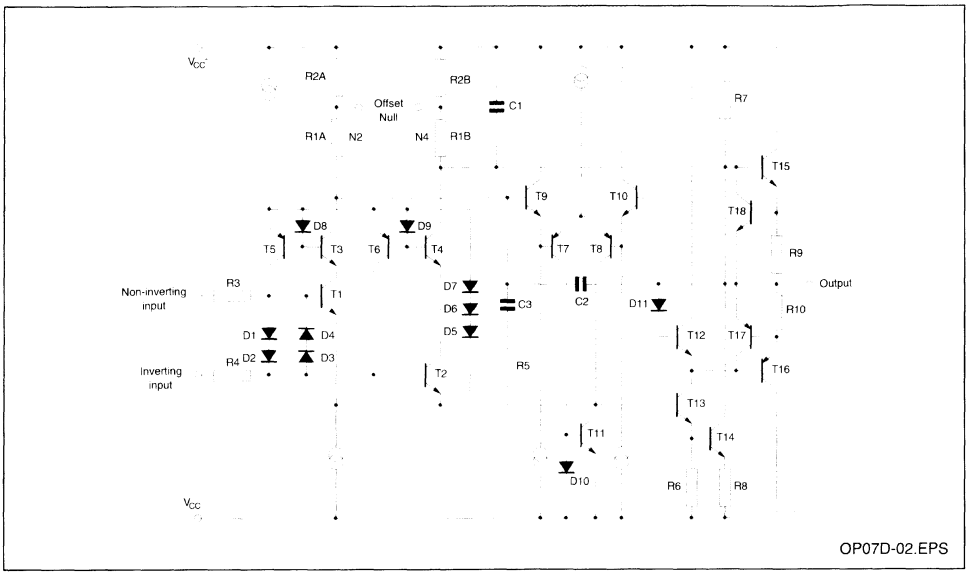
OP07D-01.TBL

PIN CONNECTIONS (top view)

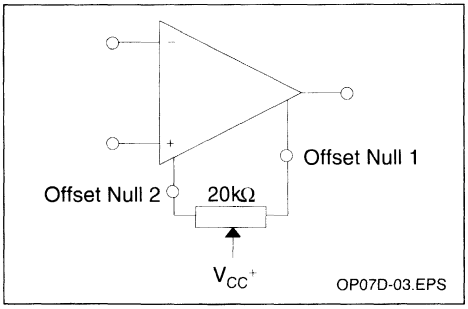


OP07D-01.EPS

SCHEMATIC DIAGRAM



INPUT OFFSET VOLTAGE NULLING CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	±22	V
V_{id}	Differential Input Voltage	±30	V
V_i	Input Voltage	±22	V
T_{oper}	Operating Temperature	-40 to +105	°C
T_{stg}	Storage Temperature	-65 to +150	°C

OP07D-02.TBL

ELECTRICAL CHARACTERISTICS

V_{CC} = ±15V, T_{amb} = +25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage $0°C \le T_{amb} \le +70°C$		60	150 250	µV
	Long Term Input Offset Voltage Stability - (note 1)		0.4	3	µV/Mo
DV_{io}	Input Offset Voltage Drift		0.5	2.5	µV/°C
I_{io}	Input Offset Current $0°C \le T_{amb} \le +70°C$		0.8	6 8	nA
DI_{io}	Input Offset Current Drift		15	50	pA/°C
I_{ib}	Input Bias Current $0°C \le T_{amb} \le +70°C$		1.8	12 14	nA
DI_{ib}	Input Bias Current Drift		15	50	pA/°C
R_o	Open Loop Output Resistance		60		Ω
R_{id}	Differential Input Resistance		33		MΩ
R_{ic}	Common Mode Input Resistance		120		GΩ
V_{icm}	Input Common Mode Voltage Range $0°C \le T_{amb} \le +70°C$	±13 ±13	±13.5		V
CMR	Common Mode Rejection Ratio ($V_i = V_{icm}$ min) $0°C \le T_{amb} \le +70°C$	94 94	120		dB
SVR	Supply Voltage Rejection Ratio (V_{CC} = ±3 to ±18V) $0°C \le T_{amb} \le +70°C$	90 86	104		dB
A_{vd}	Large Signal Voltage Gain V_{CC} = ±15V, R_L = 2kΩ, V_O = ±10V $0°C \le T_{amb} \le +70°C$ V_{CC} = ±3V, R_L = 500Ω, V_O = ±0.5V	120 100	400 400		V/mV
V_{opp}	Output Voltage Swing R_L = 10kΩ R_L = 2kΩ R_L = 1kΩ $0°C \le T_{amb} \le +70°C$ R_L = 2kΩ	±12 ±11.5 ±11	±13 ±12.8 ±12		V
SR	Slew Rate (R_L = 2kΩ, C_L = 100pF)		0.17		V/µS
GBP	Gain Bandwidth Product (R_L = 2kΩ, C_L = 100pF, f = 100kHz)		0.5		MHz
I_{CC}	Supply Current - (no load) $0°C \le T_{amb} \le +70°C$ V_{CC} = ±3V		2.7 0.67	5 6 1.3	mA
e_n	Equivalent Input Noise Voltage f = 10Hz f = 100Hz f = 1kHz		11 10.5 10	20 13.5 11.5	$\frac{nV}{\sqrt{Hz}}$
i_n	Equivalent Input Noise Current f = 10Hz f = 100Hz f = 1kHz		0.3 0.2 0.1	0.9 0.3 0.2	$\frac{pA}{\sqrt{Hz}}$

OP07D-03.TBL

Note 1 : 1. Long Term Input Offset Voltage Stability refers to the average trend line of V_{io} vs time over extended periods after the first 30 days of operation.

PBL3717A

STEPPER MOTOR DRIVER

- FULL STEP - HALF STEP - QUARTER STEP OPERATING MODE
- BIPOLAR OUTPUT CURRENT UP TO 1 A
- FROM 10 V UP TO 46 V MOTOR SUPPLY VOLTAGE
- LOW SATURATION VOLTAGE WITH INTEGRATED BOOTSTRAP
- BUILT IN FAST PROTECTION DIODES
- EXTERNALLY SELECTABLE CURRENT LEVEL
- OUTPUT CURRENT LEVEL DIGITALLY OR ANALOGUE CONTROLLED
- THERMAL PROTECTION WITH SOFT INTERVENTION

DESCRIPTION

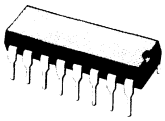
The PBL3717A is a monolithic IC which controls and drives one phase of a bipolar stepper motor with chopper control of the phase current. Current levels may be selected in three steps by means of two logic inputs which select one of three current comparators. When both of these inputs are high the device is disabled. A separate logic input controls the direction of current flow.

A monostable, programmed by an external RC network, sets the current decay time.

The power section is a full H-bridge driver with four internal clamp diodes for current recirculation. An external connection to the lower emitters is available for the insertion of a sensing resistor. Two PBL3717As and few external components form a complete stepper motor drive subsystem.

The raccomended operating ambient temperature ranges is from 0 to 70 °C.

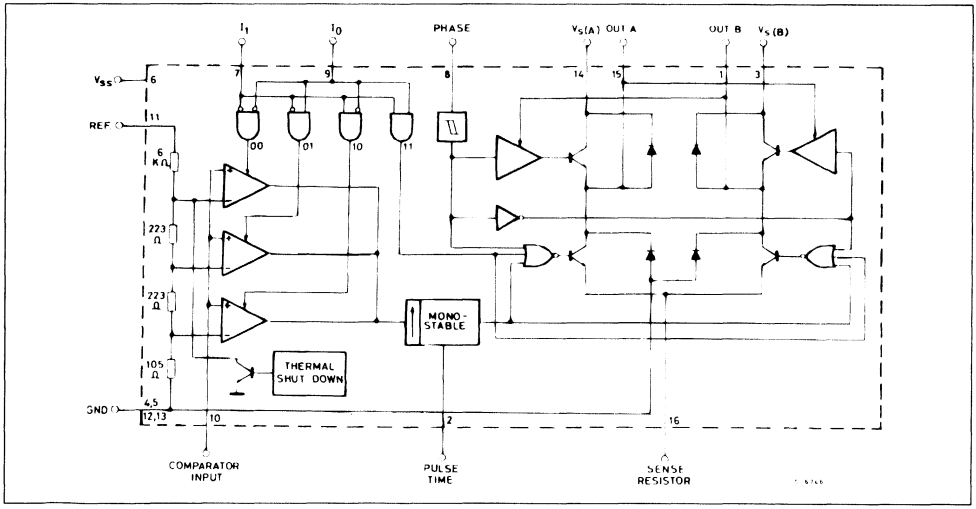
The PBL3717A is supplied in a 12 + 2 + 2 lead Powerdip package.



Powerdip
12 + 2 + 2

ORDER CODE : PBL3717A

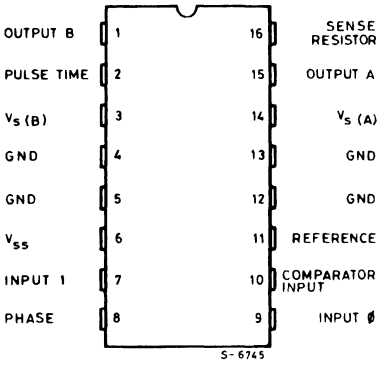
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Power Supply Voltage (pins 14, 3)	50	V
V_{ss}	Logic Supply Voltage (pin 6)	7	V
V_i	Logic Input Voltage (pins 7, 8, 9)	6	V
V_c	Comparator Input (pin 10)	V_{ss}	
V_r	Reference Input Voltage (pin 11)	15	V
I_o	Output Current (DC operation)	1.2	A
T_{stg}	Storage Temperature	– 55 to + 150	°C
T_j	Operating Junction Temperature	150	°C

CONNECTION DIAGRAM (top view)



TRUTH TABLE

Input 0 (pin 9)	Input 1 (pin 7)	
H	H	No Current
L	H	Low Current
H	L	Medium Current
L	L	High Current

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-pins	11	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient*	40	°C/W

* Soldered on a 35µ thick 20 cm^2 P.C. board copper area.

PIN FUNCTIONS

N	Name	Function
1	OUTPUT B	Output Connection (with pin 15). The output stage is a "H" bridge formed by four transistors and four diodes suitable for switching applications.
2	PULSE TIME	A parallel RC network connected to this pin sets the OFF time of the lower power transistors. The pulse generator is a monostable triggered by the rising edge of the output of the comparators ($t_{off} = 0.69\ R_T\ C_T$).
3	SUPPLY VOLTAGE B	Supply Voltage Input for Half Output Stage. See also pin 14.
4	GROUND	Ground Connection. With pins 5, 12 and 13 also conducts heat from die to printed circuit copper.
5	GROUND	See pin 4.
6	LOGIC SUPPLY	Supply Voltage Input for Logic Circuitry.
7	INPUT 1	This pin and pin 9 (INPUT 0) are logic inputs which select the outputs of the three comparators to set the current level. Current also depends on the sensing resistor and reference voltage. See truth table.
8	PHASE	This TTL-compatible logic input sets the direction of current flow through the load. A high level causes current to flow from OUTPUT A (source) to OUTPUT B (sink). A schmitt trigger on this input provides good noise immunity and a delay circuit prevents output stage short circuits during switching.
9	INPUT 0	See INPUT 1 (pin 7) .
10	COMPARATOR INPUT	Input connected to the three comparators. The voltage across the sense resistor is feedback to this input through the low pass filter $R_C\ C_C$. The lower power transistor are disabled when the sense voltage exceeds the reference voltage of the selected comparator. When this occurs the current decays for a time set by $R_T\ C_T$. $t_{off} = 0.69\ R_T\ C_T$.
11	REFERENCE	A voltage applied to this pin sets the reference voltage of the three comparators, this determining the output current (also thus depending on R_S and the two inputs INPUT 0 and INPUT 1).
12	GROUND	See pin 4.
13	GROUND	See pin 4.
14	SUPPLY VOLTAGE A	Supply Voltage Input for Half Output Stage. See also pin 13.
15	OUTPUT A	See pin 1.
16	SENSE RESISTOR	Connection to Lower Emitters of Output Stage for Insertion of Current Sense Resistor.

Figure 1 : Test and Application Circuit.

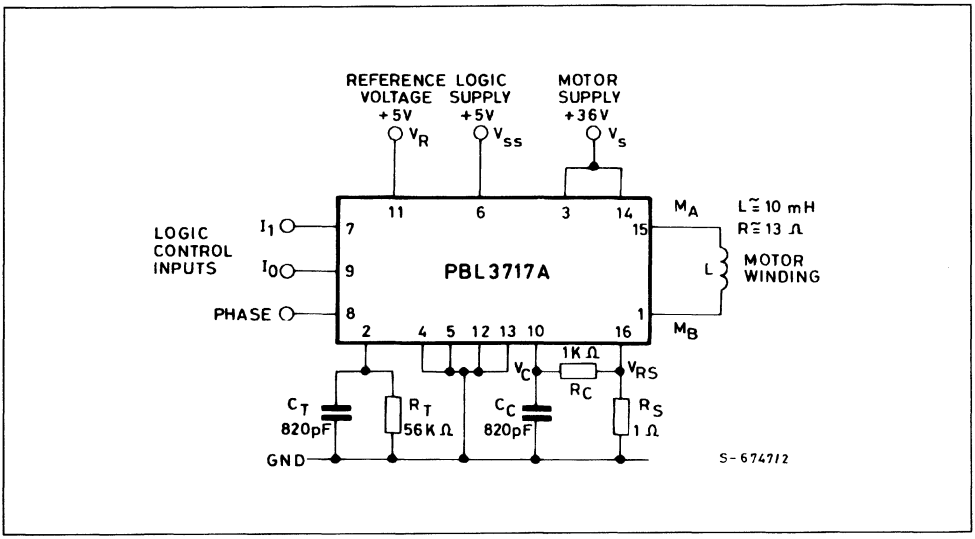
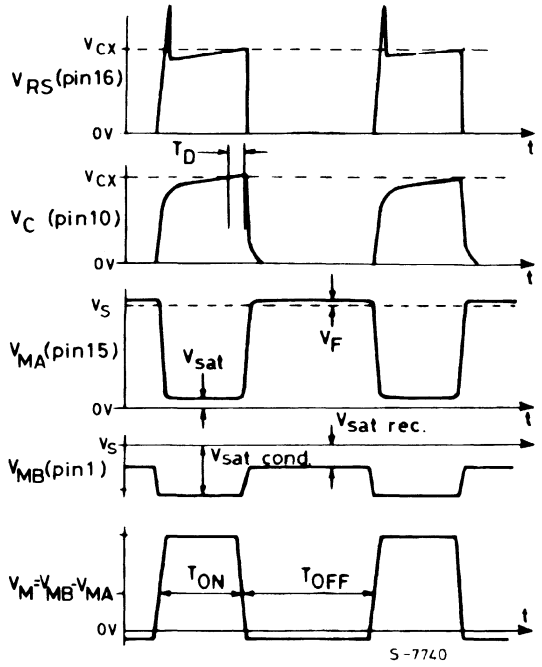


Figure 2 : Waveforms with MA Regulating (phase = 0).



ELECTRICAL CHARACTERISTICS (refer to the test circuit V_s = 36 V, V_{ss} = 5 V, Tamb = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
V_s	Supply Voltage (pin 3, 14)			10		46	V
V_{ss}	Logic Supply Voltage (pin 6)			4.75		5.25	V
I_{ss}	Logic Supply Current (pin 6)				7	15	mA
I_R	Reference Input Current (pin 11)	V_R = 5 V			0.75	1	mA

LOGIC INPUTS

V_{iL}	Input Low Voltage (pins 7, 8, 9)					0.8	V
V_{iH}	Input High Voltage (pin 7, 8, 9)			2		V_{ss}	V
I_{iL}	Low Voltage Input Current (pins 7, 8, 9)	V_i = 0.4 V	pin 8			− 100	µA
			pins 7, 9			− 400	µA
I_{iH}	High Voltage Input Current (pins 7, 8, 9)	V_i = 2.4 V				10	µA

COMPARATORS

V_{CL}	Comparator Low Threshold Voltage (pin 10)	V_R = 5 V	I_o = L I_1 = H	66	78	90	mV
V_{CM}	Comparator Medium Threshold Voltage (pin 10)	V_R = 5 V	I_o = H I_1 = L	236	251	266	mV
V_{CH}	Comparator High Threshold Voltage (pin 10)	V_R = 5 V	I_o = L I_1 = L	396	416	436	mV
I_C	Comparator Input Current (pin 10)					± 20	µA
t_{off}	Cutoff Time	R_T = 56 KΩ	C_T = 820 pF	25		35	µs
t_d	Turn Off Delay	(see fig. 2)				2	µs
I_{off}	Output Leakage Current (pins 1, 15)	I_o = H	I_1 = H			100	µA

SOURCE DIODE-TRANSISTOR PAIR

V_{sat}	Saturation Voltage (pins 1, 15)	I_M = − 0.5 A (see fig. 2)	Conduction Period		1.7	2.1	V
			Recirculation Period		1.1	1.35	
V_{sat}	Saturation Voltage (pins 1, 15)	I_M = − 1 A (see fig. 2)	Conduction Period		2.1	2.8	V
			Recirculation Period		1.7	2.5	
I_{LK}	Leakage Current	V_s = 46 V				300	µA
V_F	Diode Forward Voltage	I_M = − 0.5 A			1	1.25	V
		I_M = − 1 A			1.3	1.7	
I_{SLK}	Substrate Leakage Current when Clamped	I_M = − 0.5 A				2	mA
		I_M = − 1A				5	

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SINK DIODE-TRANSISTOR PAIR						
V_{sat}	Saturation Voltage (pins 1, 15)	I_M = 0.5 A		1.1	1.35	V
		I_M = 1 A		1.6	2.3	V
I_{LK}	Leakage Current	V_s = 46 V			300	µA
V_F	Diode Forward Voltage	I_M = 0.5 A		1.1	1.5	V
		I_M = 1 A		1.4	2	

APPLICATION CIRCUIT

Figure 3 : Two Phase Bipolar Stepper Motor Driver.

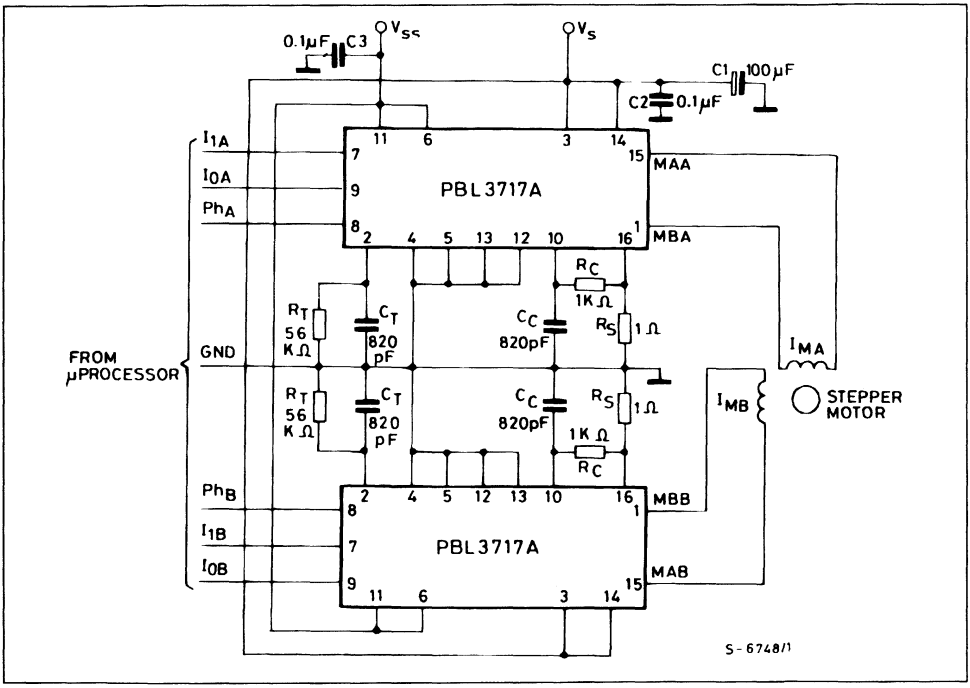


Figure 4 : P.C. Board and Component Layout of the Circuit of fig. 3 (1 : 1 scale).

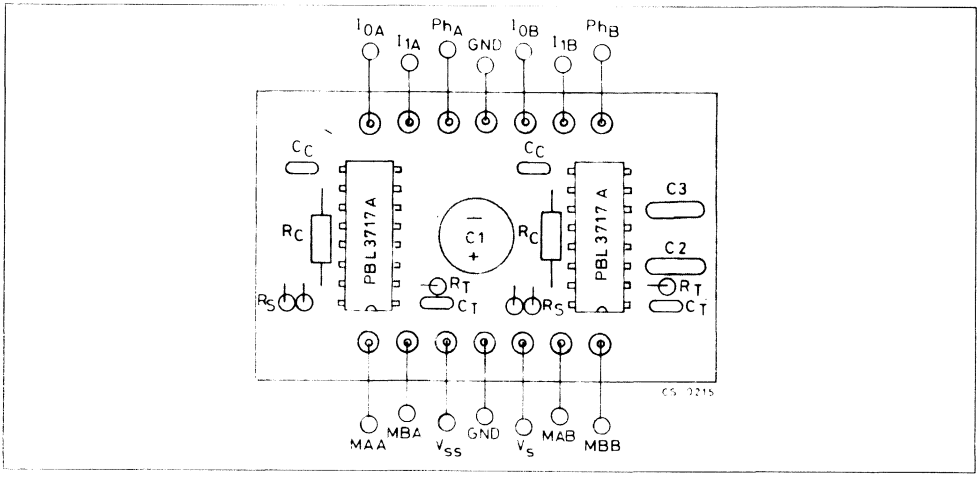
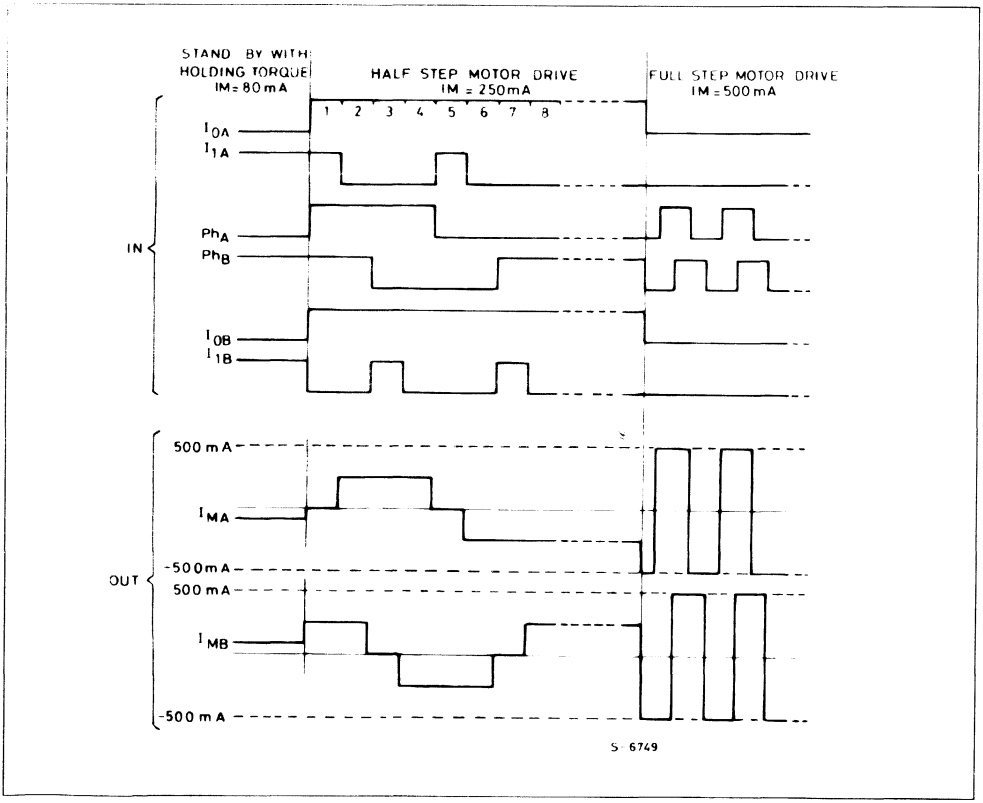


Figure 5 : Input and Output Sequences for Half Step and Full Step Operation.



APPLICATION INFORMATIONS

Fig. 3 shows a typical application in which two PBL3717A control a two phase bipolar stepper motor.

PROGRAMMING

The logic inputs I_0 and I_1 set at three different levels the amplitude of the current flowing in the motor winding according to the truth table of page 2. A high level on the "PHASE" logic input sets the direction of that current from output A to output B ; a low level from output B to output A.

It is recommended that unused inputs are tied to pin 6 (V_{SS}) or pin 4 (GND) as appropriate to avoid noise problem.

The current levels can be varied continuously by changing the ref. voltage on pin 11.

CONTROL OF THE MOTOR

The stepper motor can rotate in either directions according to the sequence of the input signals. It is possible to obtain a full step, a half step and a quarter step operation.

FULL STEP OPERATION

Both the windings of the stepper motor are energized all the time with the same current $I_{MA} = I_{MB}$.

I_0 and I_1 remain fixed at whatever torque value is required.

Calling A the condition with winding A energized in one direction and $\overline{A}$ in the other direction, the sequence for full step rotation is :

$$AB \rightarrow \overline{A}B \rightarrow \overline{A}\,\overline{B} \rightarrow A\overline{B} \text{ etc.}$$

For the rotation in the other direction the sequence must be reserved.

In the full step operation the torque is constant each step.

HALF STEP OPERATION

Power is applied alternately to one winding then both according to the sequence :

$AB \rightarrow B \rightarrow \overline{A}B \rightarrow \overline{A} \rightarrow \overline{A}\,\overline{B} \rightarrow \overline{B} \rightarrow A\overline{B} \rightarrow A$ etc.

Like full step this can be done at any current level ; the torque is not constant but it is lower when only one winding is energized.

A coil is turned off by setting I_0 and I_1 both high.

QUARTER STEP OPERATION

It is preferable to realize the quarter step operation at full power otherwise the steps will be of very irregular size.

The extra quarter steps are added to the half steps sequence by putting one coil on half current according to the sequence.

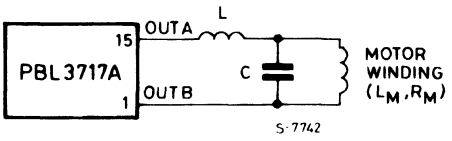
$$AB \rightarrow \frac{A}{2}B \rightarrow B \rightarrow \frac{\overline{A}}{2}B \rightarrow \overline{A}B \rightarrow \overline{A}\frac{B}{2} \rightarrow \overline{A} \text{ etc.}$$

MOTOR SELECTION

As the PBL3717A provides constant current drive, with a switching operation, care must be taken to select stepper motors with low hysteresis losses to prevent motor over heat.

L -C FILTER

To reduce EMI and chopping losses in the motor a low pass L -C filter can be inserted across the outputs of the PBL3717A as shown on the following picture.



$$L \cong \frac{1}{10} LM \qquad C \cong \frac{4 \cdot 10^{-10}}{L}$$

Figure 6 : Source sat. Voltage vs. Output Current (recirc. period).

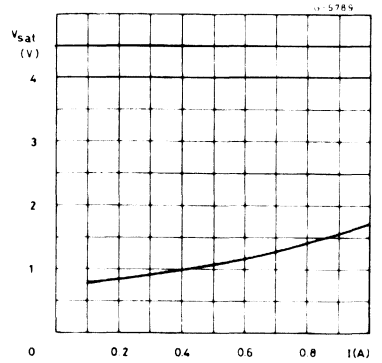


Figure 7 : Source sat. Voltage vs. Output Current (conduction period).

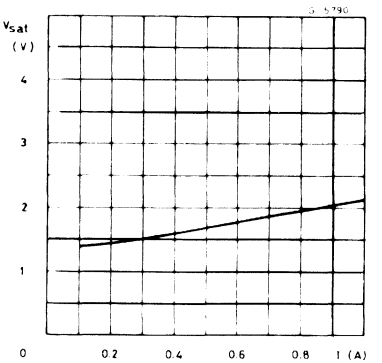


Figure 8 : Sink sat. Voltage vs. Output Current.

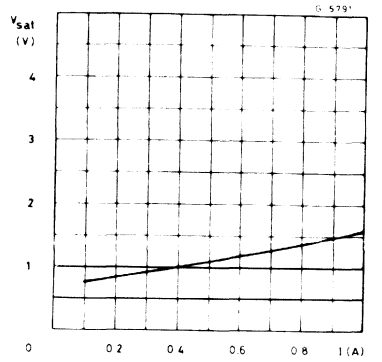
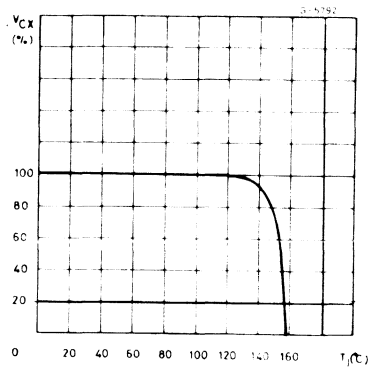


Figure 9 : Comparator threshold vs. Junction Temperature.



MOUNTING INSTRUCTIONS

The $R_{th\ j\text{-}amb}$ of the PBL 3717A can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board or to an external heatsink.

The diagram of fig. 11 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side "α" of two equal square copper areas having a thichkness of 35µ (see fig. 10).

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 10 : Example of P.C. Board Copper Area Which is Used as Heatsink.

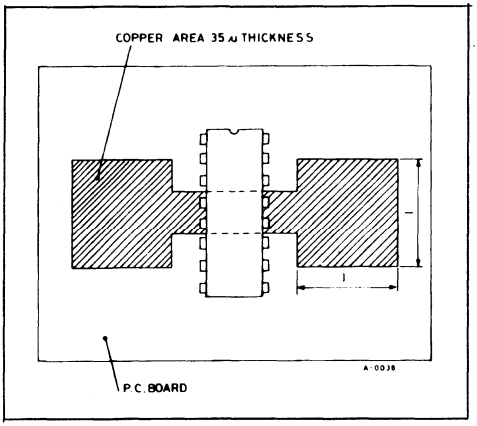
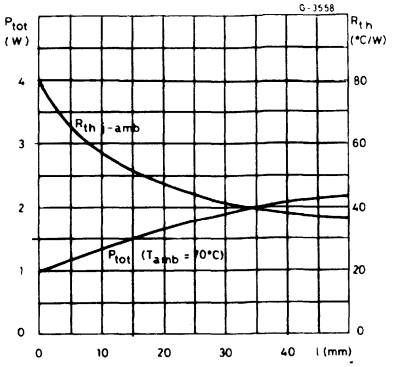


Figure 11 : Max. Dissipable Power and Junction to Ambient Thermal Resistance vs. size "α".



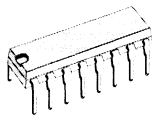
SGS-THOMSON MICROELECTRONICS

SG2524
SG3524

REGULATING PULSE WIDTH MODULATORS

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST/1)

- COMPLETE PWM POWER CONTROL CIRCUITRY
- UNCOMMITTED OUTPUTS FOR SINGLE-ENDED OR PUSH PULL APPLICATIONS
- LOW STANDBY CURRENT 8mA TYPICAL
- OPERATION UP TO 300KHz
- 1% MAXIMUM TEMPERATURE VARIATION OF REFERENCE VOLTAGE



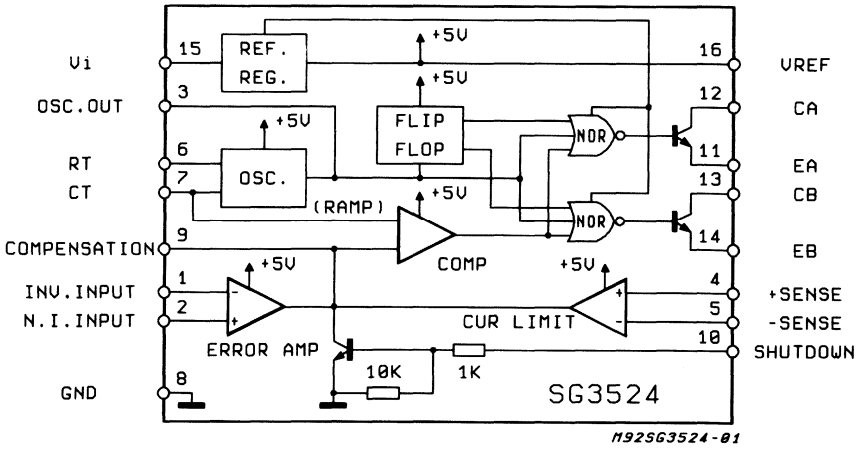
DIP16 SO16

ORDERING NUMBERS: SG2524N (DIP16)
SG3524N (DIP16)
SG2524P (SO16)
SG3524P (SO16)

DESCRIPTION

The SG2524, and SG3524 incorporate on a single monolithic chip all the function required for the construction of regulating power suppies inverters or switching regulators. They can also be used as the control element for high power-output applications. The SG3524 family was designed for switching regulators of either polarity, transformer-coupled dc-to-dc converters, transformerless voltage doublers and polarity converter applications employing fixed-frequency, pulse-width modulation techniques. The dual alternating outputs allows either single-ended or push-pull applications. Each device includes an on-ship reference, error amplifier, programmable oscillator, pulse-steering flip flop, two uncommitted output transistors, a high-gain comparator, and current-limiting and shut-down circuitry.

BLOCK DIAGRAM



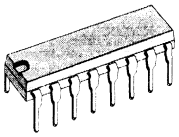
SGS-THOMSON MICROELECTRONICS

SG2525A/2527A SG3525A/3527A

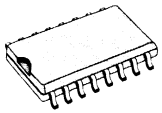
REGULATING PULSE WIDTH MODULATORS

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST/1)

- 8 TO 35 V OPERATION
- 5.1 V REFERENCE TRIMMED TO ± 1 %
- 100 Hz TO 500 KHz OSCILLATOR RANGE
- SEPARATE OSCILLATOR SYNC TERMINAL
- ADJUSTABLE DEADTIME CONTROL
- INTERNAL SOFT-START
- PULSE-BY-PULSE SHUTDOWN
- INPUT UNDERVOLTAGE LOCKOUT WITH HYSTERESIS
- LATCHING PWM TO PREVENT MULTIPLE PULSES
- DUAL SOURCE/SINK OUTPUT DRIVERS



DIP16

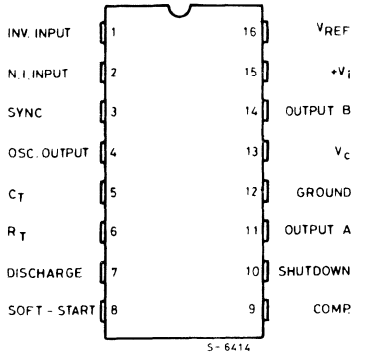


SO16

DESCRIPTION

The SG3525A/3527A series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used in designing all types of switching power supplies. The on-chip + 5.1 V reference is trimmed to ± 1 % and the input common-mode range of the error amplifier includes the reference voltage eliminating external resistors. A sync input to the oscillator allows multiple units to be slaved or a single unit to be synchronized to an external system clock. A single resistor between the C_T and the discharge terminals provide a wide range of dead time adjustment. These devices also feature built-in soft-start circuitry with only an external timing capacitor required. A shutdown terminal controls both the soft-start circuity and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands. These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for sub-normal input voltages. This lockout circuitry includes approximately 500 mV of hysteresis for jitter-free operation. Another feature of these PWM circuits is a latch following the comparator. Once a PWM pulses has been terminated for any reason, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking in excess of 200 mA. The SG3525A output stage features NOR logic, giving a LOW output for an OFF state. The SG3527A utilizes OR logic which results in a HIGH output level when OFF.

PIN CONNECTIONS AND ORDERING NUMBERS (top view)

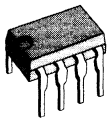


Type	Plastic DIP	SO16
SG2525A	SG2525AN	SG2525AP
SG2527A	SG2527AN	SG2527AP
SG3525A	SG3525AN	SG3525AP
SG3527A	SG3527AN	SG3527AP

SGS-THOMSON MICROELECTRONICS

TDA2320

PREAMPLIFIER FOR INFRARED REMOTE CONTROL SYSTEMS



N
DIP8
(Plastic Package)

ORDER CODE : TDA2320N

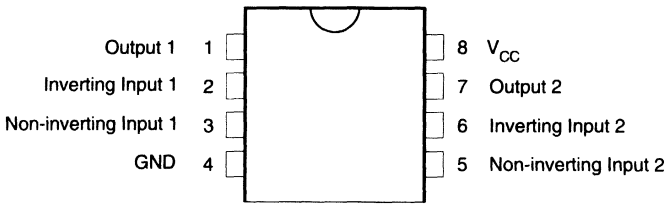
DESCRIPTION

The TDA2320 is a monolithic integrated circuit in Dip package specially designed to amplify the IR signal in remote controlled TV or radio sets. It directly interfaces with the digital control circuitry.

The TDA2320 incorporates a two-stage amplkifier with excellent sensitivity and high noise immunity. It can work with a single 5V supply voltage and flash or carrier transmission modes as provided for example by the M709A/M710A/MOS transmitters.

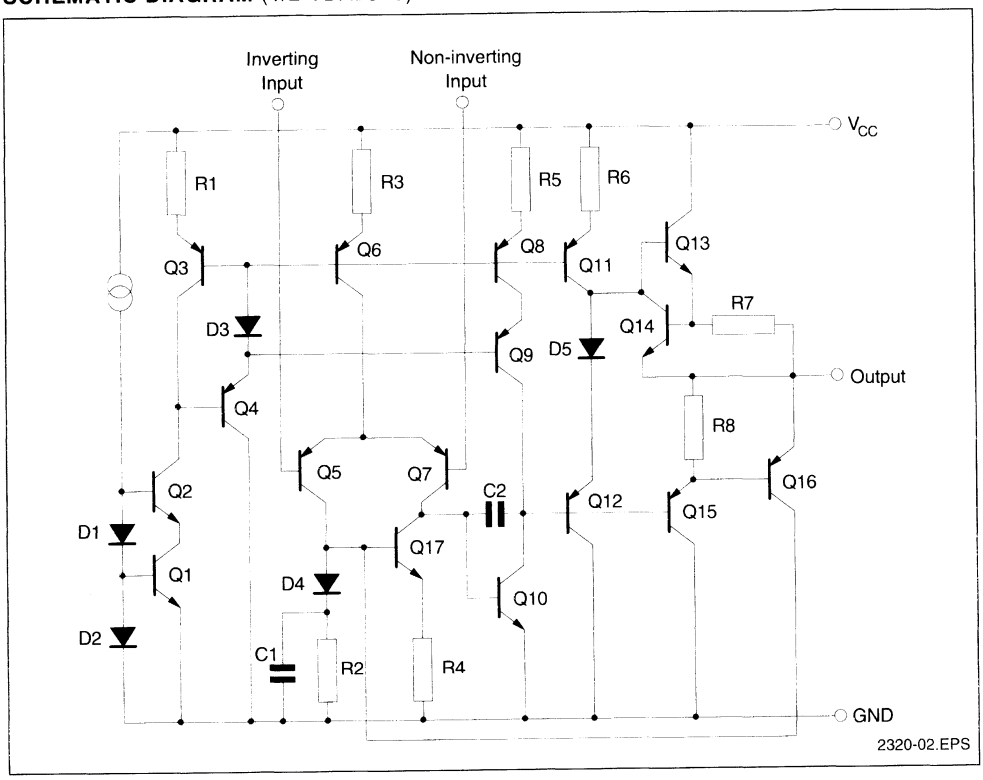
The TDA2320 is particularly intended to be used in conjunction with the M104 and M206 + M3870 remote control receivers.

PIN CONNECTIONS (top view)



2320-01.EPS

SCHEMATIC DIAGRAM (1/2 TDA2320)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	20	V
P_{tot}	Total Power Dissipation at T_{amb} = 70°C	400	mW
T_{stg}, T_j	Storage and Junction Temperature	–40 to 150	°C

ELECTRICAL CHARACTERISTICS

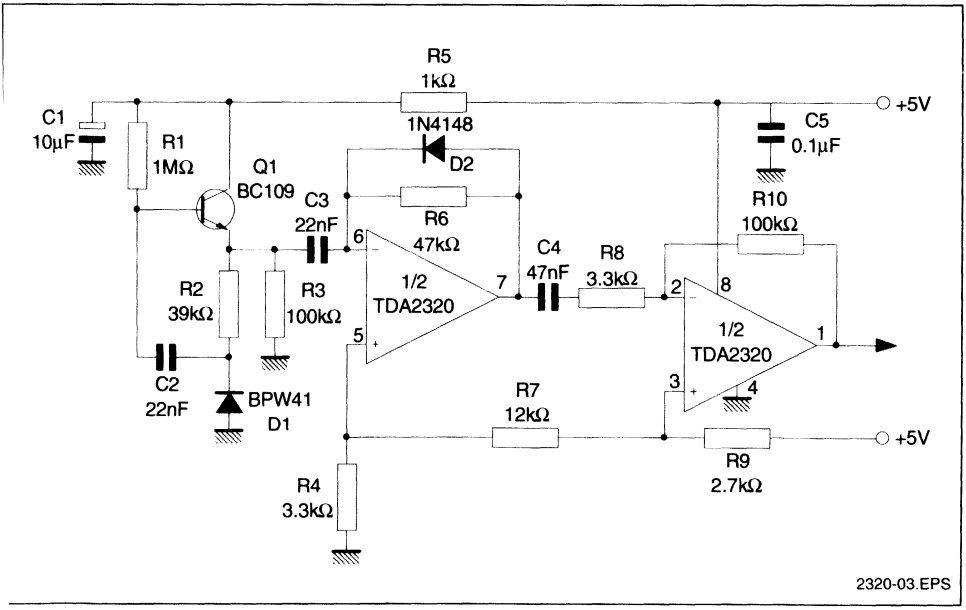
V_{CC} = 5V, T_{amb} = 25°C) (unless otherwise specified) (refer to the test circuits)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4		20	V
I_{CC}	Supply Current V_{CC} = 20V		0.8	2	mA
I_{ib}	Input Bias Current		100	500	nA
V_{io}	Input Offset Voltage R_s < 10kΩ		0.5		mV
I_{io}	Input Offset Current		15		nA
A_{vd}	Large Signal Voltage Gain f = 1kHz f = 100kHz	64	70 30		dB
V_{OPP}	DC Output Voltage Swing		2.5		V
GBP	Gain-bandwidth Product f = 100kHz	1.5	3		MHz
SR	Slew Rate R_L = 2kΩ		1.5		V/µs
e_n	Equivalent Input Noise Voltage f = 40kHz R_s = 10kΩ		20		$\frac{nV}{\sqrt{Hz}}$
SVR	Supply Voltage Rejection Ratio f = 100Hz		80		dB

2320-02.TBL

APPLICATION CIRCUIT

FLASH MODE PREAMPLIFIER



APPLICATION INFORMATION

Figure 1 : Application Circuit for Carrier Transmission Mode

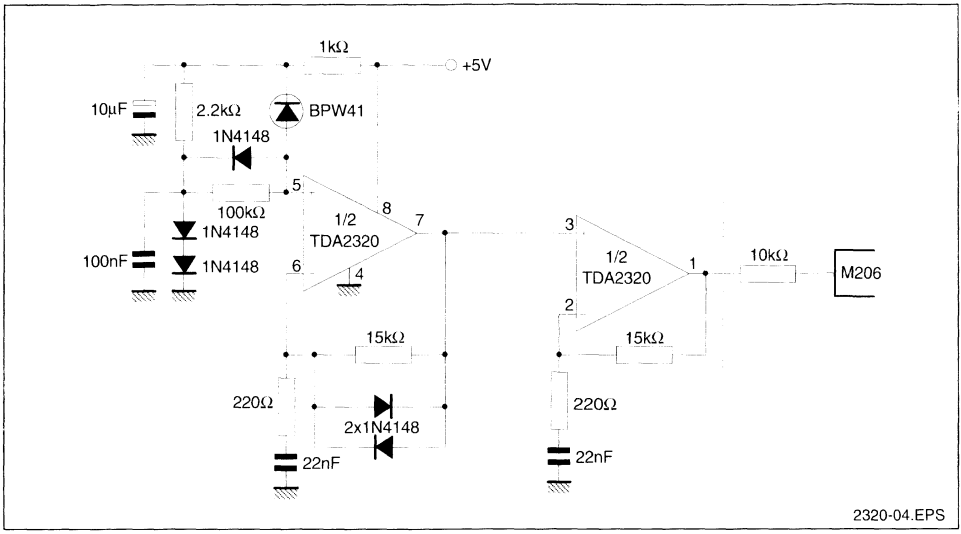


Figure 2 : IR Transmitter Using M709 or M710

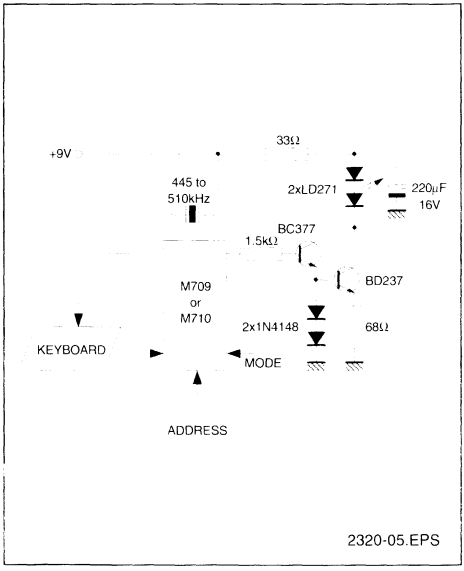
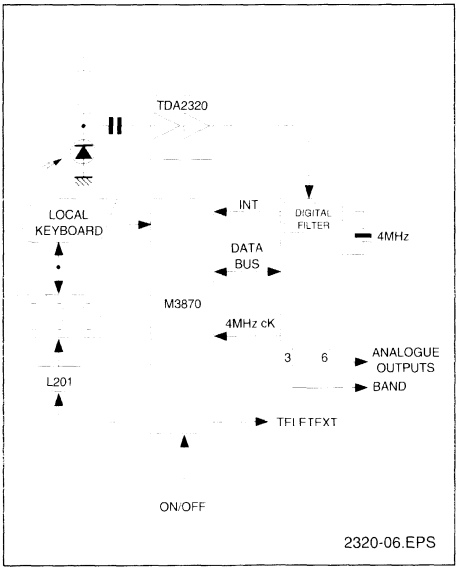


Figure 3 : MMC II - PLL TV Frequency Synthetizer

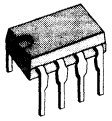


SGS-THOMSON MICROELECTRONICS

TDA2320A

STEREO AMPLIFIER

- WIDE SUPPLY VOLTAGE RANGE (3 to 36V)
- SINGLE OR SPLIT SUPPLY OPERATION
- VERY LOW CURRENT CONSUMPTION (0.8mA)
- VERY LOW DISTORTION
- NO POP-NOISE



N
DIP8
(Plastic Package)

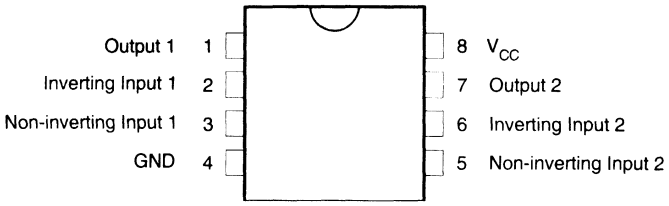
ORDER CODE : TDA2320AN

DESCRIPTION

The TDA2320A is a stereo class A preamplifier intended for application in portable cassette players and high quality audio systems.

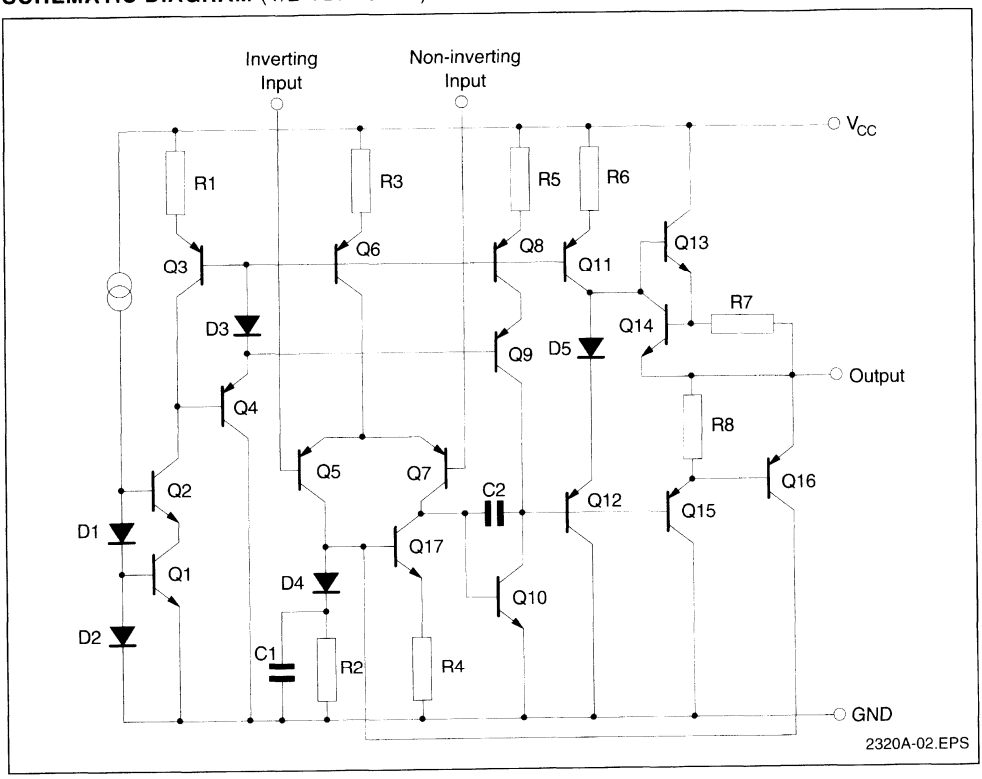
The TDA2320A is a monolithic integrated circuit in a 8 lead plastic dip.

PIN CONNECTIONS (top view)



2320A-01.EPS

SCHEMATIC DIAGRAM (1/2 TDA2320A)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	36	V
P_{tot}	Total Power Dissipation at T_{amb} = 70°C	400	mW
T_{stg}, T_j	Storage and Junction Temperature	–40 to 150	°C

ELECTRICAL CHARACTERISTICS

V_{CC} = 15V, T_{amb} = 25°C (unless otherwise specified) (refer to the test circuits)

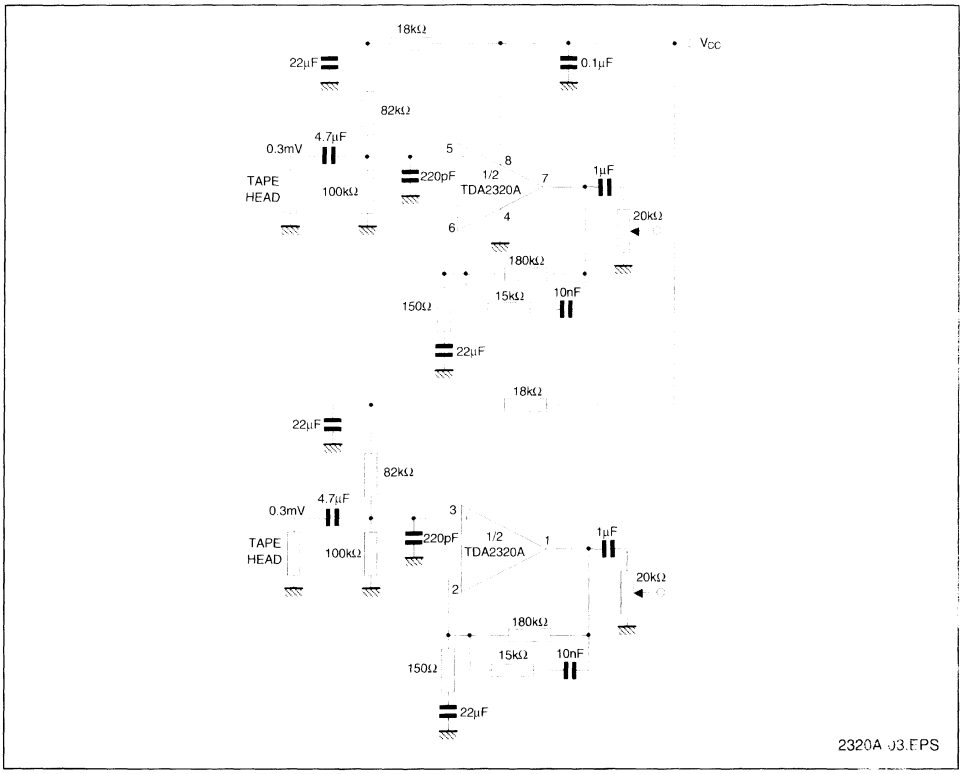
Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage (*)		3		36	V
I_{CC}	Supply Current (*)			0.8	2	mA
I_{ib}	Input Bias Current			150	500	nA
V_{io}	Input Offset Voltage $R_s \leq 10k\Omega$			 1	 5	mV
I_{io}	Input Offset Current			10	50	nA
A_{vd}	Open Loop Voltage Gain					dB
	V_{CC} = 15V	f = 333Hz		80		
		f = 1kHz		70		
		f = 10kHz		50		
	V_{CC} = 4.5V	f = 1kHz		70		
V_{OPP}	Output Voltage Swing (f = 1kHz, R_L = 600Ω) (*)					V
		V_{CC} = 15V		13		
		V_{CC} = 4.5V		2.5		
GBP	Gain-bandwidth Product f = 20kHz		 1.5	 2.5		MHz
FBP	Power Bandwidth (*) V_o = 5V_{PP}, THD = 1%		 40	 70		kHz
SR	Slew Rate (*)		1	1.6		V/µs
THD	Distortion (V_o = 2V, A_V = 20dB) (*)					%
		f = 1kHz		0.03		
		f = 10kHz		0.08		
e_n	Equivalent Input Noise Voltage (**)					µV
	Curve A	R_s = 50Ω		1		
		R_s = 600Ω		1.1	1.4	
		R_s = 5kΩ		1.5		
	B = 22Hz to 22kHz	R_s = 50Ω		1.3		
		R_s = 600Ω		1.5		
		R_s = 5kΩ		2		
	f = 1kHz	R_s = 600Ω		9		nV√Hz
V_{O1}/V_{O2}	Channel Separation (**) f = 1kHz			 100		dB
SVR	Supply Voltage Rejection Ratio(**) f = 100Hz			 80		dB

(*) Test circuit of figure 1
(**) Test circuit of figure 2

2320A-02.TBL

TYPICAL APPLICATION

STEREO PREAMPLIFIER FOR CASSETTE PLAYERS



TEST CIRCUITS

Figure 1

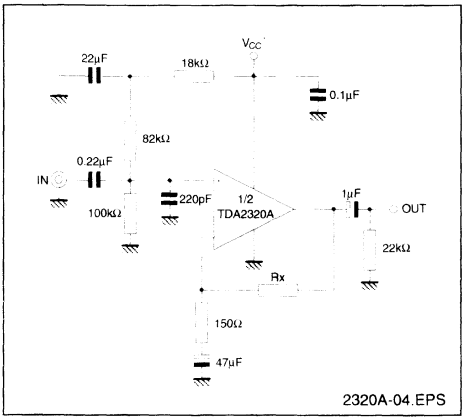


Figure 2

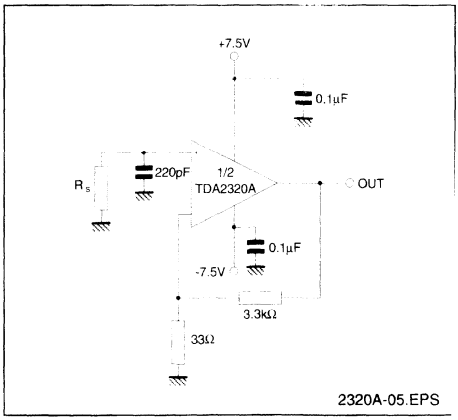
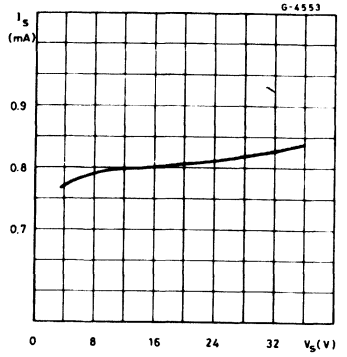
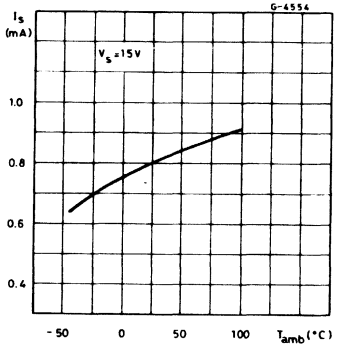


Figure 3 : Supply Current versus Supply Voltage



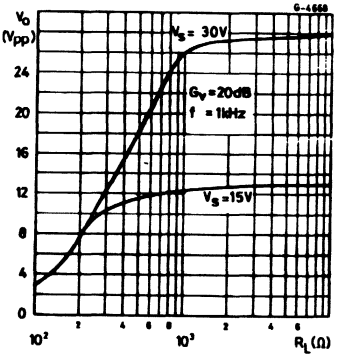
2320A-06.EPS

Figure 4 : Supply Current versus Ambient Temperature



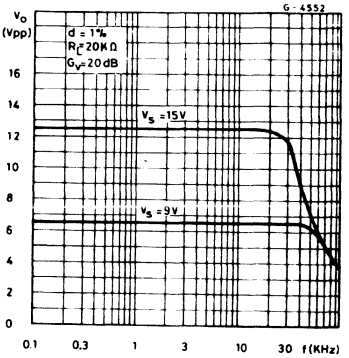
2320A-07.EPS

Figure 5 : Output Voltage Swing versus Load Resistance



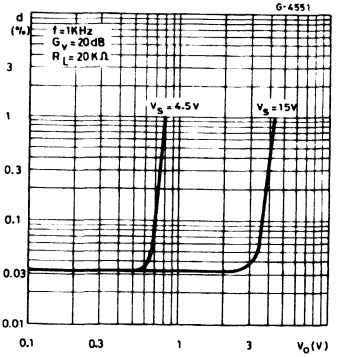
2320A-08.EPS

Figure 6 : Power Bandwidth



2320A-09.EPS

Figure 7 : Total Harmonic Distortion versusOutput Voltage



2320A-10.EPS

Figure 8 : Total Input Noise versus Source Resistance

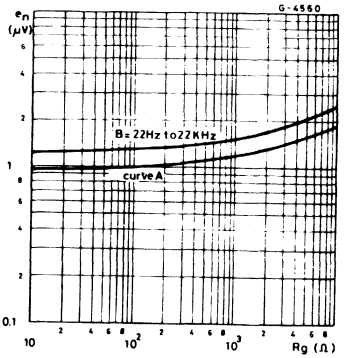


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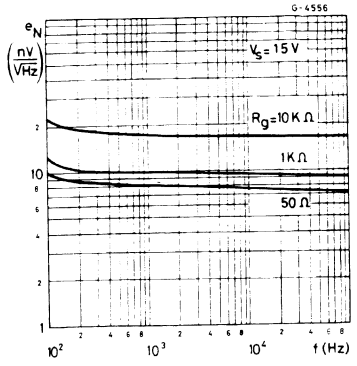
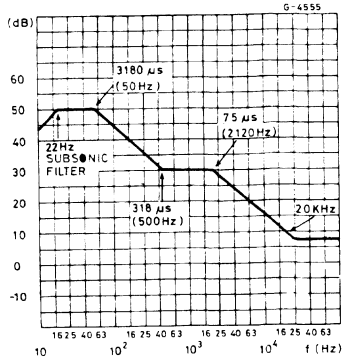
Figure 9 : Noise Density versus Frequency



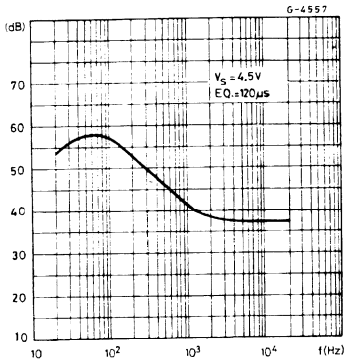
2320A-12.EPS

Figure 10 : RIAA Preamplifier Response



2320A-13.EPS

Figure 11 : Tape Preamplifier Frequency



2320A-14.EPS

APPLICATION INFORMATION

Figure 12 :Stereo RIAA Preamplifier

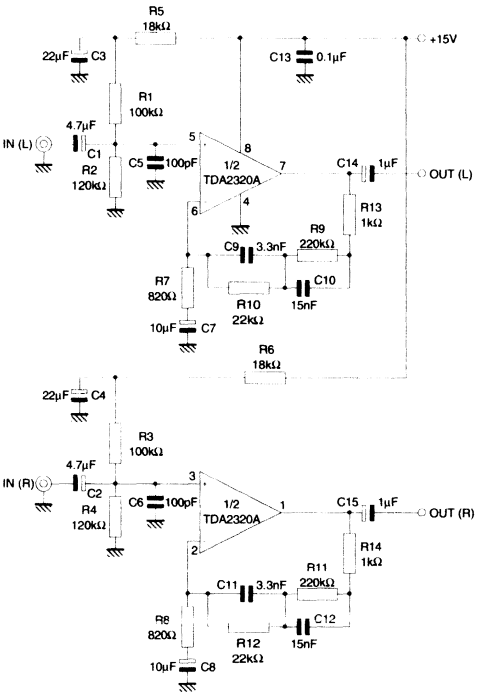


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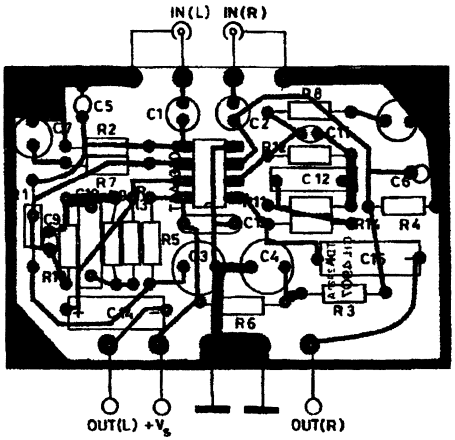
Figure 13 :P.C. Board and Components layout of the Circuit of figure 12



2320A-16.TIF

Figure 14 : Second Order 2kHz Butterworth Crossover Filter for Hi-Fi Active Boxes

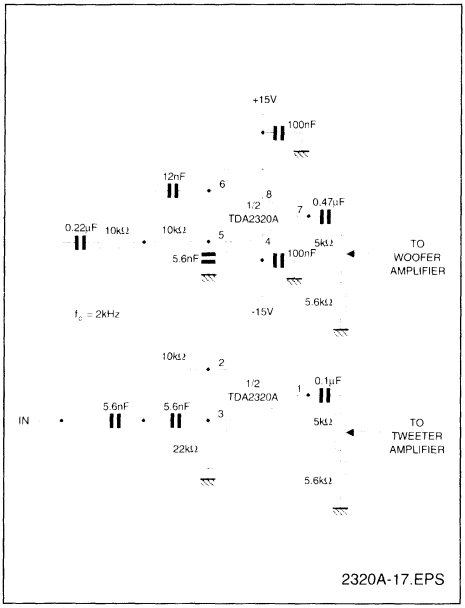


Figure 15 : Third Order 2.8kHz Bessel Crossover Filter for Hi-Fi Actives Boxes

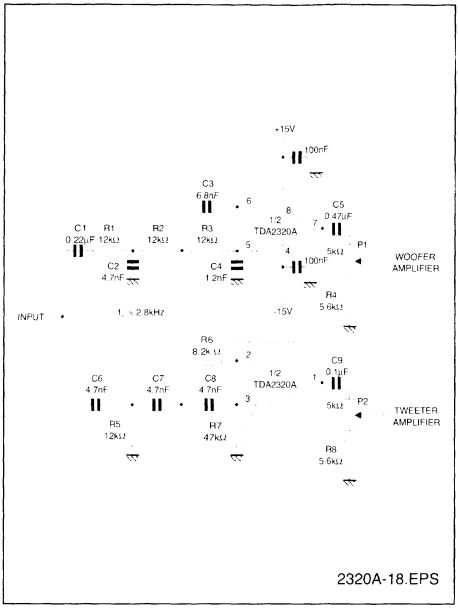


Figure 16 : Frequency Response (circuit of figure 14)

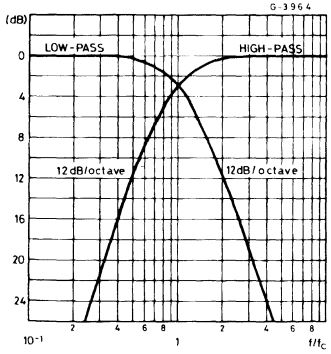


Figure 17 : Frequency Response (circuit of figure 15)

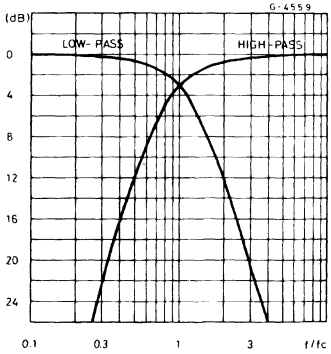


Figure 18 :200Hz to 2kHz Active Bandpass Filter for Midrange Speakers

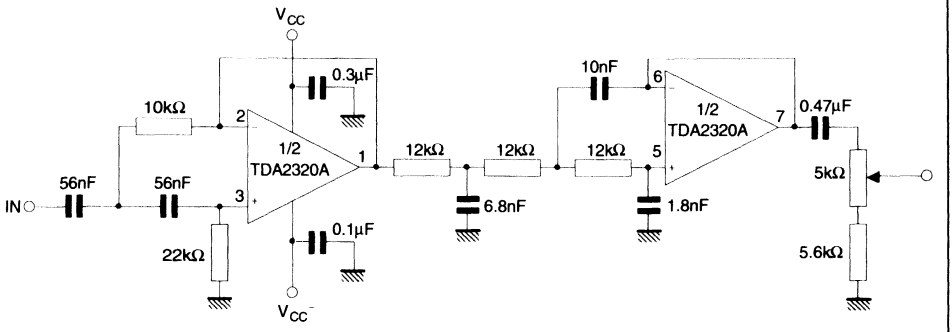
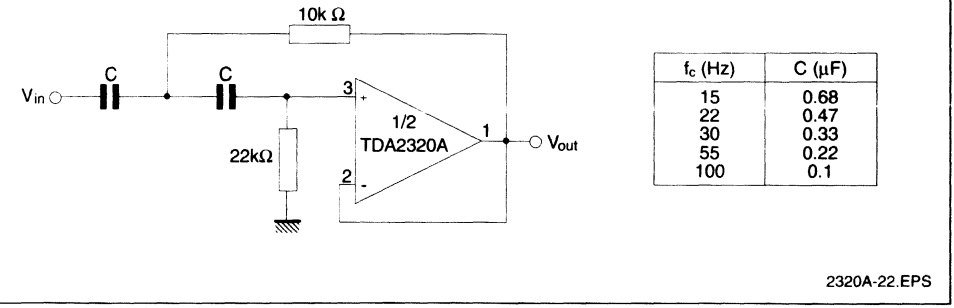
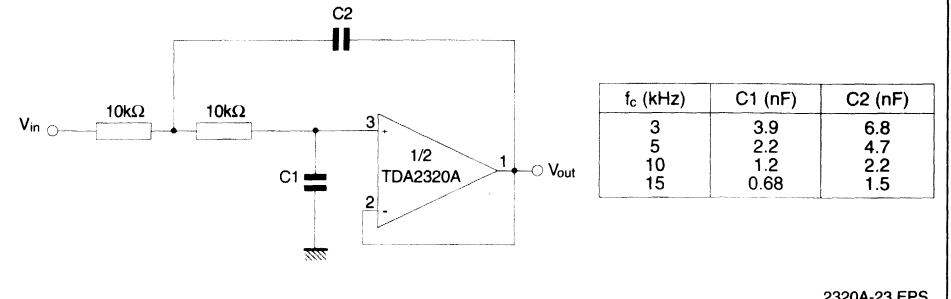


Figure 19 :Subsonic Filter



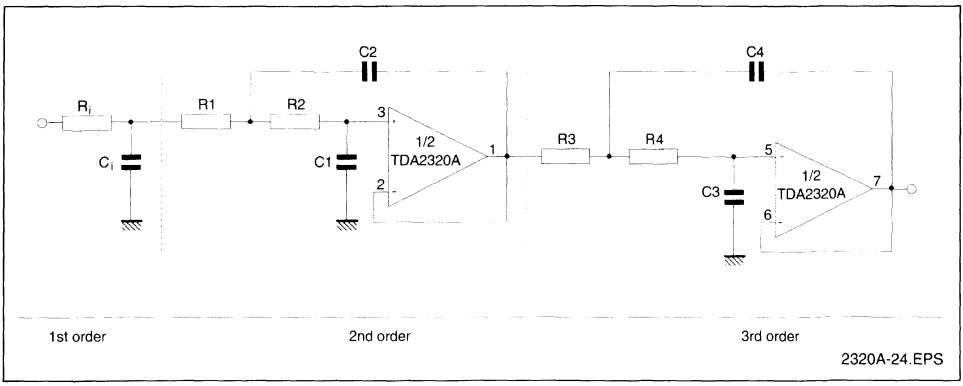
f_c (Hz)	C (µF)
15	0.68
22	0.47
30	0.33
55	0.22
100	0.1

Figure 20 :High-cut Filter



f_c (kHz)	C1 (nF)	C2 (nF)
3	3.9	6.8
5	2.2	4.7
10	1.2	2.2
15	0.68	1.5

Figure 21 : Fifth Order 3.4kHz Low-pass Butterworth Filter



For f_c = 3.4kHz and R_i = R1 = R2 = R3 = R4 = 10kΩ, we obtain :

$$C1 = 1.354 \cdot \frac{1}{R} \cdot \frac{1}{2\Pi f_c} = 6.33nF$$

$$C1 = 0.421 \cdot \frac{1}{R} \cdot \frac{1}{2\Pi f_c} = 1.97nF$$

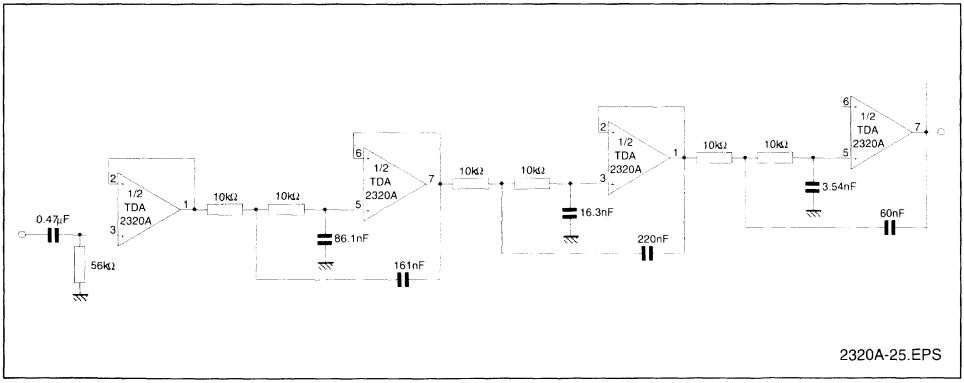
$$C2 = 1.753 \cdot \frac{1}{R} \cdot \frac{1}{2\Pi f_c} = 8.20nF$$

$$C3 = 0.309 \cdot \frac{1}{R} \cdot \frac{1}{2\Pi f_c} = 1.45nF$$

$$C4 = 3.325 \cdot \frac{1}{R} \cdot \frac{1}{2\Pi f_c} = 15.14nF$$

The attenuation of the filter is 30dB at 6.8kHz and better than 60dB at 15kHz.

Figure 22 : Sixth-pole 355Hz Low-pass Filter (Chebychev type)



This is a 6-pole Chebychev type with ±0.25dB ripple in the passband. A decoupling stage is used to avoid the influence of the input impedance of the filter's characteristics.

The attenuation is about 55dB at 710Hz and reaches 80dB at 1065Hz. The in band attenuation is limited in practice to the ±0.25dB ripple and does not exceed 1/2dB at 0.9f_c.

Figure 23 : Three Band Tone Control

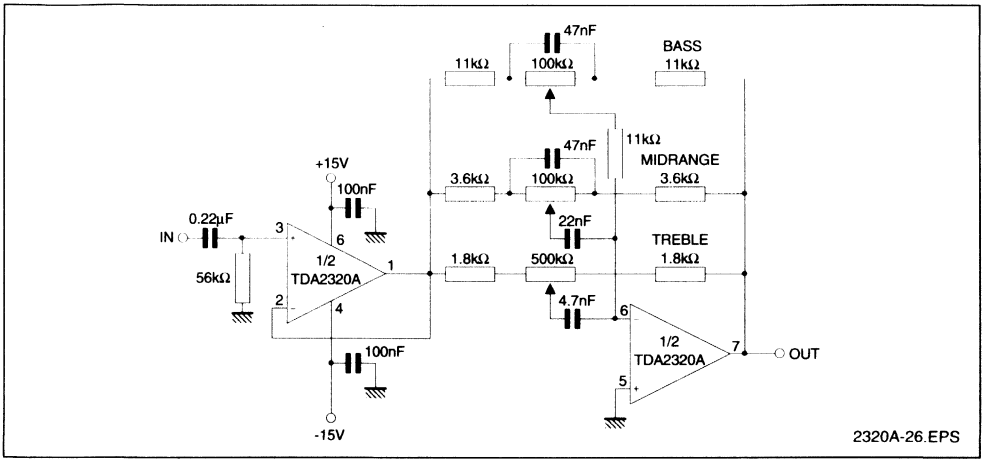
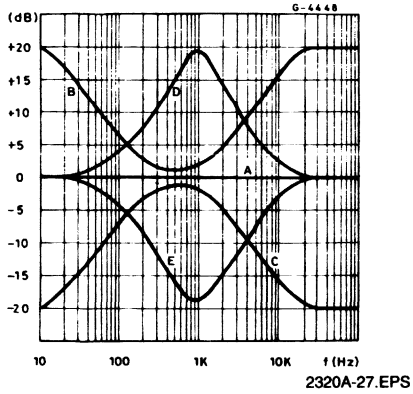


Figure 24 : Frequency Response of the Circuit of figure 23



A : all controls flat

B : bass & treble boost, mid flat

C : bass & treble cut, mid flat

D : mid boost, bass & treble flat

E : mid cut, bass treble flat

SGS-THOMSON MICROELECTRONICS

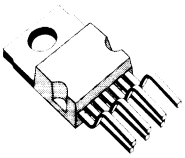
TDA8134

5V +12V REGULATOR WITH DISABLE

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST 1)

ADVANCE DATA

- OUTPUT CURRENTS UP TO 600mA
- FIXED PRECISION OUTPUT 1 VOLTAGE 5V ± 2%
- FIXED PRECISION OUTPUT 2 VOLTAGE 12V ± 2%
- OUTPUT 2 VOLTAGE DISABLED BY A TTL INPUT
- SHORT CIRCUIT PROTECTION AT BOTH OUTPUTS
- THERMAL PROTECTION
- LOW DROP OUT 1.5V AT 400mA
- HIGH SUPPLY VOLTAGE REJECTION



HEPTAWATT
(Plastic Package)

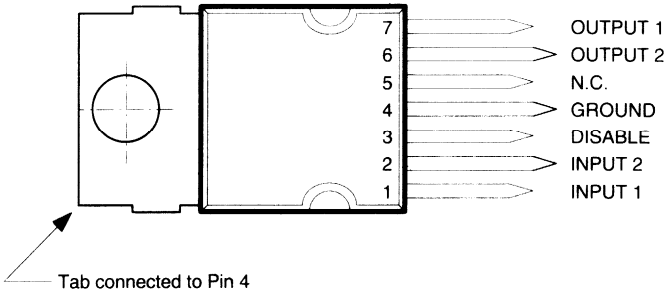
ORDER CODE : TDA8134

DESCRIPTION

The TDA8134 is a monolithic dual positive voltage regulator designed to provide fixed precision output voltages, 5V + 12V at currents up to 600mA.

Output 2 can be disabled by a TTL input. Both output currents are limited by an internal short circuit protection.

PIN CONNECTIONS



8134-01.EPS

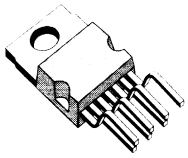
SGS-THOMSON MICROELECTRONICS

TDA8135

5V + ADJUSTABLE VOLTAGE REGULATOR WITH DISABLE

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual " (Order Code AMLISVOREST/1) **ADVANCE DATA**

- OUTPUT CURRENTS UP TO 600mA
- FIXED PRECISION OUTPUT 1 VOLTAGE 5V ± 2%
- OUTPUT 2 - VOLTAGE PROGRAMMABLE FROM 5V TO 14V
- OUTPUT 2 VOLTAGE DISABLED BY A TTL INPUT
- SHORT CIRCUIT PROTECTION AT BOTH OUTPUTS
- THERMAL PROTECTION
- LOW DROP OUT 1.5V AT 400mA
- HIGH SUPPLY VOLTAGE REJECTION



HEPTAWATT
(Plastic Package)

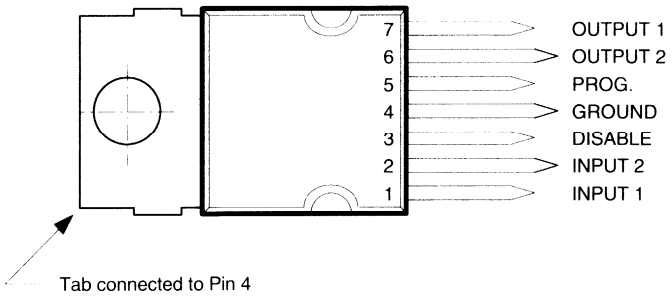
ORDER CODE : TDA8135

DESCRIPTION

The TDA8135 is a monolithic dual positive voltage regulator designed to provide fixed precision output voltages, 5V + adjustable outputs at currents up to 600mA.

Output 2 can be disabled by a TTL input. Both output currents are limited by an internal short circuit protection.

PIN CONNECTIONS



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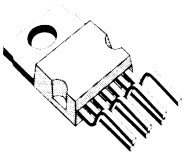
SGS-THOMSON MICROELECTRONICS

TDA8136

DUAL 12V REGULATOR WITH DISABLE

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST 1) **ADVANCE DATA**

- OUTPUT CURRENTS UP TO 600mA
- FIXED PRECISION OUTPUT 1 VOLTAGE 12V ± 2%
- FIXED PRECISION OUTPUT 2 VOLTAGE 12V ± 2%
- OUTPUT 2 VOLTAGE DISABLED BY A TTL INPUT
- SHORT CIRCUIT PROTECTION AT BOTH OUTPUTS
- THERMAL PROTECTION
- LOW DROP OUT 1.5V AT 400mA
- HIGH SUPPLY VOLTAGE REJECTION



HEPTAWATT
(Plastic Package)

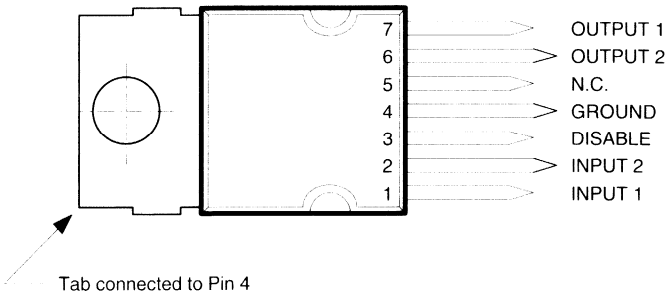
ORDER CODE : TDA8136

DESCRIPTION

The TDA8136 is a monolithic dual positive voltage regulator designed to provide fixed precision output voltages, both 12V at currents up to 600mA.

Output 2 can be disabled by a TTL input. Both output currents are limited by an internal short circuit protection.

PIN CONNECTIONS



8136-01.EPS

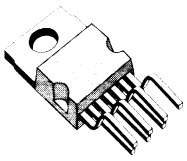
SGS-THOMSON MICROELECTRONICS

TDA8137

DUAL 5.1V REGULATOR WITH DISABLE AND RESET

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST/1) **ADVANCED DATA**

- OUTPUT CURRENTS UP TO 1A
- FIXED PRECISION OUTPUT VOLTAGES 5.1V ± 2%
- OUTPUT 1 WITH RESET FACILITY
- OUTPUT 2 WITH DISABLE BY TTL INPUT
- SHORT CIRCUIT PROTECTION AT BOTH OUTPUTS
- THERMAL PROTECTION
- LOW DROP OUTPUT VOLTAGE



HEPTAWATT
(Plastic Package)

ORDER CODE : TDA8137

DESCRIPTION

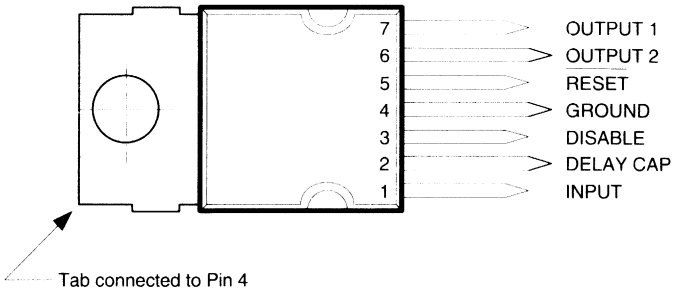
The TDA8137 is a monolithic dual positive voltage regulator designed to provide fixed precision output voltages of 5.1V at currents up to 1A.

An internal reset circuit generates a reset pulse when the output 1 decreases below the regulated voltage value.

Output 2 can be disabled by TTL input.

Short circuit and thermal protections are included.

PIN CONNECTION (top view)

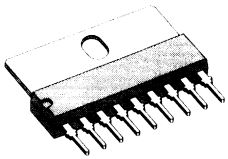


8137-01.EPS

5.1V +12V REGULATOR WITH DISABLE AND RESET

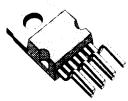
For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST/1) **ADVANCE DATA**

- OUTPUT CURRENTS UP TO 1A
- FIXED PRECISION OUTPUT 1 VOLTAGE 5.1V +/- 2%
- FIXED PRECISION OUTPUT 2 VOLTAGE 12V +/- 2%
- OUTPUT 1 WITH RESET FACILITY
- OUTPUT 2 WITH DISABLE BY TTL INPUT
- SHORT CIRCUIT PROTECTION AT BOTH OUTPUTS
- THERMAL PROTECTION
- LOW DROP OUTPUT VOLTAGE
- AVAILABLE ALSO IN HEPTAWATT PACKAGE IN TWO VERSIONS : TDA8138A (DISABLE ONLY), TDA8138B (RESET ONLY)



SIP9
(Plastic Package)

ORDER CODE : TDA8138



HEPTAWATT
(Plastic Package)

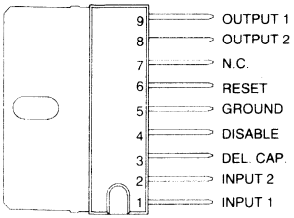
ORDER CODE : TDA8138A / TDA8138B

DESCRIPTION

The TDA8138 is a monolithic dual positive voltage regulator designed to provide fixed precision output voltages of 5.1V and 12V at currents up to 1A.
An internal reset circuit generates a reset pulse when the output 1 decrease below the regulated voltage value (for TDA8138 and TDA8138B).
Output 2 can be disabled by TTL input (for TDA8138 and TDA8138A).
Short circuit and thermal protections are included in all the versions.

PIN CONNECTIONS

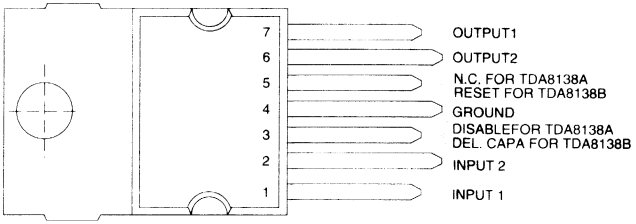
SIP9



Tab. connected to Pin 5

8138-01A.EPS

HEPTAWATT



Tab. connected to Pin 4

8138-01B.EPS

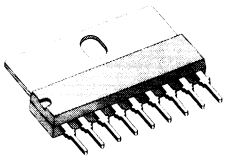
SGS-THOMSON MICROELECTRONICS

TDA8139

5.1V AND ADJUSTABLE VOLTAGE REGULATOR WITH DISABLE AND RESET

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual " (Order Code AMLISVOREST/1) **ADVANCE DATA**

- OUTPUT CURRENTS UP TO 750mA
- FIXED PRECISION OUTPUT 1 VOLTAGE 5.1V ± 2%
- OUTPUT 2 VOLTAGE PROGRAMMABLE FROM 2.8 TO 16V
- OUTPUT 1 WITH RESET FACILITY
- OUTPUT 2 WITH DISABLE BY TTL INPUT
- SHORT CIRCUIT PROTECTION AT BOTH OUTPUTS
- THERMAL PROTECTION
- LOW DROP OUTPUT VOLTAGE



SIP9
(Plastic Package)

ORDER CODE : TDA8139

DESCRIPTION

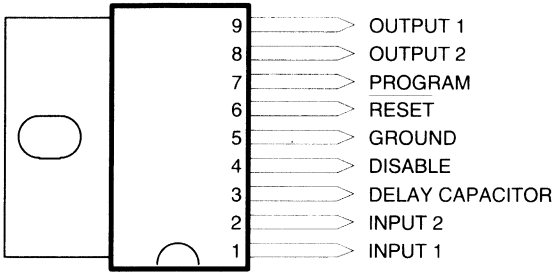
The TDA8139 is a monolithic dual positive voltage regulator designed to provide precision output voltages of 5.1V and adjustable at currents up to 1A.

An internal reset circuit generates a reset pulse when the output 1 decrease below the regulated voltage value.

Output 2 can be disabled by TTL input.

Short circuit and thermal protections are included.

PIN CONNECTIONS



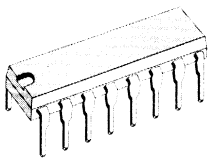
8139-01.EPS

SGS-THOMSON MICROELECTRONICS

TDB7910
TDA7910

MEDIUM POWER SINGLE BIPOLAR OPERATIONAL AMPLIFIER

- OUTPUT CURRENT UP TO 500 mA
- OFFSET VOLTAGE NULL CAPABILITY
- SHORT-CIRCUIT PROTECTION
- THERMAL OVERLOAD PROTECTION
- PLASTIC PACKAGE FOR EASY ASSEMBLY



N
DIP16
(Plastic Package)

DESCRIPTION

The TDB7910 and TDA7910 are internally compensated medium power operational amplifiers intended for use in those applications requiring load currents of several hundred milliamperes. Applications include servo amplifiers, driver interfaces, precision power comparators and motor speed control.

These amplifiers are designed to operate from a single or dual power supplies and the input common-mode range includes the negative supply if balance inputs are tied to the negative supply.

The TDB7910 and TDA7910 are thermal overload and short-circuit protected.

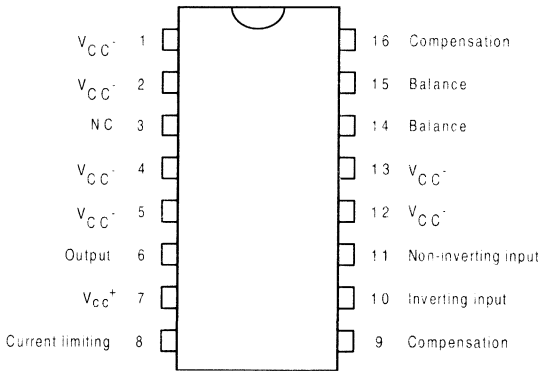
ORDER CODES

Part Number	Temperature Range	Package N
TDB7910	0°C, +70°C	•
TDA7910	-40°C, +105°C	•

Example : TDB7910N

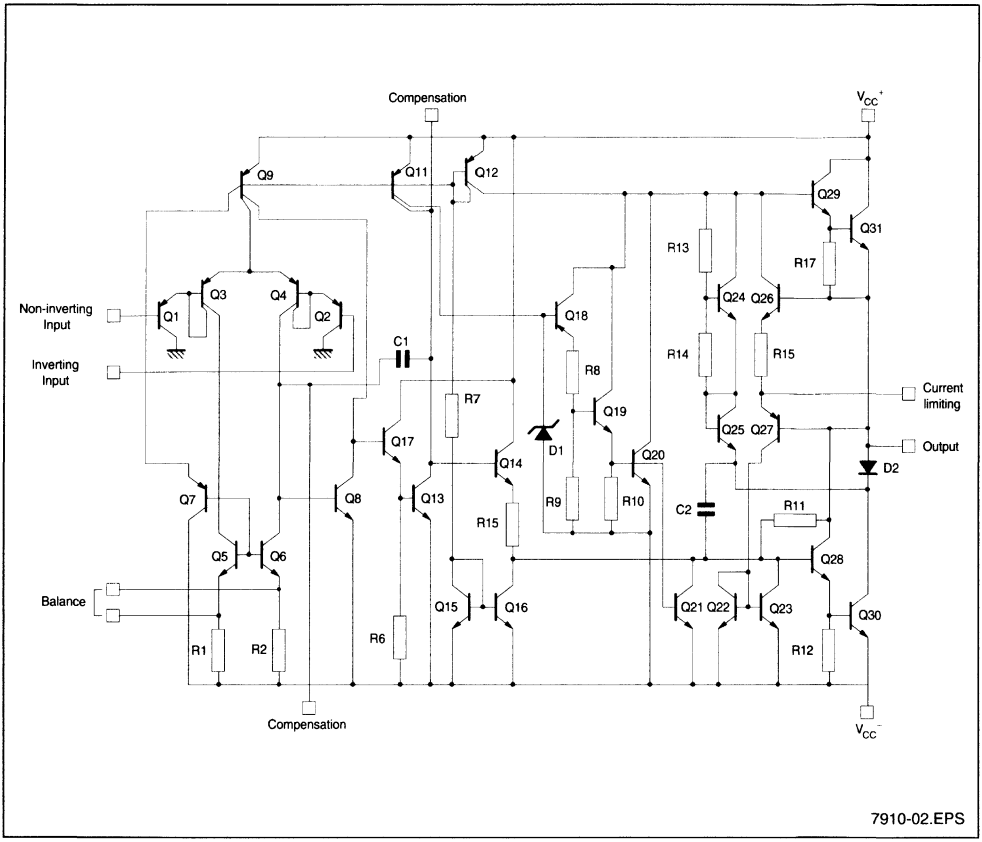
7910-01.TBL

PIN CONNECTIONS (top view)



7910-01.EPS

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		± 18	V
V_i	Input Voltage		± 15	V
V_{id}	Differential Input Voltage		± 30	V
I_O	Output Current*		0.75	A
P_{tot}	Power Dissipation		7.5	W
T_{oper}	Operating Free-air Temperature Range	TDA7910 TDA7910	0 to +70 -40 to +105	°C
T_{stg}	Storage Temperature Range		-65 to +150	°C

* Under short-circuit conditions, the safe operating area and dc power dissipation limitations must be observed.

7910-02 TBL

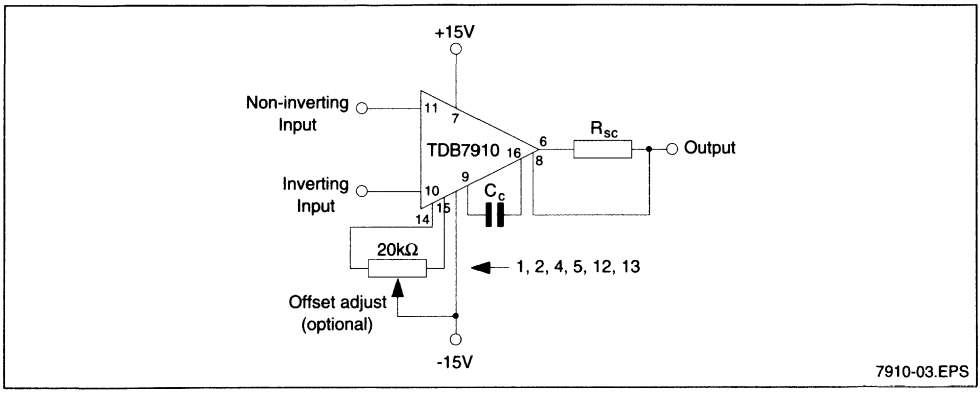
ELECTRICAL CHARACTERISTICS

V_{CC} = ±15V, T_{amb} = 25°C (unless otherwise specified)

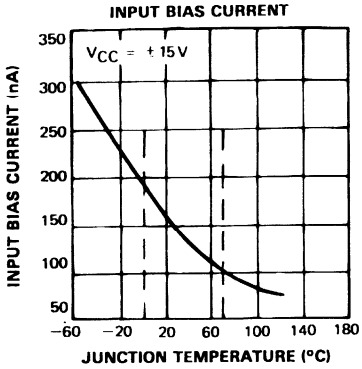
Symbol	Parameter	TDB7910 - TDA7910			Unit
		Min.	Typ.	Max.	
V_{io}	Input Offset Voltage T_{amb} = +25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		2	6 7.5	mV
I_{io}	Input Offset Current T_{amb} = +25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		20	200 300	nA
I_{ib}	Input Bias Current T_{amb} = +25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		80	500 800	nA
A_{vd}	Large Signal Voltage Gain (R_L = 47Ω, V_o = ±10V) T_{amb} = +25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	20 15			V/mV
I_{CC}	Supply Current - (no load) T_{amb} = +25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		10	20 25	mA
V_{icm}	Input Common Mode Voltage Range	±12	±13		V
I_{OS}	Output Short Circuit Current (R_{SC} = 1.5Ω)		0.5		A
SVR	Supply Voltage Rejection Ratio	77			dB
CMR	Common Mode Rejection Ratio	70			dB
Z_i	Input Impedance	0.3			MΩ
V_{OPP}	Output Voltage Swing (R_{SC} = 0, R_L = 47Ω) T_{amb} = +25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	 ±11 ±10	±12		V
V_{ior}	Offset Voltage Adjustment Range		±15		mV
SR	Slew Rate (R_L = 47Ω, T_{amb} = +25°C , A_V = 1, V_{in} = ±10V)		0.5		V/µs
GBP	Gain Bandwidth Product (C_C = 0, R_L = 47Ω, C_L = 100pF, f = 100kHz, V_{in} = 10mV)		1		MHz
R_{TH}	Thermal Resistance		60		°C/W

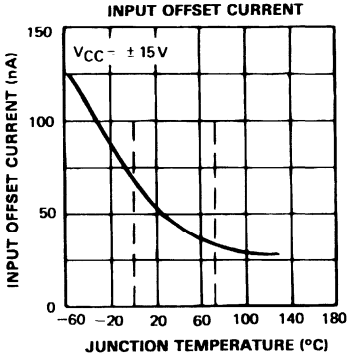
7910-03.TBL

BASIC DIAGRAM



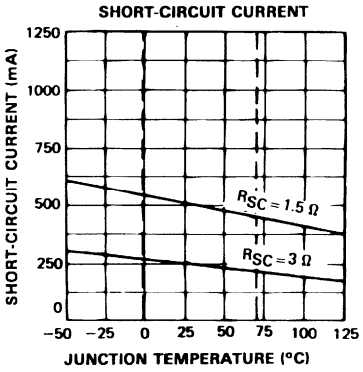
7910-03.EPS





7910-04.EPS

7910-05.EPS

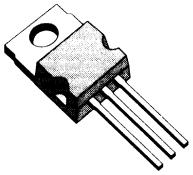


7910-06.EPS

LOW-DROP VOLTAGE REGULATOR

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST/1)

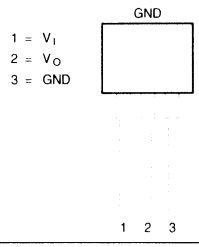
- V_O = 5V ± 4 % (I_O = 5mA)
- $I_{OS} \geq$ 500mA
- $V_I - V_O \leq$ 0.6 V (I_O = 500mA)
- $V_{I\ (surge)}$ = ± 80V
- THERMAL AND SHORT-CIRCUIT PROTECTION



TO220
(Plastic Package)

ORDER CODE : TEA7605SP

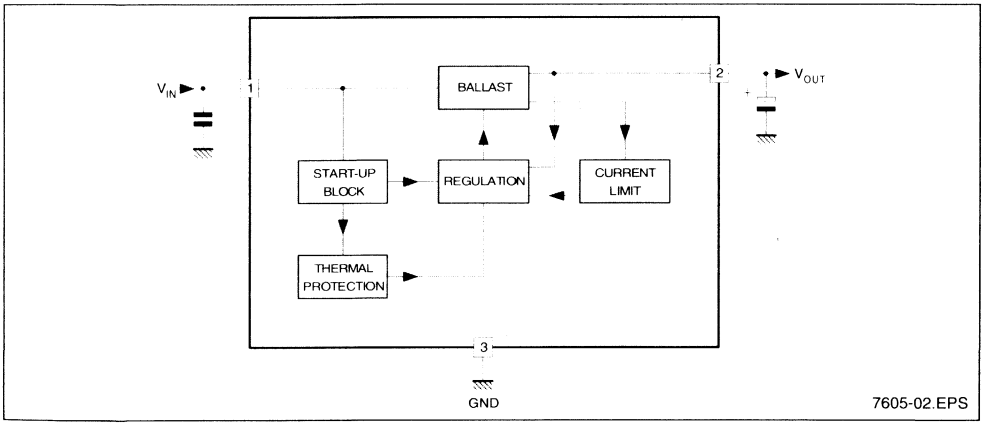
PIN CONNECTIONS



DESCRIPTION

TEA7605 is a low-drop 5V regulator well suited to supplying stabilized voltage to µPs in harsh industrial environment.
Special care was taken to keep :
- Lowest possible quiescent current (250µA).
- Lowest possible output capacitor (1µF).

BLOCK DIAGRAM

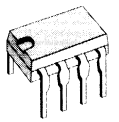


SGS-THOMSON MICROELECTRONICS

TEB1033
TEF1033-TEC1033

DUAL BIPOLAR OPERATIONAL AMPLIFIERS

- LOW DISTORTION RATIO
- LOW NOISE
- VERY LOW SUPPLY CURRENT
- LOW INPUT OFFSET CURRENT
- VERY LOW INPUT OFFSET VOLTAGE
- LARGE COMMON-MODE RANGE
- HIGH GAIN
- HIGH OUTPUT CURRENT
- GAIN-BANDWIDTH PRODUCT : 2.5MHz
- TEMPERATURE DRIFT : 2μV/°C
- LONG TERM STABILITY : 8μV/YEAR (for $T_{amb} \leq 50°C$)
- THE TEB1033 AND TEF1033 ARE PIN TO PIN REPLACEMENT OF THE LS204C AND LS204I RESPECTIVELY



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

J
CERDIP8
(Cerdip Package)

H
TO99
(Metal Can)

DESCRIPTION

The TEB1033, TEF1033 and TEC1033 are high performance dual-operational amplifiers intended for active filter applications. The internal phase compensation allows stable operation as voltage follower in spite of their high gain-bandwidth products.

The circuits present very stable electrical characteristics over the entire supply voltage range.

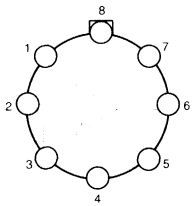
ORDER CODES

Part Number	Temperature Range	Package			
		H	N	J	D
TEB1033	0°C, +70°C	•	•	•	•
TEF1033	–40°C, +105°C	•	•	•	•
TEC1033	–55°C, +125°C	•	•	•	•
Example : TEB1033N					

1033-01 TBL

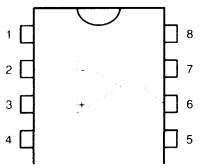
PIN CONNECTIONS (top views)

TO99



1033-01.EPS

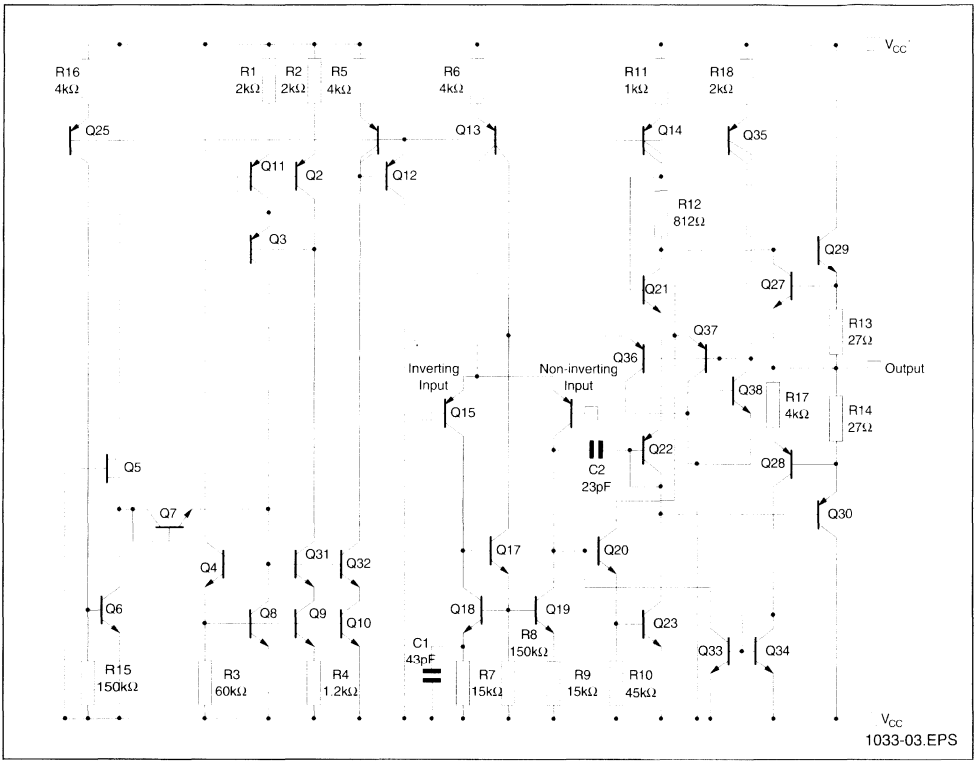
DIP8/SO8
CERDIP8



1033-02.EPS

1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^-
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - V_{CC}^+

BLOCK DIAGRAM (1/2 TEB1033)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		± 18	V
V_i	Input Voltage		± V_{CC}	V
V_{id}	Differential Input Voltage		± (V_{CC} –1)	V
P_{tot}	Power Dissipation	D suffix N suffix	400 665	mW
T_{oper}	Operating Free-air Temperature Range	TEB1033 TEF1033 TEC1033	0 to +70 –40 to +105 –55 to +125	°C
T_{stg}	Storage Temperature Range		–65 to +150	°C

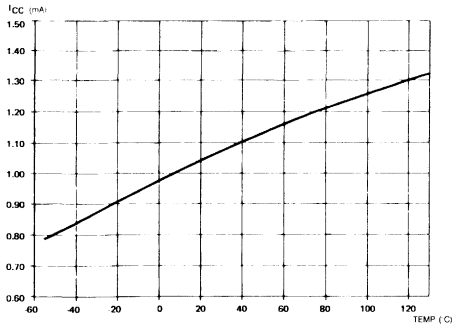
1033-02.TBL

ELECTRICAL CHARACTERISTICS

V_{CC} = ±15V, T_{amb} = +25°C (unless otherwise specified)

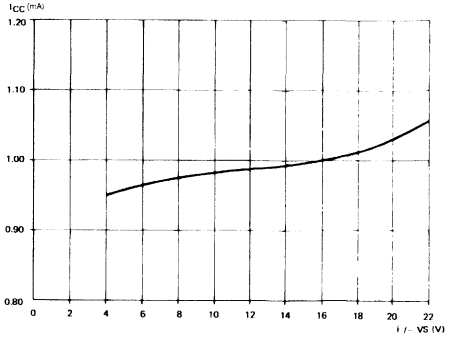
Symbol	Parameter	TEB 1033 TEF 1033 TEC 1033			Unit
		Min.	Typ.	Max.	
V_{io}	Input Offset Voltage ($R_S \leq 10k\Omega$) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		0.3	1 3	mV
DV_{io}	Input Offset Voltage Drift		2		µV/°C
I_{io}	Input Offset Current T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		5	20 40	nA
I_{ib}	Input Bias Current T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		50	100 200	nA
A_{vd}	Large Signal Voltage Gain (R_L = 2kΩ, V_O = ±10V) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	80 40	120		V/mV
SVR	Supply Voltage Rejection Ratio (DV_{CC} from ±15V to ±4V) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	80 70	100		dB
I_{CC}	Supply Current, all Amp, no Load T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		1	1.5 2	mA
V_{icm}	Input Common Mode Voltage Range T_{amb} = 25°C	±12			V
CMR	Common Mode Rejection Ratio ($R_S \leq 10k\Omega$, V_{ic} = ±10V) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	80 70	100		dB
I_{os}	Output Short-circuit Current T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	10 10	23	40 40	mA
± V_{opp}	Output Voltage Swing T_{amb} = 25°C R_L = 2kΩ $T_{min.} \leq T_{amb} \leq T_{max.}$ R_L = 2kΩ V_{CC} = ±4V, R_L = 2kΩ, T_{amb} = 25°C V_{CC} = ±6V, R_L = 600Ω, T_{amb} = 25°C	13 12 2.8 4.6	14 3		V
SR	Slew-rate (V_I = ±10V, R_L = 2 kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)	0.6	1		V/µs
GBP	Gain Bandwidth Product (f = 100kHz, T_{amb} = 25°C, V_{in} = 10mV, R_L = 2kΩ, C_L = 100pF)	1.5	2		MHz
R_I	Input Resistance		1		MΩ
THD	Total Harmonic Distortion (f = 1kHz, A_v = 20dB, R_L = 2kΩ C_L = 100pF, T_{amb} = 25°C, V_o = $2V_{pp}$)		0.008	0.05	%
e_n	Equivalent Input Noise Voltage (f = 1kHz) R_S = 50Ω R_S = 1kΩ R_S = 10kΩ		8 10 18	15	$\frac{nV}{\sqrt{Hz}}$
V_{OPP}	Large Signal Voltage Swing R_L =10kΩ, f = 10kHz	26	28		V
Øm	Phase Margin		45		Degrees
V_{o1}/V_{o2}	Channel Separation	100	120		dB

1033-03.TBL



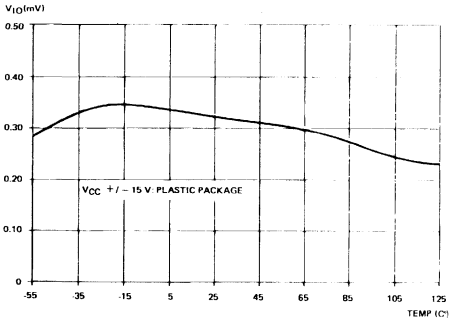
SUPPLY CURRENT VS. AMBIENT TEMPERATURE

1033-04.EPS



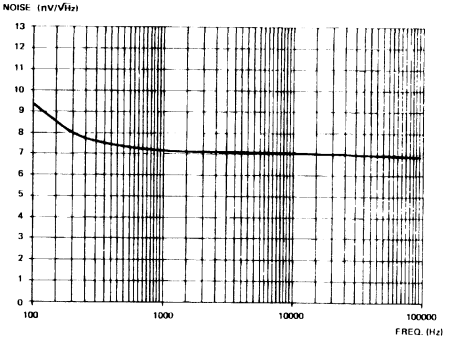
SUPPLY CURRENT VS. SUPPLY VOLTAGE

1033-05.EPS



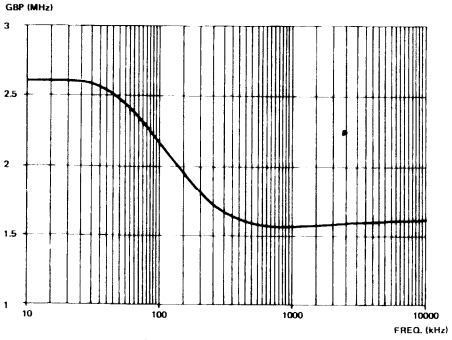
OFFSET VOLTAGE VS. AMBIENT TEMPERATURE

1033-06.EPS



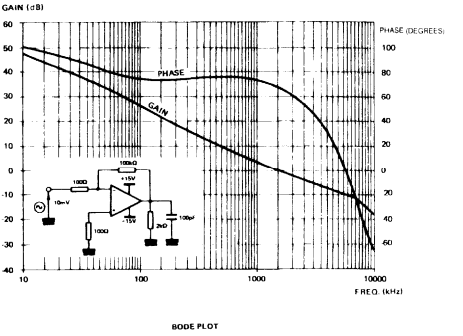
TOTAL INPUT NOISE VS. FREQUENCY

1033-07.EPS



GAIN BANDWIDTH PRODUCT VS. FREQUENCY

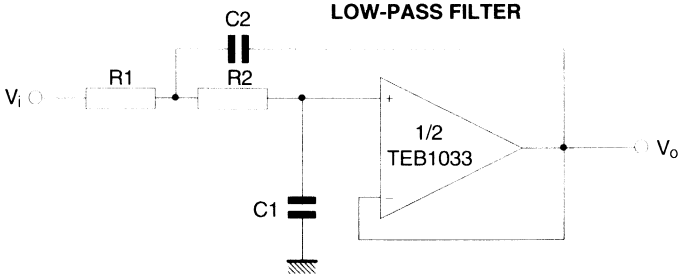
1033-08.EPS



BODE PLOT

1033-09.EPS

TYPICAL APPLICATION



$$\frac{V_o}{V_i} = \frac{1}{1 + 2\xi\frac{S}{\omega_c} + \frac{S^2}{\omega_c^2}}$$

$\varpi_C = 2\pi f_C$, with f_C = cutt-off frequency
ξ = damping factor

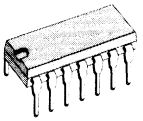
1033-10.EPS

SGS-THOMSON MICROELECTRONICS

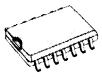
TEB4033
TEF4033-TEC4033

QUAD BIPOLAR OPERATIONAL AMPLIFIERS

- LOW DISTORTION RATIO
- LOW NOISE
- VERY LOW SUPPLY CURRENT
- LOW INPUT OFFSET CURRENT
- VERY LOW INPUT OFFSET VOLTAGE
- LARGE COMMON-MODE RANGE
- HIGH GAIN
- HIGH OUTPUT CURRENT
- GAIN-BANDWIDTH PRODUCT : 2.5MHz
- TEMPERATURE DRIFT : 2µV/°C
- LONG TERM STABILITY : 8µV/YEAR (for $T_{amb} \leq 50°C$)
- THE TEB4033 AND TEF4033 ARE PIN TO PIN REPLACEMENT OF THE LS204C AND LS204I RESPECTIVELY



N
DIP14
(Plastic Package)
J
CERDIP14
(Cerdip Package)



D
SO14
(Plastic Micropackage)

DESCRIPTION

The TEB4033, TEF4033 and TEC4033 are high performance quad-operational amplifiers intended for active filter applications. The internal phase compensation allows stable operation as voltage follower in spite of their high gain-bandwidth products.

The circuits present very stable electrical characteristics over the entire supply voltage range.

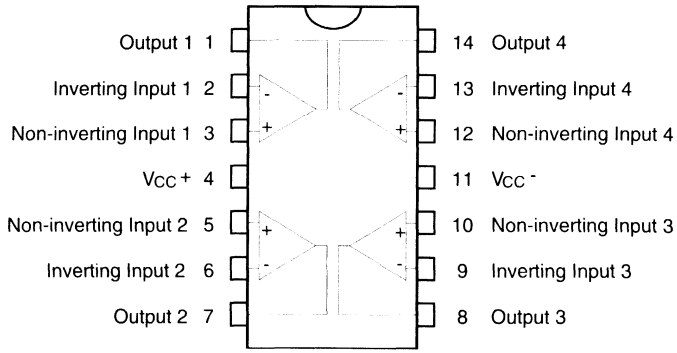
ORDER CODES

Part Number	Temperature Range	Package		
		N	J	D
TEB4033	0°C, +70°C	•	•	•
TEF4033	–40°C, +105°C	•	•	•
TEC4033	–55°C, +125°C	•	•	•

Example : TEB4033N

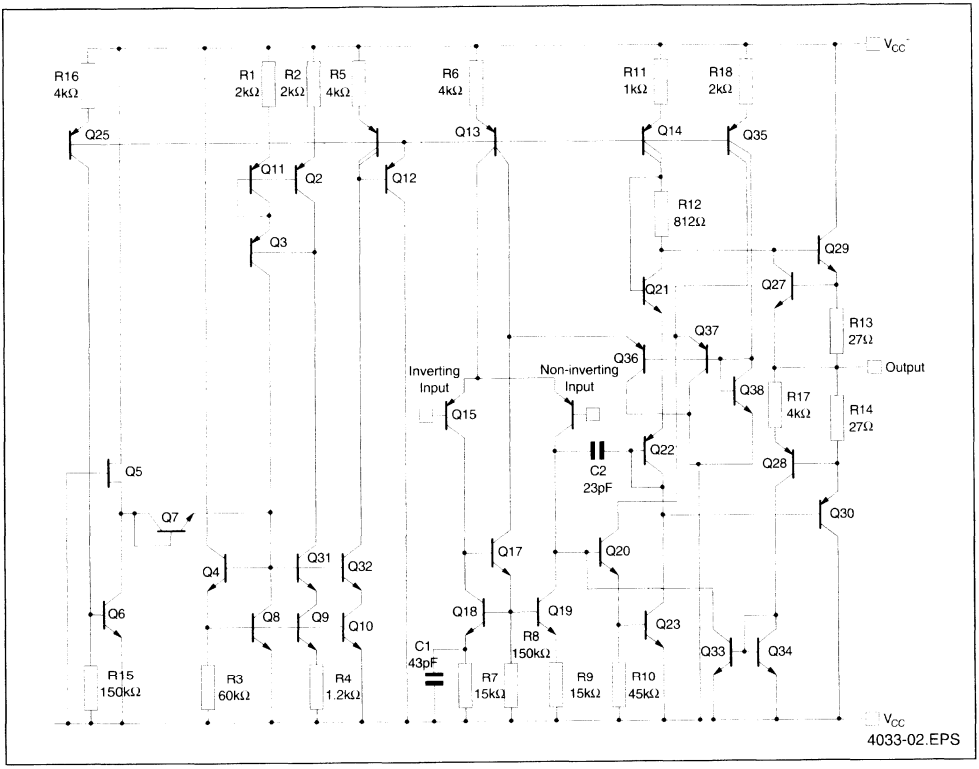
4033-01.TBL

PIN CONNECTIONS (top view)



4033-01.EPS

BLOCK DIAGRAM (1/4 TEB4033)



ABSOLUTE MAXIMUM RATINGS

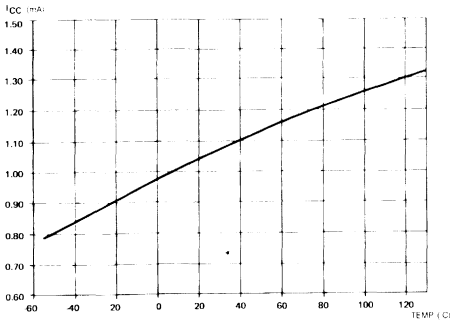
Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		± 18	V
V_i	Input Voltage		± V_{CC}	V
V_{id}	Differential Input Voltage		± (V_{CC} –1)	V
P_{tot}	Power Dissipation	D suffix N suffix	400 665	mW
T_{oper}	Operating Free-air Temperature Range	TEB4033 TEF4033 TEC4033	0 to +70 –40 to +105 –55 to +125	°C
T_{stg}	Storage Temperature Range		–65 to +150	°C

ELECTRICAL CHARACTERISTICS

V_{CC} = ±15V, T_{amb} = +25°C (unless otherwise specified)

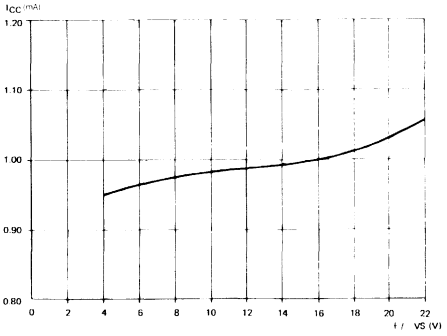
Symbol	Parameter	TEB 1033 TEF 1033 TEC 1033 Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage ($R_S \leq 10k\Omega$) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		0.3	1 3	mV
DV_{io}	Input Offset Voltage Drift		2		µV/°C
I_{io}	Input Offset Current T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		5	20 40	nA
I_{ib}	Input Bias Current T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		50	100 200	nA
A_{vd}	Large Signal Voltage Gain (R_L = 2kΩ, V_O = ±10V) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	80 40	120		V/mV
SVR	Supply Voltage Rejection Ratio (DV_{CC} from ±15V to ±4V) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	80 70	100		dB
I_{CC}	Supply Current, all Amp, no Load T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		2	3 4	mA
V_{icm}	Input Common Mode Voltage Range T_{amb} = 25°C	±12			V
CMR	Common Mode Rejection Ratio ($R_S \leq 10k\Omega$, V_I = ±10V) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	80 70	100		dB
I_{os}	Output Short-circuit Current T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	10 10	23	40 40	mA
± V_{opp}	Output Voltage Swing T_{amb} = 25°C R_L = 2kΩ $T_{min.} \leq T_{amb} \leq T_{max.}$ R_L = 2kΩ V_{CC} = ±4V, R_L = 2kΩ, T_{amb} = 25°C V_{CC} = ±6V, R_L = 600Ω, T_{amb} = 25°C	13 12 2.8 4.6	14 3		V
SR	Slew-rate (V_I = ±10V, R_L = 2 kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)	0.6	1		V/µs
GBP	Gain Bandwidth Product (f = 100kHz, T_{amb} = 25°C, V_{in} = 10mV, R_L = 2kΩ, C_L = 100pF)	1.5	2		MHz
R_i	Input Resistance		1		MΩ
THD	Total Harmonic Distortion (f = 1kHz, A_v = 20dB, R_L = 2kΩ C_L = 100pF, T_{amb} = 25°C, V_o = $2V_{pp}$)		0.008	0.05	%
e_n	Equivalent Input Noise Voltage (f = 1kHz) R_S = 50Ω R_S = 1kΩ R_S = 10kΩ		8 10 18	15	$\frac{nV}{\sqrt{Hz}}$
V_{OPP}	Large Signal Voltage Swing R_L =10kΩ, f = 10kHz	26	28		V
∅m	Phase Margin		45		Degrees
V_{o1}/V_{o2}	Channel Separation	100	120		dB

4033-03.TBL



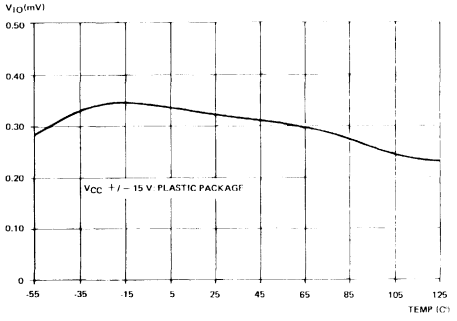
SUPPLY CURRENT VS. AMBIENT TEMPERATURE

4033-03.EPS



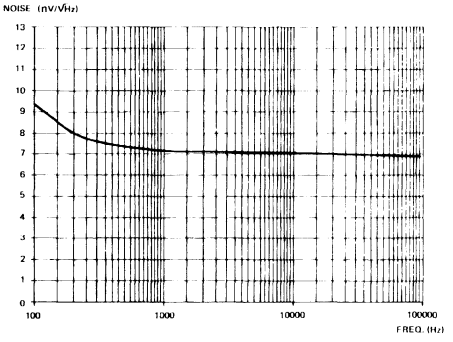
SUPPLY CURRENT VS. SUPPLY VOLTAGE

4033-04.EPS



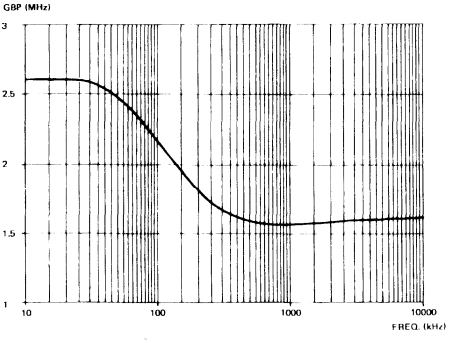
OFFSET VOLTAGE VS. AMBIENT TEMPERATURE

4033-05.EPS



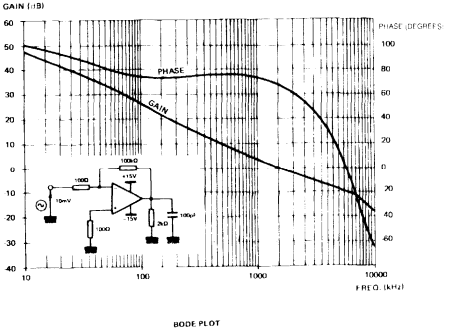
TOTAL INPUT NOISE VS. FREQUENCY

4033-06.EPS



GAIN BANDWIDTH PRODUCT VS. FREQUENCY

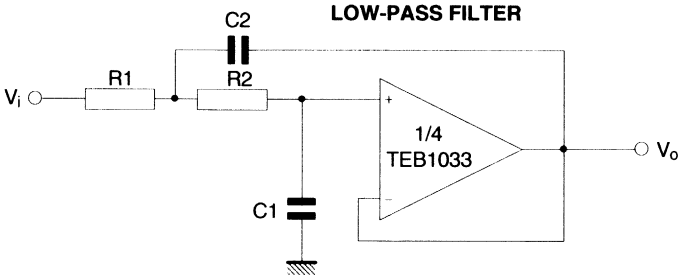
4033-07.EPS



BODE PLOT

4033-08.EPS

TYPICAL APPLICATION



$$\frac{V_o}{V_i} = \frac{1}{1 + 2\xi \frac{S}{\omega_c} + \frac{S^2}{\omega_c^2}}$$

$\varpi_C = 2\pi f_C$, with f_C = cutt-off frequency
ξ = damping factor

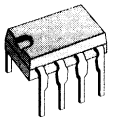
4033-09.EPS

SGS-THOMSON MICROELECTRONICS

TL061
TL061A - TL061B

LOW POWER SINGLE J-FET OPERATIONAL AMPLIFIERS

- VERY LOW POWER CONSUMPTION :
- WIDE COMMON-MODE (UP TO V_{CC}^+) AND DIFFERENTIAL VOLTAGE RANGES
- LOW INPUT BIAS AND OFFSET CURRENTS
- TYPICAL SUPPLY CURRENT : 200µA
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J-FET INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : 3.5V/µs (TYP)



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

H
TO99
(Metal Can)

DESCRIPTION

The TL061, TL061A and TL061B are high speed J-FET input single operational amplifier family. Each of these J-FET input operational amplifiers incorporates well matched, high voltage J-FET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.

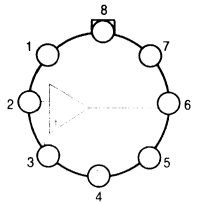
ORDER CODES

Part Number	Temperature Range	Package		
		H	N	D
TL061M/AM/BM	-55°C, +125°C	●	●	●
TL061I/AI/BI	-40°C, +105°C	●	●	●
TL061C/AC/BC	0°C, +70°C	●	●	●
Examples : TL061MH, TL061IN				

061-01.TBL

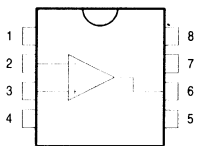
PIN CONNECTIONS (top views)

TO99



061-01.EPS

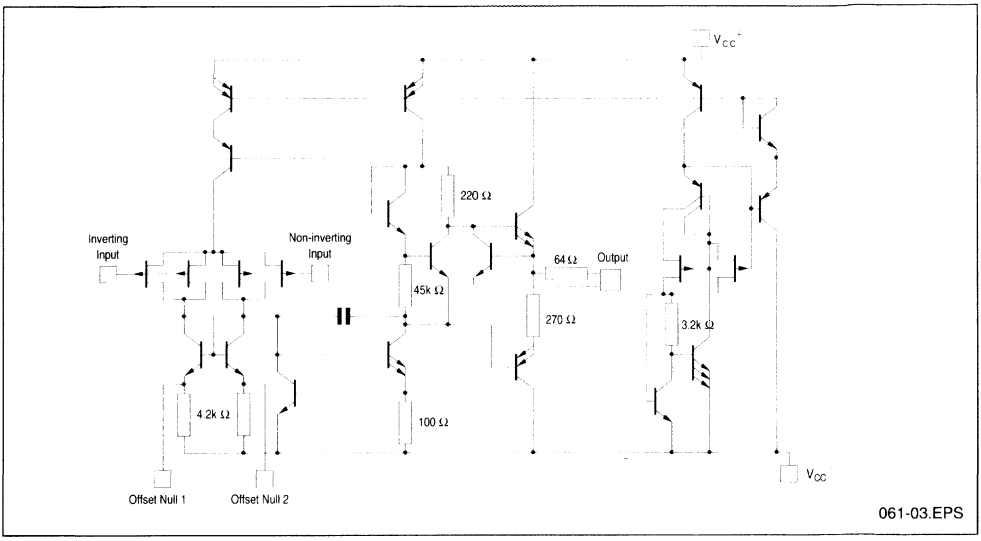
DIP8/SO8



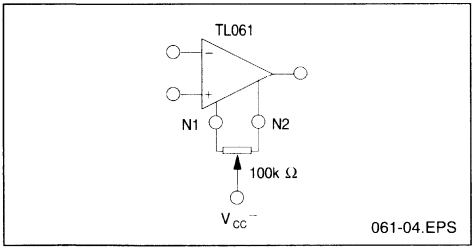
061-02.EPS

1 - Offset Null 1
2 - Inverting input
3 - Non-inverting input
4 - V_{CC}^-
5 - Offset Null 2
6 - Output
7 - V_{CC}^+
8 - N.C.

SCHEMATIC DIAGRAM



INPUT OFFSET VOLTAGE NULL CIRCUIT



MAXIMUM RATINGS

Symbol	Parameter	TL061M,AM,BM	TL061I,AI,BI	TL061C,AC,BC	Unit
V_{CC}	Supply Voltage - (note 1)	±18	±18	±18	V
V_i	Input Voltage - (note 3)	±15	±15	±15	V
V_{id}	Differential Input Voltage - (note 2)	±30	±30	±30	V
P_{tot}	Power Dissipation	680	680	680	mW
	Output Short-Circuit Duration (Note 4)	Infinite	Infinite	Infinite	
T_{oper}	Operating Free-Air Temperature Range	-55 to +125	-40 to +105	0 to +70	°C
T_{stg}	Storage Temperature Range	- 65 to + 150	- 65 to + 150	- 65 to + 150	°C

061-02.TBL

Notes :
1. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

ELECTRICAL CHARACTERISTICS

$V_{CC} = \pm 15V$, $T_{amb} = 25°C$ (unless otherwise specified)

Symbol	Parameter	TL061M			TL061I			TL061C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage ($R_s = 50\Omega$) $T_{amb} = 25°C$ $T_{min.} \le T_{amb} \le T_{max.}$		3	6 9		3	6 9		3	15 20	mV
DV_{io}	Temperature Coefficient of Input Offset Voltage ($R_s = 50\Omega$)		10			10			10		µV/°C
I_{io}	Input Offset Current * $T_{amb} = 25°C$ $T_{min.} \le T_{amb} \le T_{max.}$		5	100 20		5	100 10		5	200 5	pA nA
I_{ib}	Input Bias Current * $T_{amb} = 25°C$ $T_{min.} \le T_{amb} \le T_{max.}$		30	200 50		30	200 20		30	400 10	pA nA
V_{icm}	Input Common Mode Voltage Range	±11.5	+15 -12		±11.5	+15 -12		±11	+15 -12		V
V_{OPP}	Output Voltage Swing ($R_L = 10k\Omega$) $T_{amb} = 25°C$ $T_{min.} \le T_{amb} \le T_{max.}$	20 20	27		20 27	27		20 20	27		V
A_{vd}	Large Signal Voltage Gain ($R_L = 10k\Omega$, $V_o = \pm 10V$) $T_{amb} = 25°C$ $T_{min.} \le T_{amb} \le T_{max.}$	4 4	6		4 4	6		3 3	6		V/mV
GBP	Gain Bandwidth Product ($T_{amb} = 25°C$, $R_L = 10k\Omega$, $C_L = 100pF$)		1			1			1		MHz
R_i	Input Resistance		10^{12}			10^{12}			10^{12}		Ω
CMR	Common Mode Rejection Ratio ($R_s = 50\Omega$)	80	86		80	86		70	76		dB
SVR	Supply Voltage Rejection Ratio ($R_s = 50\Omega$)	80	95		80	95		70	95		dB
I_{cc}	Supply Current ($T_{amb} = 25°C$, no load, no signal)		200	250		200	250		200	250	µA
P_D	Total Power Consumption ($T_{amb} = 25°C$, no load, no signal)		6	7.5		6	7.5		6	7.5	mW

061-03.TBL

* The input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

ELECTRICAL CHARACTERISTICS (continued)

$V_{CC} = \pm 15V$, $T_{amb} = 25°C$

Symbol	Parameter	TL061C,I,M			Unit
		Min.	Max.	Typ.	
SR	Slew Rate ($V_i = 10V$, $R_L = 10k\Omega$, $C_L = 100pF$, $A_V = 1$)	1.5	3.5		V/µs
t_r	Rise Time ($V_i = 20mV$, $R_L = 10k\Omega$, $C_L = 100pF$, $A_V = 1$)		0.2		µs
K_{OV}	Overshoot Factor ($V_i = 20mV$, $R_L = 10k\Omega$, $C_L = 100pF$, $A_V = 1$) (see figure 1)		10		%
e_n	Equivalent Input Noise Voltage ($R_s = 100\Omega$, f = 1KHz)		42		$\frac{nV}{\sqrt{Hz}}$

061-04.TBL

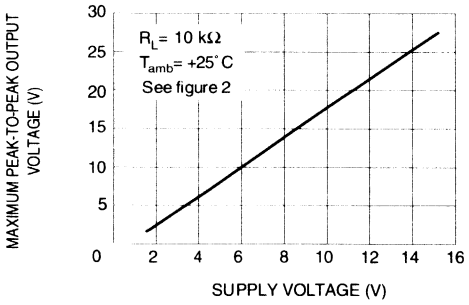
ELECTRICAL CHARACTERISTICS (continued)
$V_{CC} = \pm 15V$, $T_{amb} = 25°C$ (unless otherwise specified)

Symbol	Parameter	TL061AC,AI,AM			TL061BC,BI,BM			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage ($R_s = 50\Omega$) $T_{amb} = 25°C$ $T_{min.} \le T_{amb} \le T_{max.}$		3	6 7.5		2	3 5	mV
DV_{io}	Temperature Coefficient of Input Offset Voltage ($R_s = 50\Omega$)		10			10		µV/°C
I_{io}	Input Offset Current * $T_{amb} = 25°C$ $T_{min.} \le T_{amb} \le T_{max.}$		5	100 3		5	100 3	pA nA
I_{ib}	Input Bias Current * $T_{amb} = 25°C$ $T_{min.} \le T_{amb} \le T_{max.}$		30	200 7		30	200 7	pA nA
V_{icm}	Input Common Mode Voltage Range	±11.5	+15 -12		±11.5	+15 -12		V
V_{OPP}	Output Voltage Swing ($R_L = 10k\Omega$) $T_{amb} = 25°C$ $T_{min.} \le T_{amb} \le T_{max.}$	20 20	27		20 27	27		V
A_{vd}	Large Signal Voltage Gain ($R_L = 10k\Omega$, $V_o = \pm 10V$) $T_{amb} = 25°C$ $T_{min.} \le T_{amb} \le T_{max.}$	4 4	6		4 4	6		V/mV
GBP	Gain Bandwidth Product ($T_{amb} = 25°C$, $R_L = 10k\Omega$, $C_L = 100pF$)		1			1		MHz
R_i	Input Resistance		10^{12}			10^{12}		Ω
CMR	Common Mode Rejection Ratio ($R_s = 50\Omega$, $T_{amb} = 25°C$)	80	86		80	86		dB
SVR	Supply Voltage Rejection Ratio ($R_s = 50\Omega$, $T_{amb} = 25°C$)	80	95		80	95		dB
I_{cc}	Supply Current, no Load ($T_{amb} = 25°C$, no load, no signal)		200	250		200	250	µA
P_D	Total Power Consumption ($T_{amb} = 25°C$, no load, no signal)		6	7.5		6	7.5	mW
SR	Slew Rate ($V_i = 10V$, $R_L = 10k\Omega$, $C_L = 100pF$, $A_V = 1$)	1.5	3.5		1.5	3.5		V/µs
t_r	Rise Time ($V_i = 20mV$, $R_L = 10k\Omega$, $C_L = 100pF$, $A_V = 1$)		0.2			0.2		µs
K_{OV}	Overshoot Factor ($V_i = 20mV$, $R_L = 10k\Omega$, $C_L = 100pF$, $A_V = 1$) - (see figure 1)		10			10		%
e_n	Equivalent Input Noise Voltage ($R_s = 100\Omega$, f = 1KHz)		42			42		$\frac{nV}{\sqrt{Hz}}$

061-05.TBL

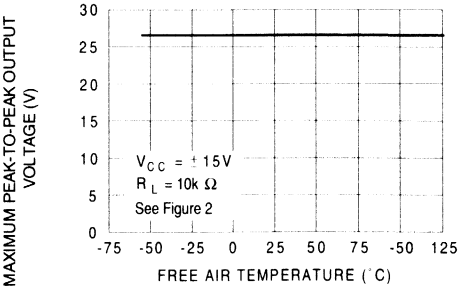
* The input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS SUPPLY VOLTAGE



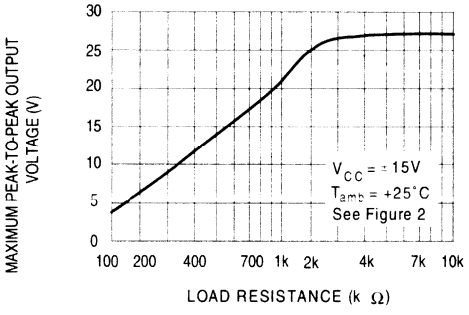
061-05.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREE AIR TEMP.



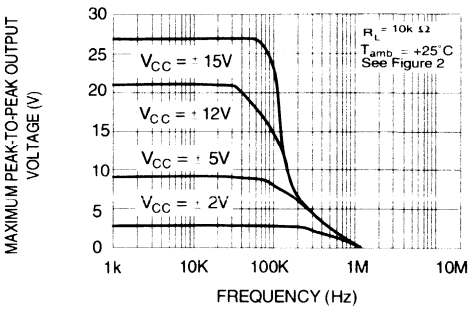
061-06.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS LOAD RESISTANCE



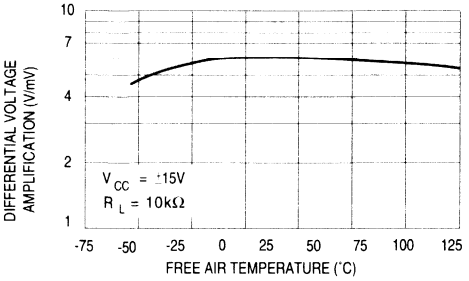
061-07.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



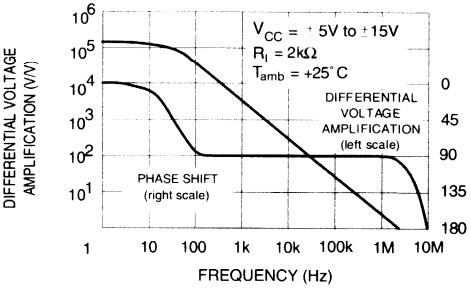
061-08.EPS

DIFFERENTIAL VOLTAGE AMPLIFICATION VERSUS FREE AIR TEMPERATURE



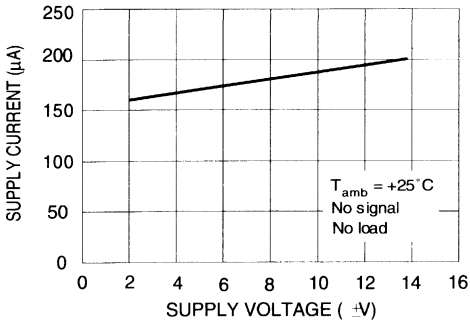
061-09.EPS

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT VERSUS FREQUENCY



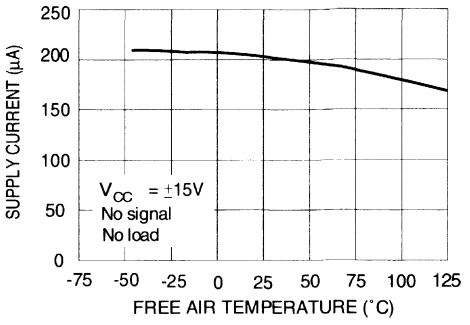
061-10.EPS

SUPPLY CURRENT PER AMPLIFIER VERSUS SUPPLY VOLTAGE



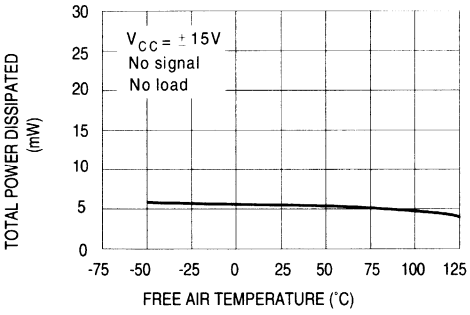
061-11.EPS

SUPPLY CURRENT PER AMPLIFIER VERSUS FREE AIR TEMPERATURE



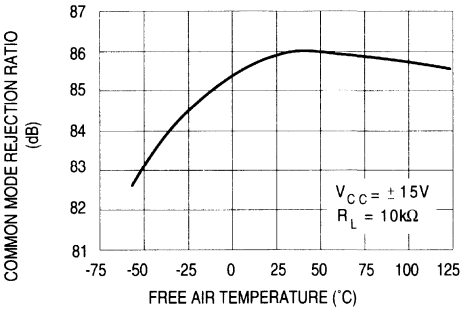
061-12.EPS

TOTAL POWER DISSIPATED VERSUS FREE AIR TEMPERATURE



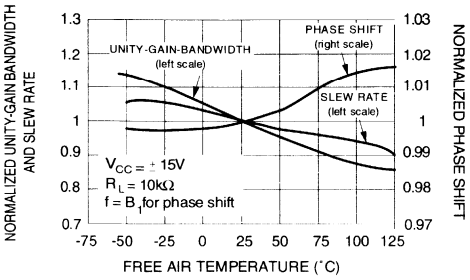
061-13.EPS

COMMON MODE REJECTION RATIO VERSUS FREE AIR TEMPERATURE



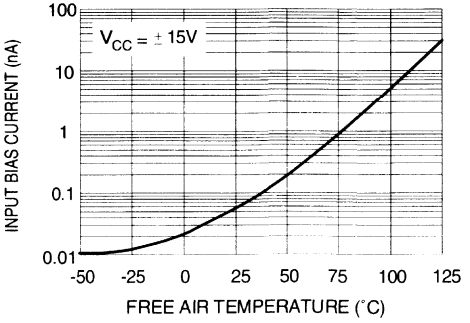
061-14.EPS

NORMALIZED UNITY GAIN BANDWIDTH SLEW RATE, AND PHASE SHIFT VERSUS TEMPERATURE



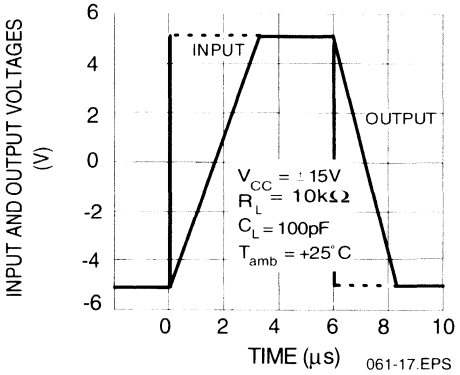
061-15.EPS

INPUT BIAS CURRENT VERSUS FREE AIR TEMPERATURE

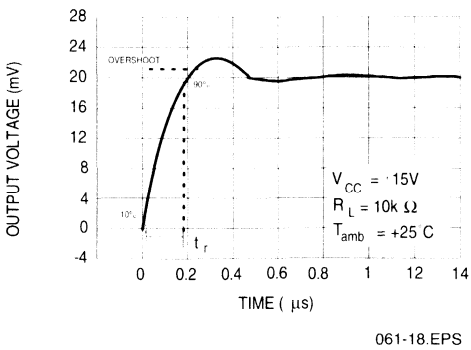


061-16.EPS

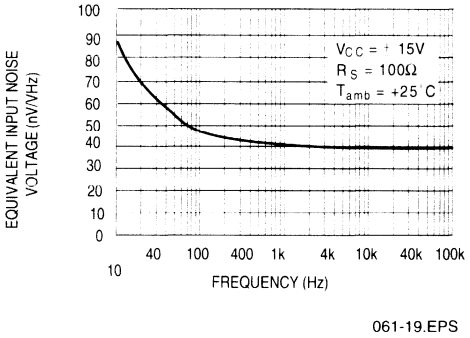
VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



OUTPUT VOLTAGE VERSUS ELAPSED TIME



EQUIVALENT INPUT NOISE VOLTAGE VERSUS FREQUENCY



PARAMETER MEASUREMENT INFORMATION

Figure 1 : Voltage follower

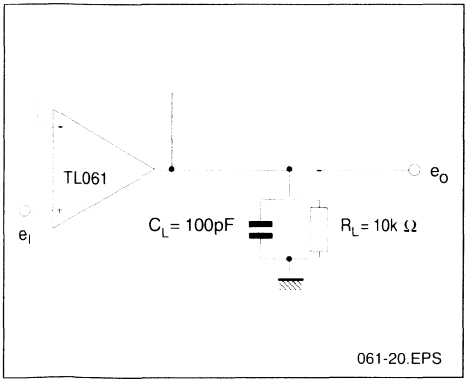
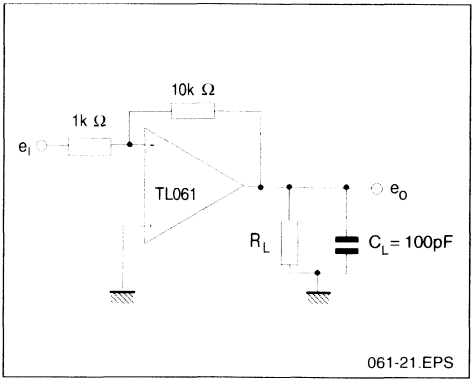


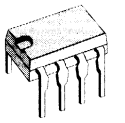
Figure 2 : Gain-of-10 inverting amplifier



TL062
TL062A - TL062B

LOW POWER DUAL J-FET OPERATIONAL AMPLIFIERS

- VERY LOW POWER CONSUMPTION :
- WIDE COMMON-MODE (UP TO V_{CC}^+) AND DIFFERENTIAL VOLTAGE RANGES
- LOW INPUT BIAS AND OFFSET CURRENTS
- TYPICAL SUPPLY CURRENT : 200µA
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J-FET INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : 3.5V/µs (TYP)



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

H
TO99
(Metal Can)

DESCRIPTION

The TL062, TL062A and TL062B are high speed J-FET input dual operational amplifier family. Each of these J-FET input operational amplifiers incorporates well matched, high voltage J-FET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.

ORDER CODES

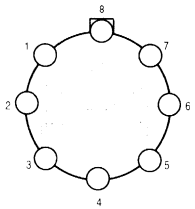
Part Number	Temperature Range	Package		
		H	N	D
TL062M/AM/BM	-55°C, +125°C	•	•	•
TL062I/AI/BI	-40°C, +105°C	•	•	•
TL062C/AC/BC	0°C, +70°C	•	•	•

Examples : TL062MH, TL062IN

062-01.TBL

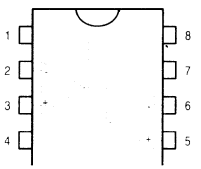
PIN CONNECTIONS (top views)

TO99



062-01.EPS

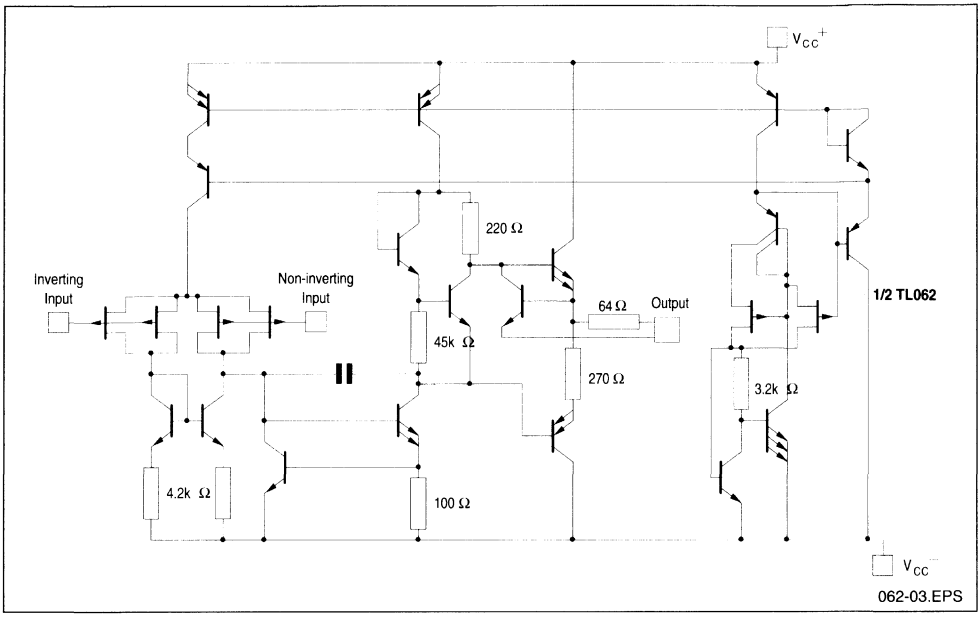
DIP8/SO8



062-02.EPS

1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^-
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - V_{CC}^+

SCHEMATIC DIAGRAM



MAXIMUM RATINGS

Symbol	Parameter	TL062M,AM,BM	TL062I,AI,BI	TL062C,AC,BC	Unit
V_{CC}	Supply Voltage - (note 1)	±18	±18	±18	V
V_i	Input Voltage - (note 3)	±15	±15	±15	V
V_{id}	Differential Input Voltage - (note 2)	±30	±30	±30	V
P_{tot}	Power Dissipation	680	680	680	mW
	Output Short-Circuit Duration (Note 4)	Infinite	Infinite	Infinite	
T_{oper}	Operating Free-Air Temperature Range	-55 to +125	-40 to +105	0 to +70	°C
T_{stg}	Storage Temperature Range	- 65 to + 150	- 65 to + 150	- 65 to + 150	°C

Notes : 1. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.
2. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

ELECTRICAL CHARACTERISTICS

$V_{CC} = \pm 15V$, $T_{amb} = 25°C$ (unless otherwise specified)

Symbol	Parameter	TL062M			TL062I			TL062C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage ($R_s = 50\Omega$) $T_{amb} = 25°C$ $T_{min.} \le T_{amb} \le T_{max.}$		3	6 15		3	6 9		3	15 20	mV
DV_{io}	Temperature Coefficient of Input Offset Voltage ($R_s = 50\Omega$)		10			10			10		µV/°C
I_{io}	Input Offset Current * $T_{amb} = 25°C$ $T_{min.} \le T_{amb} \le T_{max.}$		5	100 20		5	100 10		5	200 5	pA nA
I_{ib}	Input Bias Current * $T_{amb} = 25°C$ $T_{min.} \le T_{amb} \le T_{max.}$		30	200 50		30	200 20		30	400 10	pA nA
V_{icm}	Input Common Mode Voltage Range	±11.5	+15 -12		±11.5	+15 -12		±11	+15 -12		V
V_{OPP}	Output Voltage Swing ($R_L = 10k\Omega$) $T_{amb} = 25°C$ $T_{min.} \le T_{amb} \le T_{max.}$	20 20	27		20 20	27		20 20	27		V
A_{vd}	Large Signal Voltage Gain ($R_L = 10k\Omega$, $V_o = \pm 10V$) $T_{amb} = 25°C$ $T_{min.} \le T_{amb} \le T_{max.}$	4 4	6		4 4	6		3 3	6		V/mV
GBP	Gain Bandwidth Product ($T_{amb} = 25°C$, $R_L = 10k\Omega$ $C_L = 100pF$)		1			1			1		MHz
R_i	Input Resistance		10^{12}			10^{12}			10^{12}		Ω
CMR	Common Mode Rejection Ratio ($R_s = 50\Omega$)	80	86		80	86		70	76		dB
SVR	Supply Voltage Rejection Ratio ($R_s = 50\Omega$)	80	95		80	95		70	95		dB
I_{cc}	Supply Current (Per Amplifier) ($T_{amb} = 25°C$, no load, no signal)		200	250		200	250		200	250	µA
V_{O1}/V_{O2}	Channel Separation ($A_v = 100$, $T_{amb} = 25°C$)		120			120			120		dB
P_D	Total Power Consumption (Each Amplifier) ($T_{amb} = 25°C$, no load, no signal)		6	7.5		6	7.5		6	7.5	mW

062-03.TBL

* Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as closes to the ambient temperature as possible.

ELECTRICAL CHARACTERISTICS (continued)

$V_{CC} = \pm 15V$, $T_{amb} = 25°C$

Symbol	Parameter	TL062C,I,M			Unit
		Min.	Max.	Typ.	
SR	Slew Rate ($V_i = 10V$, $R_L = 10k\Omega$, $C_L = 100pF$, $A_V = 1$)	1.5	3.5		V/µs
t_r	Rise Time ($V_i = 20mV$, $R_L = 10k\Omega$, $C_L = 100pF$, $A_V = 1$)		0.2		µs
K_{OV}	Overshoot Factor ($V_i = 20mV$, $R_L = 10k\Omega$, $C_L = 100pF$, $A_V = 1$) (see figure 1)		10		%
e_n	Equivalent Input Noise Voltage ($R_s = 100\Omega$, f = 1KHz)		42		$\frac{nV}{\sqrt{Hz}}$

062-04.TBL

ELECTRICAL CHARACTERISTICS (continued)

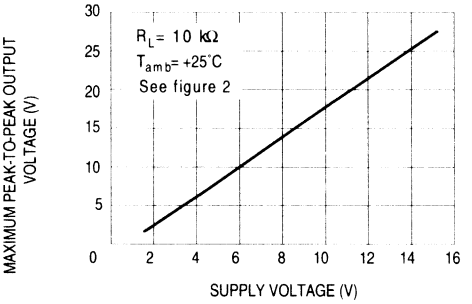
$V_{CC} = \pm 15V$, $T_{amb} = 25°C$ (unless otherwise specified)

Symbol	Parameter	TL062AC,AI, AM			TL062BC,BI,BM			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage ($R_s = 50\Omega$) $T_{amb} = 25°C$ $T_{min.} \le T_{amb} \le T_{max.}$		3	6 7.5		2	3 5	mV
DV_{io}	Temperature Coefficient of Input Offset Voltage ($R_s = 50\Omega$)		10			10		µV/°C
I_{io}	Input Offset Current * $T_{amb} = 25°C$ $T_{min.} \le T_{amb} \le T_{max.}$		5	100 3		5	100 3	pA nA
I_{ib}	Input Bias Current * $T_{amb} = 25°C$ $T_{min.} \le T_{amb} \le T_{max.}$		30	200 7		30	200 7	pA nA
V_{icm}	Input Common Mode Voltage Range	±11.5	+15 -12		±11.5	+15 -12		V
V_{OPP}	Output Voltage Swing ($R_L = 10k\Omega$) $T_{amb} = 25°C$ $T_{min.} \le T_{amb} \le T_{max.}$	20 20	27		20 20	27		V
A_{vd}	Large Signal Voltage Gain ($R_L = 10k\Omega$, $V_o = \pm 10V$) $T_{amb} = 25°C$ $T_{min.} \le T_{amb} \le T_{max.}$	4 4	6		4 4	6		V/mV
GBP	Gain Bandwidth Product ($T_{amb} = 25°C$, $R_L = 10k\Omega$, $C_L = 100pF$)		1			1		MHz
R_i	Input Resistance		10^{12}			10^{12}		Ω
CMR	Common Mode Rejection Ratio ($R_s = 50\Omega$)	80	86		80	86		dB
SVR	Supply Voltage Rejection Ratio ($R_s = 50\Omega$)	80	95		80	95		dB
I_{cc}	Supply Current (Per Amplifier) ($T_{amb} = 25°C$, no load, no signal)		200	250		200	250	µA
V_{O1}/V_{O2}	Channel Separation ($A_v = 100$, $T_{amb} = 25°C$)		120			120		
P_D	Total Power Consumption (Each Amplifier) ($T_{amb} = 25°C$, no load, no signal)		6	7.5		6	7.5	mW
SR	Slew Rate ($V_i = 10V$, $R_L = 10k\Omega$, $C_L = 100pF$, $A_V = 1$)	1.5	3.5		1.5	3.5		V/µs
t_r	Rise Time ($V_i = 20mV$, $R_L = 10k\Omega$, $C_L = 100pF$, $A_V = 1$)		0.2			0.2		µs
K_{OV}	Overshoot Factor ($V_i = 20mV$, $R_L = 10k\Omega$, $C_L = 100pF$, $A_V = 1$) - (see figure 1)		10			10		%
e_n	Equivalent Input Noise Voltage ($R_s = 100\Omega$, f = 1KHz)		42			42		$\frac{nV}{\sqrt{Hz}}$

* The input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

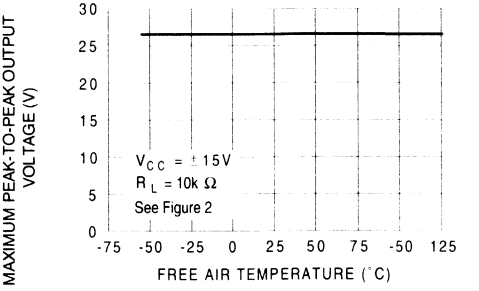
062-05 TRI

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS SUPPLY VOLTAGE



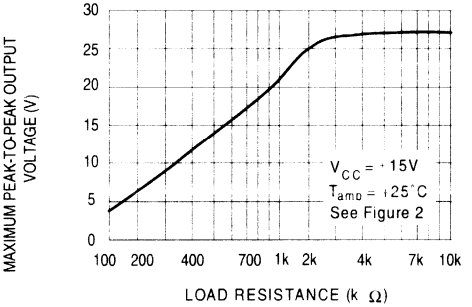
062-04.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREE AIR TEMP.



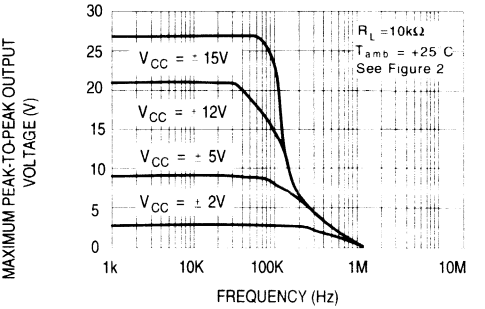
062-05.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS LOAD RESISTANCE



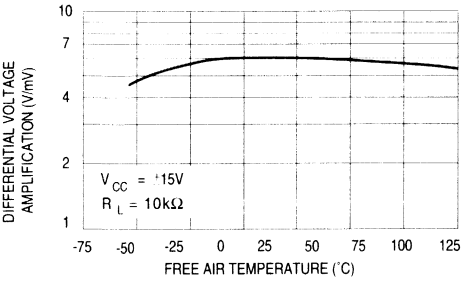
062-06.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



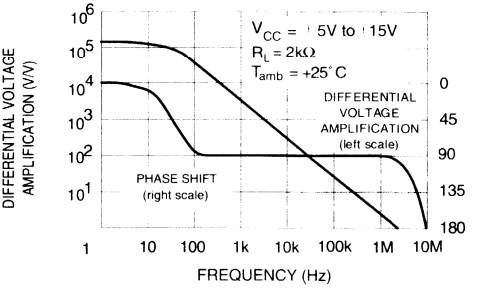
062-07.EPS

DIFFERENTIAL VOLTAGE AMPLIFICATION VERSUS FREE AIR TEMPERATURE



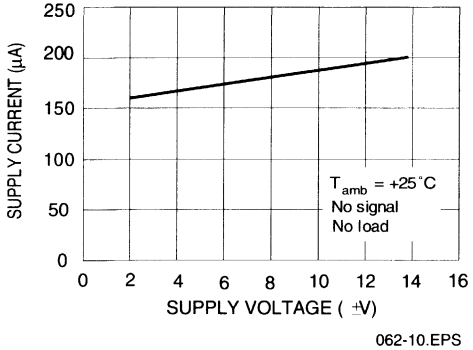
062-08.EPS

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT VERSUS FREQUENCY



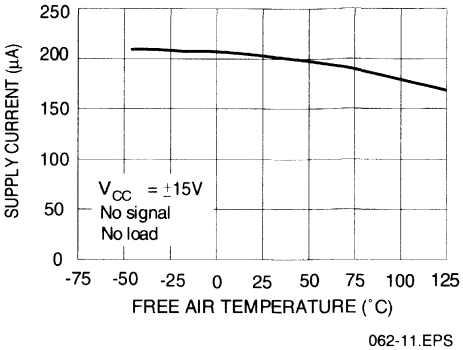
062-09.EPS

SUPPLY CURRENT PER AMPLIFIER VERSUS SUPPLY VOLTAGE



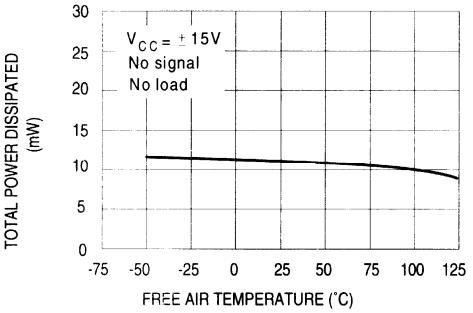
062-10.EPS

SUPPLY CURRENT PER AMPLIFIER VERSUS FREE AIR TEMPERATURE



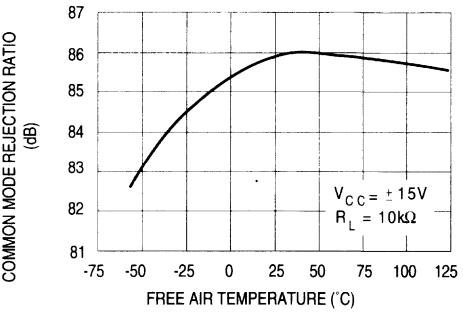
062-11.EPS

TOTAL POWER DISSIPATED VERSUS FREE AIR TEMPERATURE



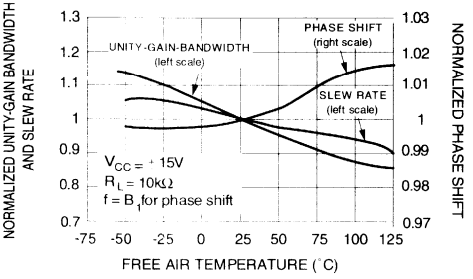
062-12.EPS

COMMON MODE REJECTION RATIO VERSUS FREE AIR TEMPERATURE



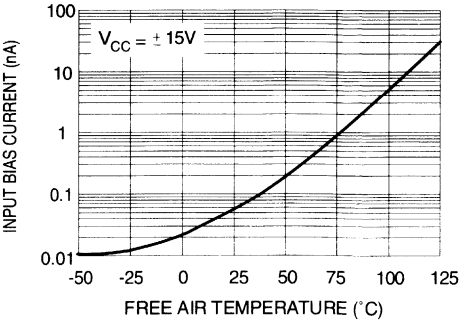
062-13.EPS

NORMALIZED UNITY GAIN BANDWIDTH SLEW RATE, AND PHASE SHIFT VERSUS TEMPERATURE



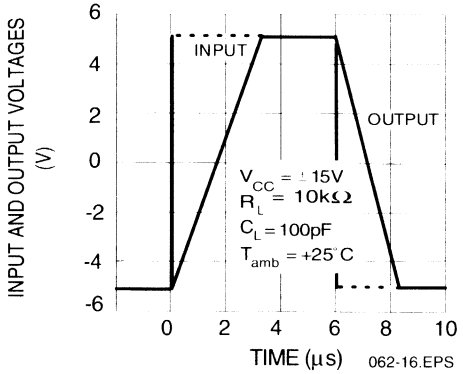
062-14.EPS

INPUT BIAS CURRENT VERSUS FREE AIR TEMPERATURE



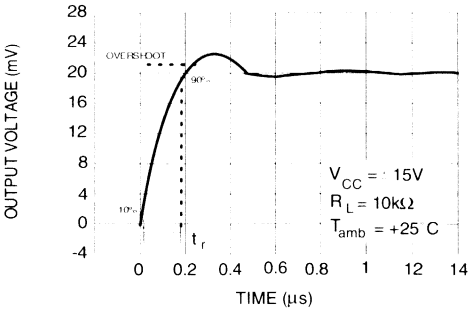
062-15.EPS

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



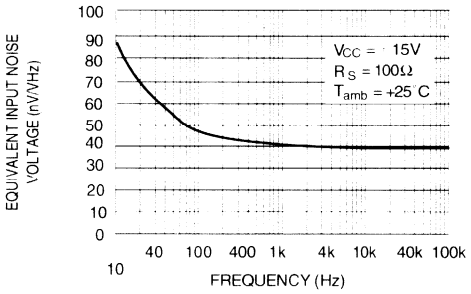
062-16.EPS

OUTPUT VOLTAGE VERSUS ELAPSED TIME



062-17.EPS

EQUIVALENT INPUT NOISE VOLTAGE VERSUS FREQUENCY



062-18.EPS

PARAMETER MEASUREMENT INFORMATION

Figure 1 : Voltage follower

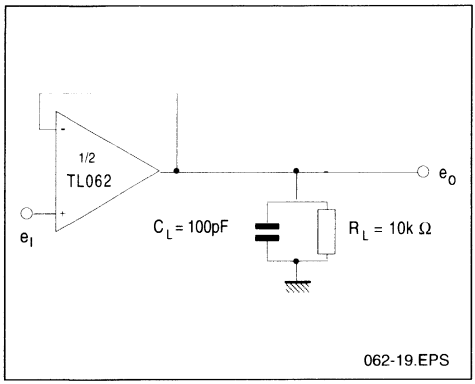
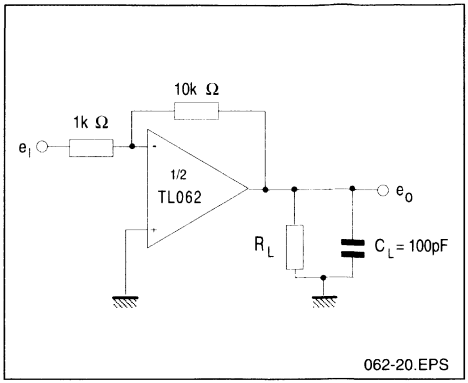
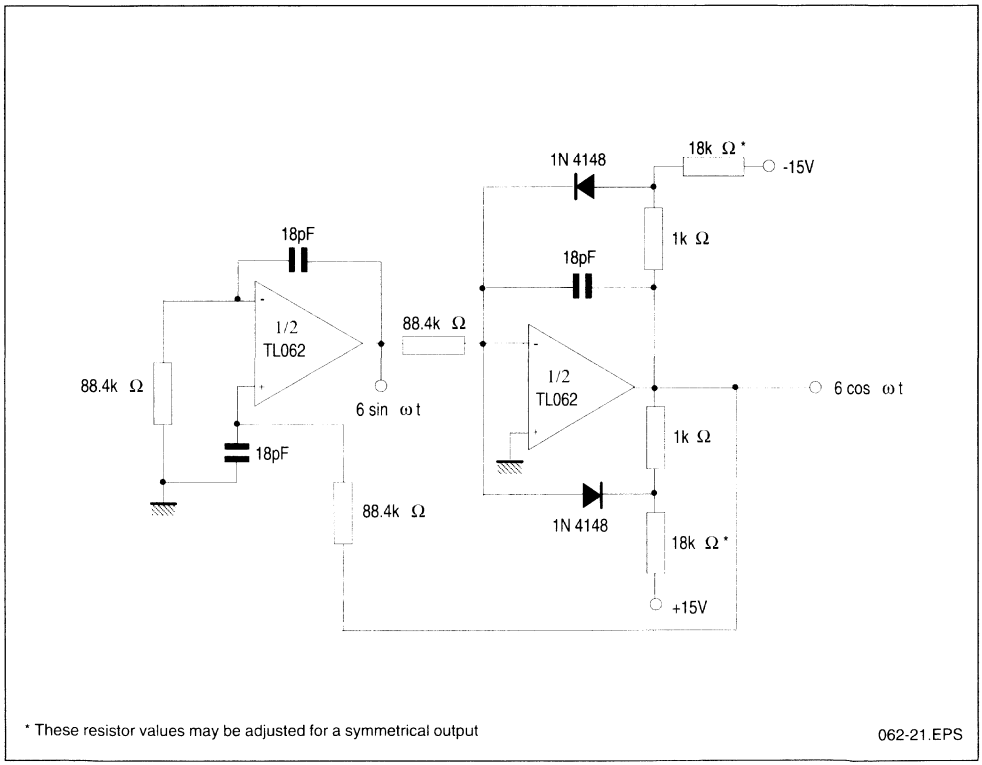


Figure 2 : Gain-of-10 inverting amplifier



TYPICAL APPLICATION

100KHz QUADRATURE OSCILLATOR

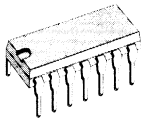


SGS-THOMSON MICROELECTRONICS

TL064
TL064A - TL064B

LOW POWER QUAD J-FET OPERATIONAL AMPLIFIERS

- VERY LOW POWER CONSUMPTION
- WIDE COMMON-MODE (UP TO V_{CC}^+) AND DIFFERENTIAL VOLTAGE RANGES
- LOW INPUT BIAS AND OFFSET CURRENTS
- TYPICAL SUPPLY CURRENT : 200µA
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J-FET INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : 3.5V/µs (TYP)



N
DIP14
(Plastic Package)

D
SO14
(Plastic Micropackage)

J
CERDIP14
(Cerdip Package)

DESCRIPTION

The TL064, TL064A and TL064B are high speed J-FET input quad operational amplifiers. Each of these J-FET input operational amplifiers incorporates well matched, high voltage J-FET and bipolar transistors in a monolithic integrated circuit.

The device features high slew rate, low input bias and offset currents, and low offset voltage temperature coefficient.

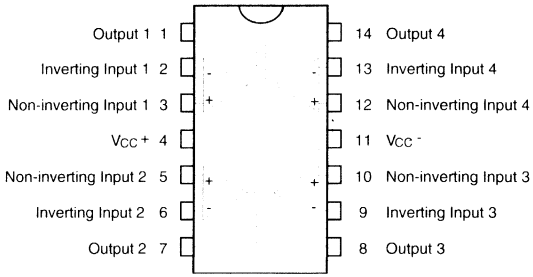
ORDER CODES

Part Number	Temperature Range	Package		
		N	J	D
TL064M/AM/BM	-55°C, +125°C	•	•	•
TL064I/AI/BI	-40°C, +105°C	•	•	•
TL064C/AC/BC	0°C, +70°C	•	•	•

Examples : TL064MJ, TL064IN

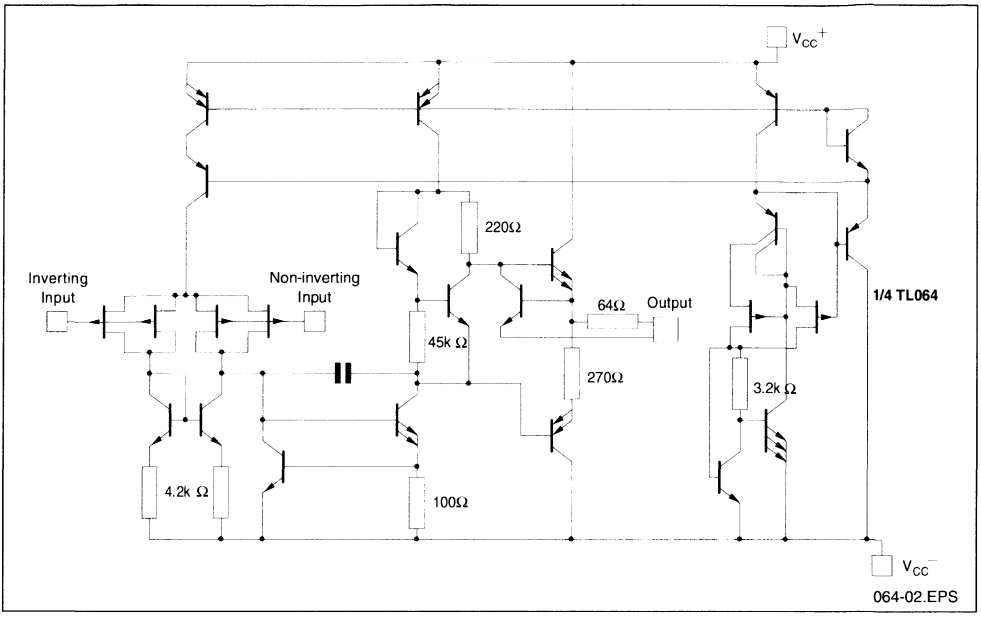
064-01.TBL

PIN CONNECTIONS (top view)



064-01.EPS

SCHEMATIC DIAGRAM



MAXIMUM RATINGS

Symbol	Parameter	TL064M,AM,BM	TL064I,AI,BI	TL064C,AC,BC	Unit
V_{CC}	Supply Voltage - (note 1)	±18	±18	±18	V
V_i	Input Voltage - (note 3)	±15	±15	±15	V
V_{id}	Differential Input Voltage - (note 2)	±30	±30	±30	V
P_{tot}	Power Dissipation	680	680	680	mW
	Output Short-Circuit Duration (Note 4)	Infinite	Infinite	Infinite	
T_{oper}	Operating Free-Air Temperature Range	-55 to +125	-40 to +105	0 to +70	°C
T_{stg}	Storage Temperature Range	-65 to +150	-65 to +150	-65 to +150	°C

064-02.TBL

Notes : 1. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

ELECTRICAL CHARACTERISTICS

$V_{CC} = \pm 15V$, $T_{amb} = 25°C$ (unless otherwise specified)

Symbol	Parameter	TL064M			TL064I			TL064C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage ($R_s = 50\Omega$) $T_{amb} = 25°C$ $T_{min.} \le T_{amb} \le T_{max.}$		3	6 15		3	6 9		3	15 20	mV
DV_{io}	Temperature Coefficient of Input Offset Voltage ($R_s = 50\Omega$)		10			10			10		µV/°C
I_{io}	Input Offset Current * $T_{amb} = 25°C$ $T_{min.} \le T_{amb} \le T_{max.}$		5	100 20		5	100 10		5	200 5	pA nA
I_{ib}	Input Bias Current * $T_{amb} = 25°C$ $T_{min.} \le T_{amb} \le T_{max.}$		30	200 50		30	200 20		30	400 10	pA nA
V_{icm}	Input Common Mode Voltage Range	±11.5	+15 -12		±11.5	+15 -12		±11	+15 -12		V
V_{OPP}	Output Voltage Swing ($R_L = 10k\Omega$) $T_{amb} = 25°C$ $T_{min.} \le T_{amb} \le T_{max.}$	20 20	27		20 27	27		20 20	27		V
A_{vd}	Large Signal Voltage Gain ($R_L = 10k\Omega$, $V_o = \pm 10V$) $T_{amb} = 25°C$ $T_{min.} \le T_{amb} \le T_{max.}$	4 4	6		4 4	6		3 3	6		V/mV
GBP	Gain Bandwidth Product ($T_{amb} = 25°C$, $R_L = 10k\Omega$ $C_L = 100pF$)		1			1			1		MHz
R_i	Input Resistance		10^{12}			10^{12}			10^{12}		Ω
CMR	Common Mode Rejection Ratio ($R_s = 50\Omega$)	80	86		80	86		70	76		dB
SVR	Supply Voltage Rejection Ratio ($R_s = 50\Omega$)	80	95		80	95		70	95		dB
I_{cc}	Supply Current (Per Amplifier) ($T_{amb} = 25°C$, no load, no signal)		200	250		200	250		200	250	µA
V_{O1}/V_{O2}	Channel Separation ($A_v = 100$, $T_{amb} = 25°C$)		120			120			120		dB
P_D	Total Power Consumption ($T_{amb} = 25°C$, no load, no signal)		6	7.5		6	7.5		6	7.5	mW

064-03.TBL

* The input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

ELECTRICAL CHARACTERISTICS (continued)

$V_{CC} = \pm 15V$, $T_{amb} = 25°C$

Symbol	Parameter	TL064C,I,M			Unit
		Min.	Max.	Typ.	
SR	Slew Rate ($V_i = 10V$, $R_L = 10k\Omega$, $C_L = 100pF$, $A_V = 1$)	1.5	3.5		V/µs
t_r	Rise Time ($V_i = 20mV$, $R_L = 10k\Omega$, $C_L = 100pF$, $A_V = 1$) (see Figure 1)		0.2		µs
K_{OV}	Overshoot Factor ($V_i = 20mV$, $R_L = 10k\Omega$, $C_L = 100pF$, $A_V = 1$) (see figure 1)		10		%
e_n	Equivalent Input Noise Voltage ($R_s = 100\Omega$, f = 1KHz)		42		$\frac{nV}{\sqrt{Hz}}$

064-04.TBL

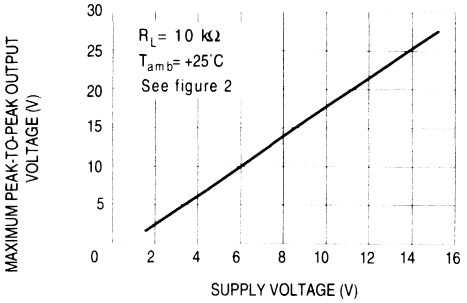
ELECTRICAL CHARACTERISTICS (continued)

$V_{CC} = \pm 15V$, $T_{amb} = 25°C$ (unless otherwise specified)

Symbol	Parameter	TL064AC,AI,AM			TL064BC,BI,BM			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage ($R_s = 50\Omega$) $T_{amb} = 25°C$ $T_{min.} \le T_{amb} \le T_{max.}$		3	6 7.5		2	3 5	mV
DV_{io}	Temperature Coefficient of Input Offset Voltage ($R_s = 50\Omega$)		10			10		µV/°C
I_{io}	Input Offset Current * $T_{amb} = 25°C$ $T_{min.} \le T_{amb} \le T_{max.}$		5	100 3		5	100 3	pA nA
I_{ib}	Input Bias Current * $T_{amb} = 25°C$ $T_{min.} \le T_{amb} \le T_{max.}$		30	200 7		30	200 7	pA nA
V_{icm}	Input Common Mode Voltage Range	±11.5	+15 -12		±11.5	+15 -12		V
V_{OPP}	Output Voltage Swing ($R_L = 10k\Omega$) $T_{amb} = 25°C$ $T_{min.} \le T_{amb} \le T_{max.}$	20 20	27		20 27	27		V
A_{vd}	Large Signal Voltage Gain ($R_L = 10k\Omega$, $V_o = \pm 10V$) $T_{amb} = 25°C$ $T_{min.} \le T_{amb} \le T_{max.}$	4 4	6		4 4	6		V/mV
GBP	Gain Bandwidth Product ($T_{amb} = 25°C$, $R_L = 10k\Omega$, $C_L = 100pF$)		1			1		MHz
R_i	Input Resistance		10^{12}			10^{12}		Ω
CMR	Common Mode Rejection Ratio ($R_s = 50\Omega$)	80	86		80	86		dB
SVR	Supply Voltage Rejection Ratio ($R_s = 50\Omega$)	80	95		80	95		dB
I_{cc}	Supply Current (Per Amplifier) ($T_{amb} = 25°C$, no load, no signal)		200	250		200	250	µA
V_{O1}/V_{O2}	Channel Separation ($A_v = 100$, $T_{amb} = 25°C$)		120			120		dB
P_D	Total Power Consumption (Each Amplifier) ($T_{amb} = 25°C$, no load, no signal)		6	7.5		6	7.5	mW
SR	Slew Rate ($V_i = 10V$, $R_L = 10k\Omega$, $C_L = 100pF$, $A_V = 1$)	1.5	3.5		1.5	3.5		V/µs
t_r	Rise Time ($V_i = 20mV$, $R_L = 10k\Omega$, $C_L = 100pF$, $A_V = 1$)		0.2			0.2		µs
K_{OV}	Overshoot Factor ($V_i = 20mV$, $R_L = 10k\Omega$, $C_L = 100pF$, $A_V = 1$) - (see figure 1)		10			10		%
e_n	Equivalent Input Noise Voltage ($R_s = 100\Omega$, f = 1KHz)		42			42		$\frac{nV}{\sqrt{Hz}}$

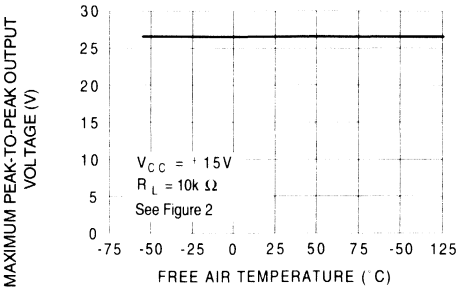
* The input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS SUPPLY VOLTAGE



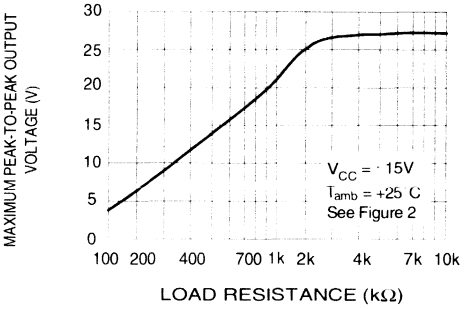
064-03.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREE AIR TEMP.



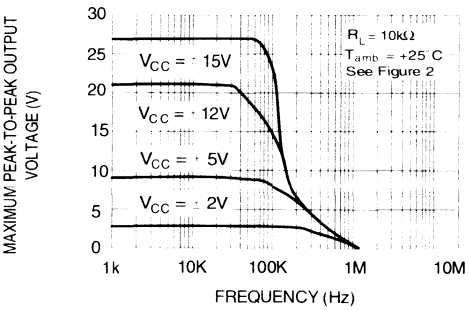
064-04.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS LOAD RESISTANCE



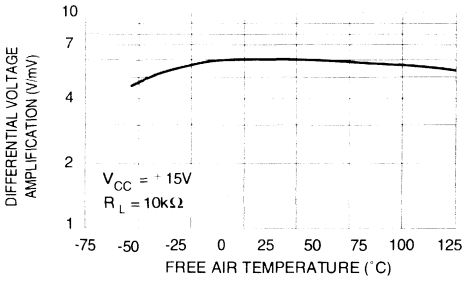
064-05.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



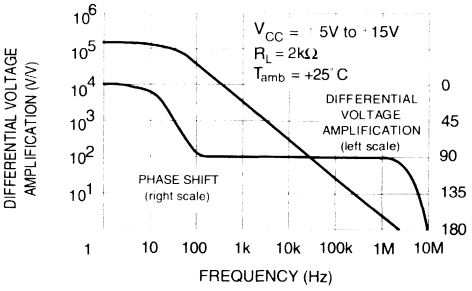
064-06.EPS

DIFFERENTIAL VOLTAGE AMPLIFICATION VERSUS FREE AIR TEMPERATURE



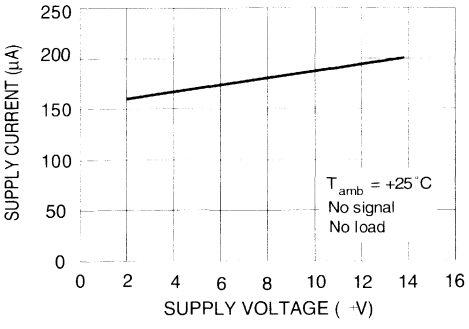
064-07.EPS

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT VERSUS FREQUENCY



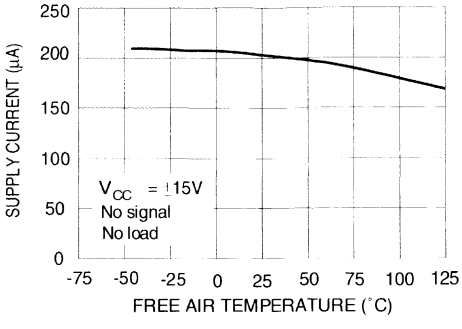
064-08.EPS

SUPPLY CURRENT PER AMPLIFIER VERSUS SUPPLY VOLTAGE



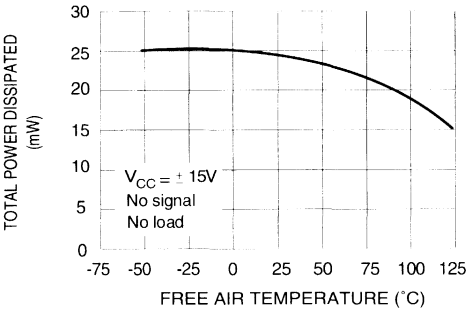
064-09.EPS

SUPPLY CURRENT PER AMPLIFIER VERSUS FREE AIR TEMPERATURE



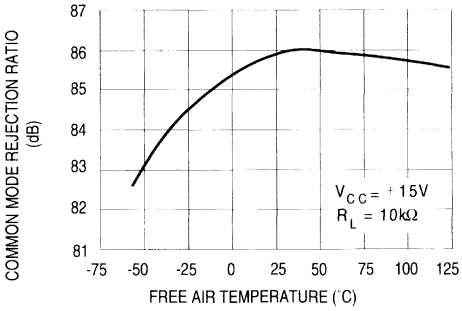
064-10.EPS

TOTAL POWER DISSIPATED VERSUS FREE AIR TEMPERATURE



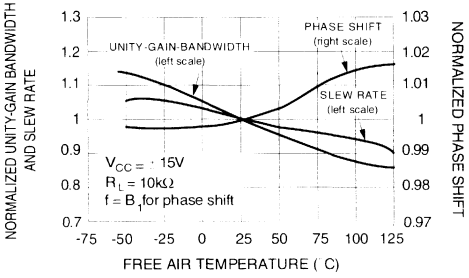
064-11.EPS

COMMON MODE REJECTION RATIO VERSUS FREE AIR TEMPERATURE



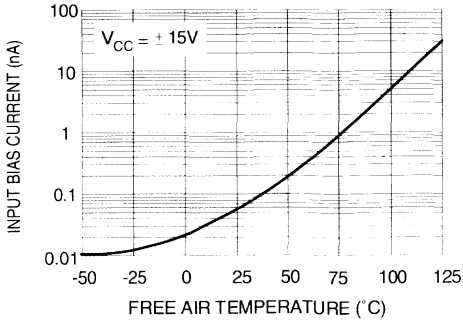
064-12.EPS

NORMALIZED UNITY GAIN BANDWIDTH SLEW RATE, AND PHASE SHIFT VERSUS TEMPERATURE



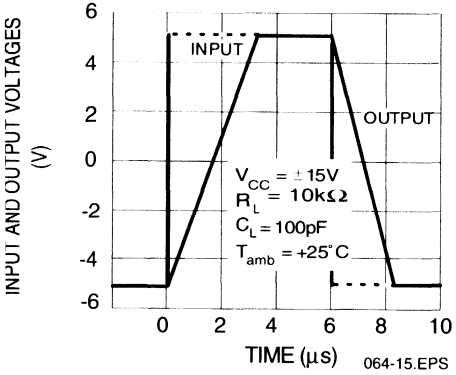
064-13.EPS

INPUT BIAS CURRENT VERSUS FREE AIR TEMPERATURE



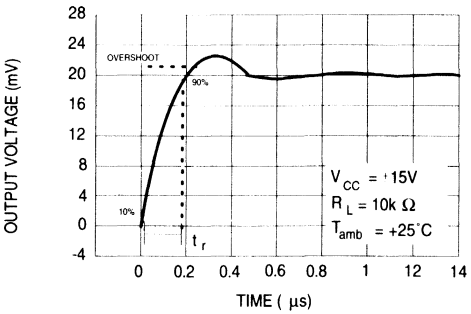
064-14.EPS

VOLTAGE FOLLOWER LARGE SIGNAL RESPONSE



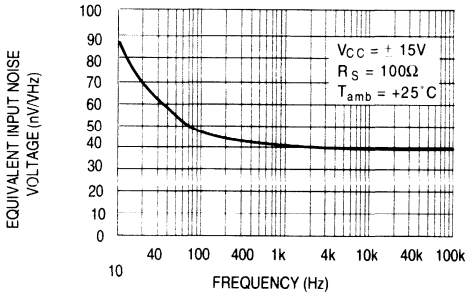
064-15.EPS

OUTPUT VOLTAGE VERSUS ELAPSED TIME



064-16.EPS

EQUIVALENT INPUT NOISE VOLTAGE VERSUS FREQUENCY



064-17.EPS

PARAMETER MEASUREMENT INFORMATION

Figure 1 : Voltage follower

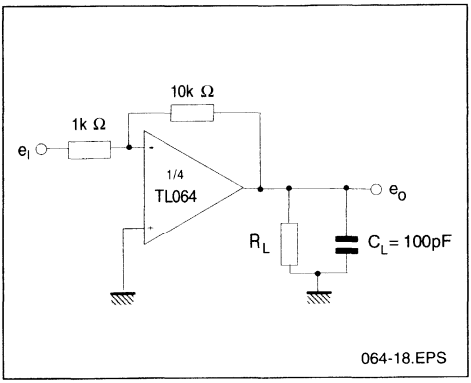
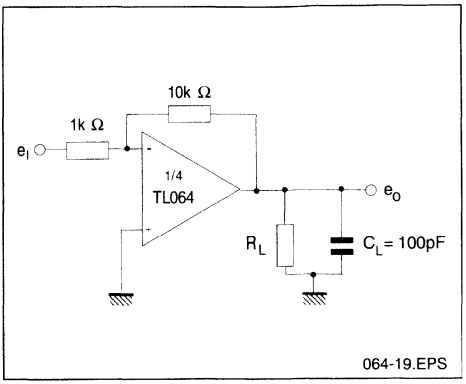
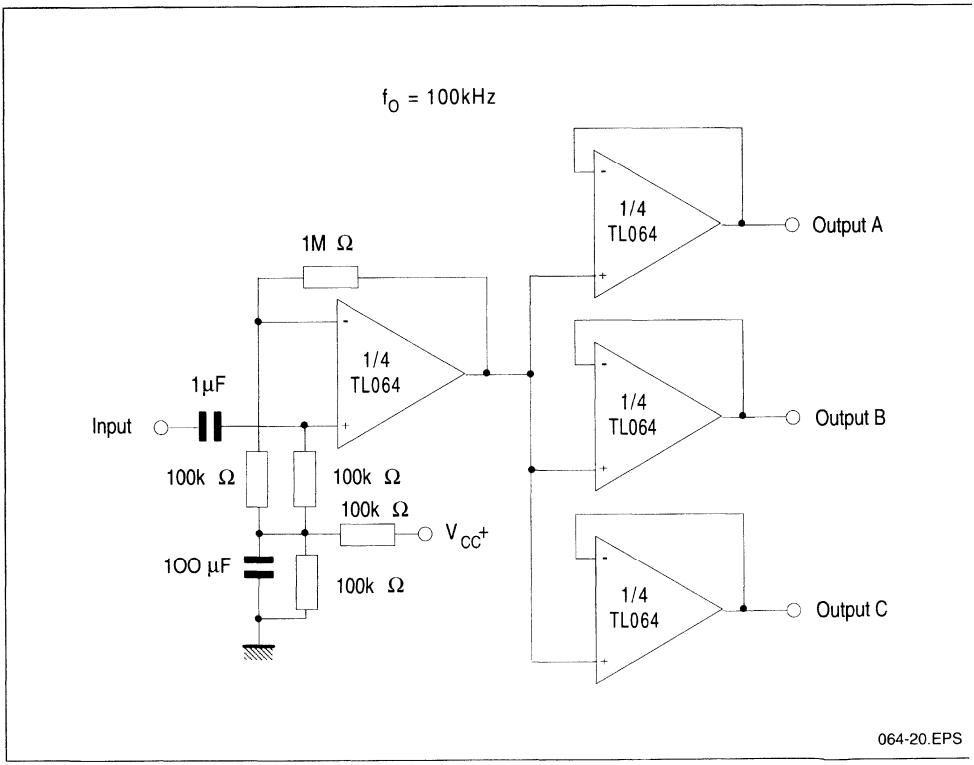


Figure 2 : Gain-of-10 inverting amplifier



TYPICAL APPLICATION

AUDIO DISTRIBUTION AMPLIFIER

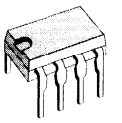


SGS-THOMSON MICROELECTRONICS

TL071
TL071A - TL071B

LOW NOISE SINGLE J-FET OPERATIONAL AMPLIFIERS

- LOW POWER CONSUMPTION
- WIDE COMMON-MODE (UP TO V_{CC}^+) AND DIFFERENTIAL VOLTAGE RANGE
- LOW INPUT BIAS AND OFFSET CURRENT
- LOW NOISE e_n = 15nV/√Hz (typ)
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J-FET INPUT STAGE
- LOW HARMONIC DISTORTION : 0.01% (typ)
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : 16V/µs (typ)



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

H
TO99
(Metal Can)

DESCRIPTION

The TL071, TL071A and TL071B are high speed J-FET input single operational amplifiers incorporating well matched, high voltage J-FET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.

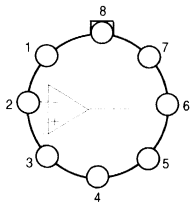
ORDER CODES

Part Number	Temperature	Package		
		H	N	D
TL071M/AM/BM	–55°C, +125°C	•	•	•
TL071I/AI/BI	–40°C, +105°C	•	•	•
TL071C/AC/BC	0°C, +70°C	•	•	•
Examples : TL071MH, TL071CN				

071-01.TBL

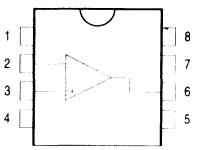
PIN CONNECTIONS (top views)

TO99



071-01.EPS

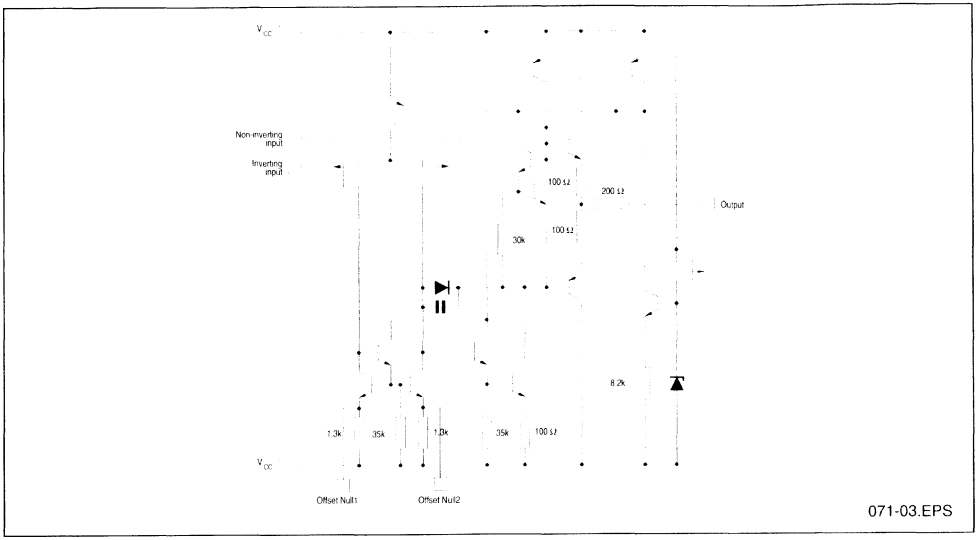
DIP8/SO8



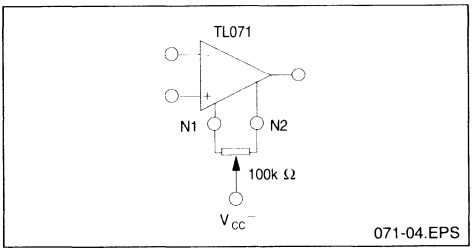
071-02.EPS

1 - Offset Null 1
2 - Inverting input
3 - Non-inverting input
4 - V_{CC}^-
5 - Offset Null 2
6 - Output
7 - V_{CC}^+
8 - N.C.

SCHEMATIC DIAGRAM



INPUT OFFSET VOLTAGE NULL CIRCUITS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage - (note 1)		±18	V
V_i	Input Voltage - (note 3)		±15	V
V_{id}	Differential Input Voltage - (note 2)		±30	V
P_{tot}	Power Dissipation		680	mW
	Output Short-circuit Duration - (note 4)		Infinite	
T_{oper}	Operating Free Air Temperature Range	TL071C,AC,BC TL071I,AI,BI TL071M,AM,BM	0 to 70 –40 to 105 –55 to 125	°C
T_{stg}	Storage Temperature Range		–65 to 150	°C

Notes :
1. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where th zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.
2. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and /or supply voltages must be limited to ensure that th dissipation rating is not exceeded.

ELECTRICAL CHARACTERISTICS

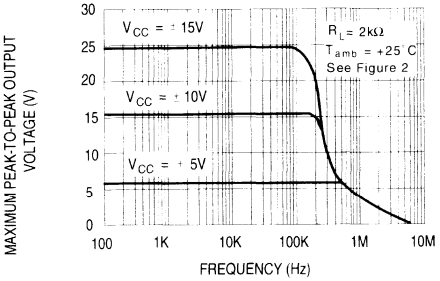
V_{CC} = ±15V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter		TL071I,M,AC,AI, AM,BC,BI,BM			TL071C			Unit
						Min.	Typ.	Max.	
V_{io}	Input Offset Voltage (R_S = 50Ω)								mV
	T_{amb} = 25°C			3	6		3	10	
		TL071BC,BI,BM		1	3				
	$T_{min.} \le T_{amb} \le T_{max.}$				7			13	
		TL071BC,BI,BM			5				
DV_{io}	Input Offset Voltage Drift			10			10		µV/°C
I_{io}	Input Offset Current *								
	T_{amb} = 25°C			5	100		5	100	pA
	$T_{min.} \le T_{amb} \le T_{max.}$				4			10	nA
I_{ib}	Input Bias Current *								
	T_{amb} = 25°C			20	200		20	200	pA
	$T_{min.} \le T_{amb} \le T_{max.}$				20			20	nA
A_{vd}	Large Signal Voltage Gain (R_L = 2kΩ, V_O = ±10V)								V/mV
	T_{amb} = 25°C		50	200		25	200		
	$T_{min.} \le T_{amb} \le T_{max.}$		25			15			
SVR	Supply Voltage Rejection Ratio (R_S = 50Ω)								dB
	T_{amb} = 25°C		80	86		70	86		
	$T_{min.} \le T_{amb} \le T_{max.}$		80			70			
I_{CC}	Supply Current, no Load								mA
	T_{amb} = 25°C			1.4	2.5		1.4	2.5	
	$T_{min.} \le T_{amb} \le T_{max.}$				2.5			2.5	
V_{icm}	Input Common Mode Voltage Range		±11	+15 -12		±11	+15 -12		V
CMR	Common Mode Rejection Ratio (R_S = 50Ω)								dB
	T_{amb} = 25°C		80	86		70	86		
	$T_{min.} \le T_{amb} \le T_{max.}$		80			70			
Ios	Output Short-circuit Current								mA
	T_{amb} = 25°C		10	40	60	10	40	60	
	$T_{min.} \le T_{amb} \le T_{max.}$		10		60	10		60	
$\pm V_{OPP}$	Output Voltage Swing								V
	T_{amb} = 25°C	R_L = 2kΩ	10	12		10	12		
		R_L = 10kΩ	12	13.5		12	13.5		
	$T_{min.} \le T_{amb} \le T_{max.}$	R_L = 2kΩ	10			10			
		R_L = 10kΩ	12			12			
SR	Slew Rate (V_{in} = 10V, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)		8	16		8	16		V/µs
t_r	Rise Time (V_{in} = 20mV, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)			0.1			0.1		µs
K_{OV}	Overshoot (V_{in} = 20mV, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)			10			10		%
GBP	Gain Bandwidth Product (f = 100kHz, T_{amb} = 25°C, V_{in} = 10mV, R_L = 2kΩ, C_L = 100pF)		2.5	4		2.5	4		MHz
R_j	Input Resistance			10^{12}			10^{12}		Ω
THD	Total Harmonic Distortion (f = 1kHz, A_V = 20dB, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, V_O = 2V_{PP})			0.01			0.01		%
e_n	Equivalent Input Noise Voltage (f = 1kHz, R_s = 100Ω)			15			15		$\frac{nV}{\sqrt{Hz}}$
∅m	Phase Margin			45			45		Degrees

* The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature.

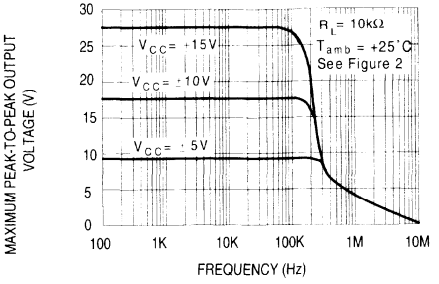
071-03.TBL

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



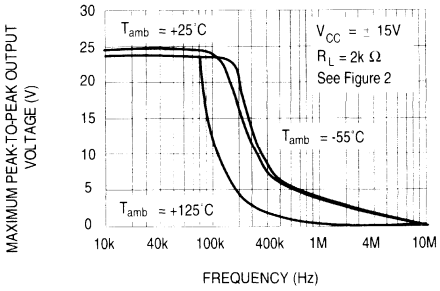
071-05.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



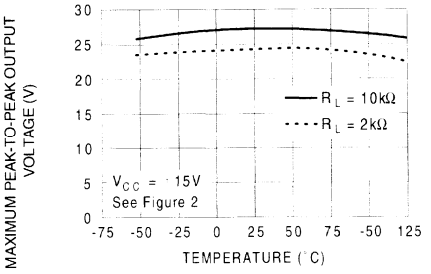
071-06.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



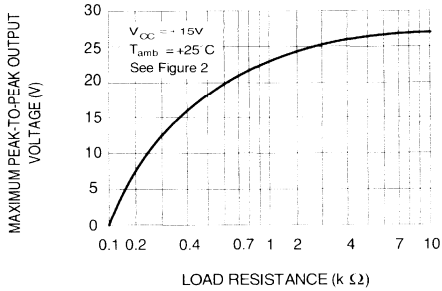
071-07.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREE AIR TEMP.



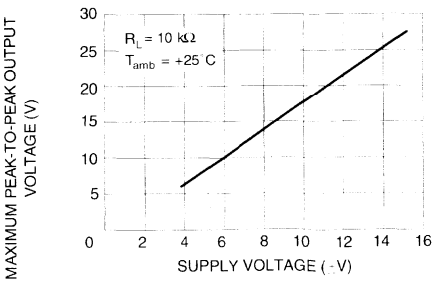
071-08.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS LOAD RESISTANCE



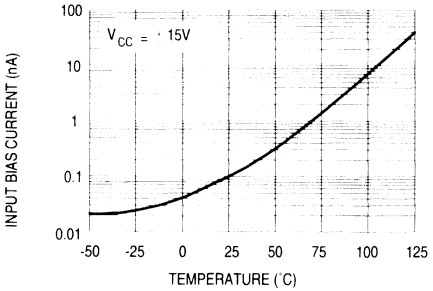
071-09.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS SUPPLY VOLTAGE



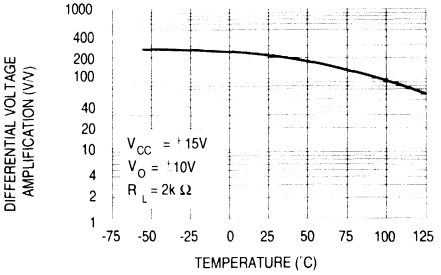
071-10.EPS

INPUT BIAS CURRENT VERSUS FREE AIR TEMPERATURE



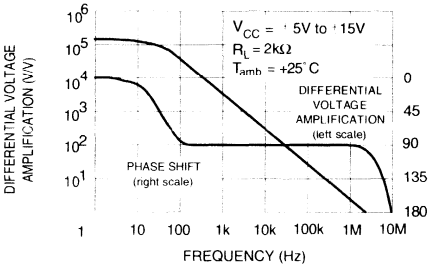
071-11.EPS

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION VERSUS FREE AIR TEMPERATURE



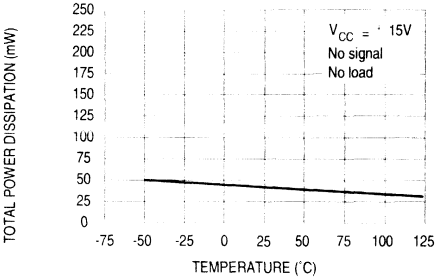
071-12.EPS

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT VERSUS FREQUENCY



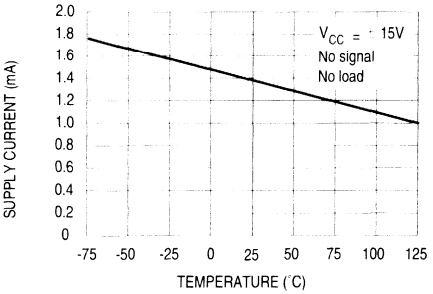
071-13.EPS

TOTAL POWER DISSIPATION VERSUS FREE AIR TEMPERATURE



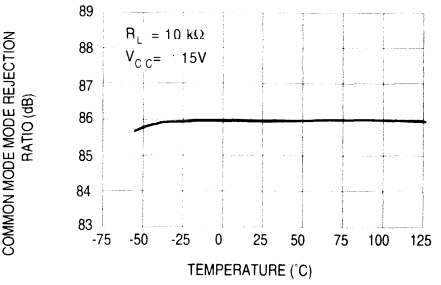
071-14.EPS

SUPPLY CURRENT PER AMPLIFIER VERSUS FREE AIR TEMPERATURE



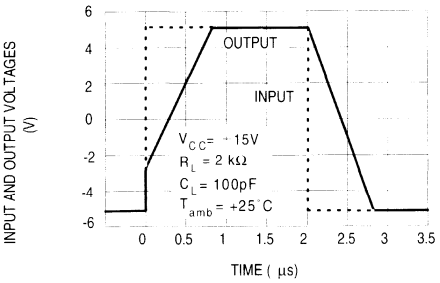
071-15.EPS

COMMON MODE REJECTION RATIO VERSUS FREE AIR TEMPERATURE



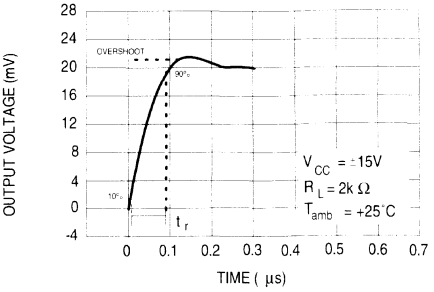
071-16.EPS

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



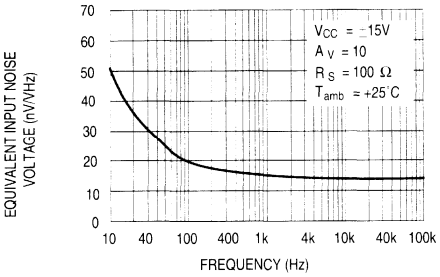
071-17.EPS

OUTPUT VOLTAGE VERSUS ELAPSED TIME



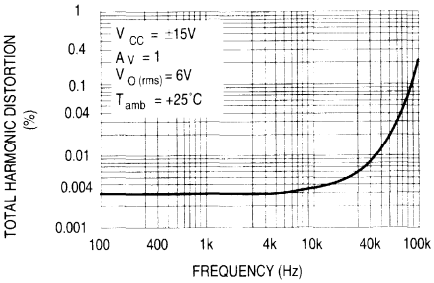
071-18.EPS

EQUIVALENT INPUT NOISE VOLTAGE VERSUS FREQUENCY



071-19.EPS

TOTAL HARMONIC DISTORTION VERSUS FREQUENCY



071-20.EPS

PARAMETER MEASUREMENT INFORMATION

Figure 1 : Voltage Follower

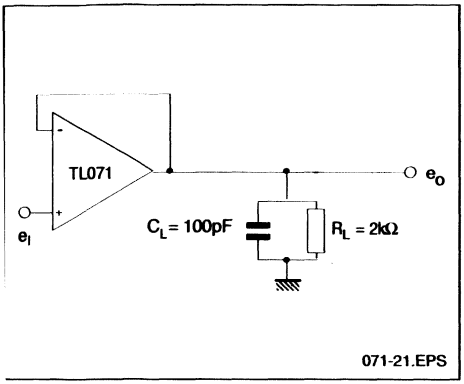
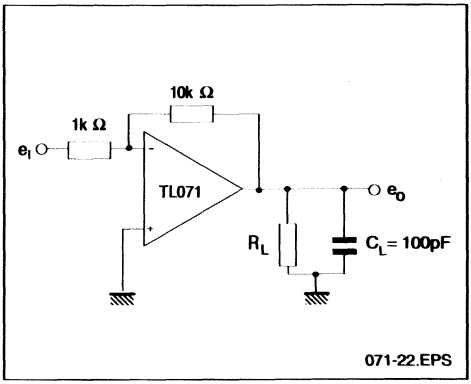
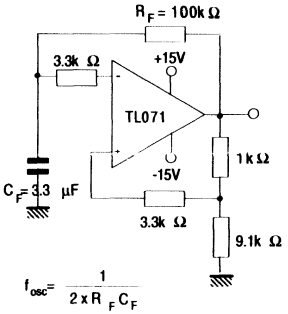


Figure 2 : Gain-of-10 Inverting Amplifier

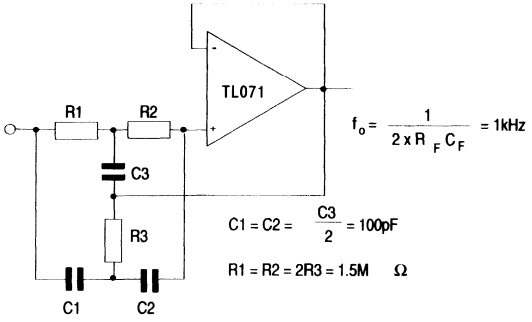


TYPICAL APPLICATIONS

(0.5Hz) SQUARE WAVE OSCILLATOR



HIGH Q NOTCH FILTER

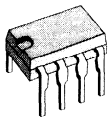


SGS-THOMSON MICROELECTRONICS

TL072
TL072A - TL072B

LOW NOISE DUAL J-FET OPERATIONAL AMPLIFIERS

- LOW POWER CONSUMPTION
- WIDE COMMON-MODE (UP TO V_{CC}^+) AND DIFFERENTIAL VOLTAGE RANGE
- LOW INPUT BIAS AND OFFSET CURRENT
- LOW NOISE e_n = 15nV/√Hz (typ)
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J-FET INPUT STAGE
- LOW HARMONIC DISTORTION : 0.01% (typ)
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : 16V/µs (typ)



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

H
TO99
(Metal Can)

DESCRIPTION

The TL072, TL072A and TL072B are high speed J-FET input dual operational amplifiers incorporating well matched, high voltage J-FET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low input bias and offset current, and low offset voltage temperature coefficient.

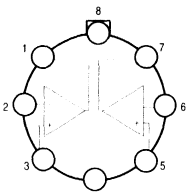
ORDER CODES

Part Number	Temperature	Package		
		H	N	D
TL072M/AM/BM	–55°C, +125°C	•	•	•
TL072I/AI/BI	–40°C, +105°C	•	•	•
TL072C/AC/BC	0°C, +70°C	•	•	•
Examples : TL072MH, TL072CN				

072-01.TBL

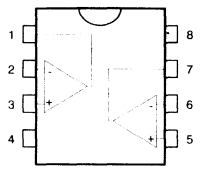
PIN CONNECTIONS (top views)

TO99



072-01.EPS

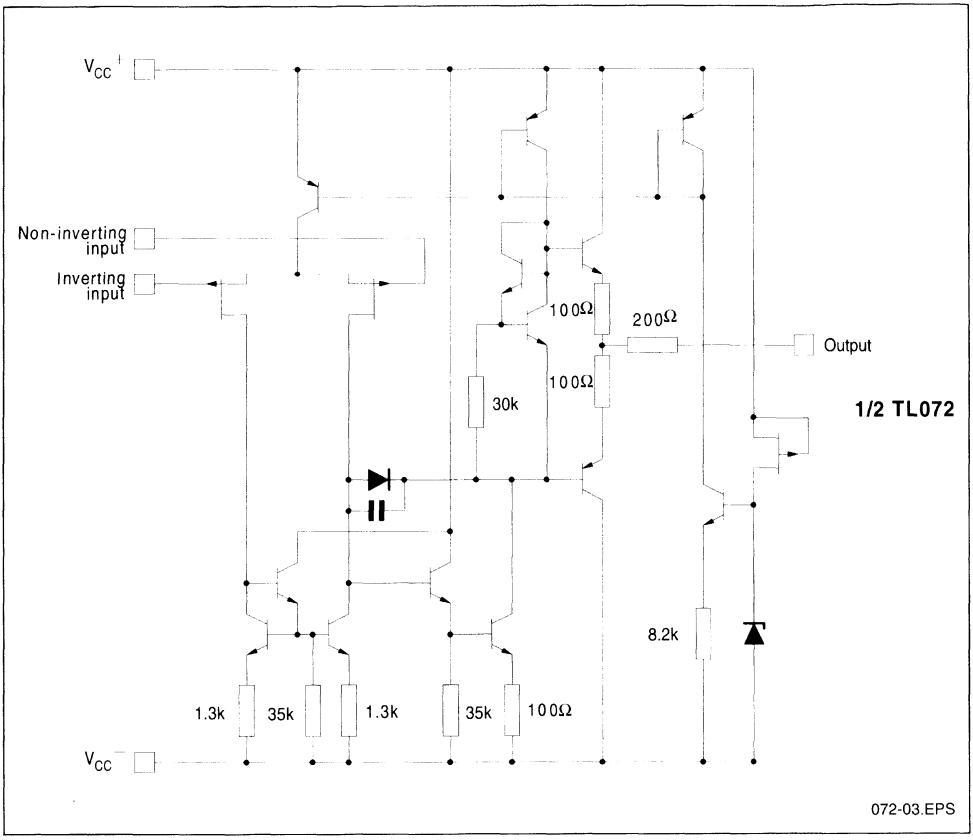
DIP8/CERDIP8
SO8



072-02.EPS

1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^-
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - V_{CC}^+

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage - (note 1)		±18	V
V_i	Input Voltage - (note 3)		±15	V
V_{id}	Differential Input Voltage - (note 2)		±30	V
P_{tot}	Power Dissipation		680	mW
	Output Short-circuit Duration - (note 4)		Infinite	
T_{oper}	Operating Free Air Temperature Range	TL072C,AC,BC TL072I,AI,BI TL072M,AM,BM	0 to 70 –40 to 105 –55 to 125	°C
T_{stg}	Storage Temperature Range		–65 to 150	°C

Notes :
1. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.
2. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and /or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

ELECTRICAL CHARACTERISTICS

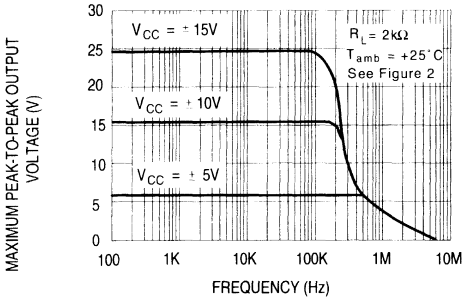
V_{CC} = ±15V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter		TL072I,M,AC,AI, AM,BC,BI,BM			TL072C			Unit
						Min.	Typ.	Max.	
V_{io}	Input Offset Voltage (R_S = 50Ω) T_{amb} = 25°C			3	6		3	10	mV
		TL072BC,BI,BM		1	3				
	$T_{min.} \le T_{amb} \le T_{max.}$				7			13	
		TL072BC,BI,BM			5				
DV_{io}	Input Offset Voltage Drift			10			10		µV/°C
I_{io}	Input Offset Current * T_{amb} = 25°C			5	100		5	100	pA
	$T_{min.} \le T_{amb} \le T_{max.}$				4			10	nA
I_{ib}	Input Bias Current * T_{amb} = 25°C			20	200		20	200	pA
	$T_{min.} \le T_{amb} \le T_{max.}$				20			20	nA
A_{vd}	Large Signal Voltage Gain (R_L = 2kΩ, V_O = ±10V) T_{amb} = 25°C		50	200		25	200		V/mV
	$T_{min.} \le T_{amb} \le T_{max.}$		25			15			
SVR	Supply Voltage Rejection Ratio (R_S = 50Ω) T_{amb} = 25°C		80	86		70	86		dB
	$T_{min.} \le T_{amb} \le T_{max.}$		80			70			
I_{CC}	Supply Current, per Amp, no Load T_{amb} = 25°C			1.4	2.5		1.4	2.5	mA
	$T_{min.} \le T_{amb} \le T_{max.}$				2.5			2.5	
V_{icm}	Input Common Mode Voltage Range		±11	+15 -12		±11	+15 -12		V
CMR	Common Mode Rejection Ratio (R_S = 50Ω) T_{amb} = 25°C		80	86		70	86		dB
	$T_{min.} \le T_{amb} \le T_{max.}$		80			70			
Ios	Output Short-circuit Current T_{amb} = 25°C		10	40	60	10	40	60	mA
	$T_{min.} \le T_{amb} \le T_{max.}$		10		60	10		60	
$\pm V_{OPP}$	Output Voltage Swing T_{amb} = 25°C	R_L = 2kΩ	10	12		10	12		V
		R_L = 10kΩ	12	13.5		12	13.5		
	$T_{min.} \le T_{amb} \le T_{max.}$	R_L = 2kΩ	10			10			
		R_L = 10kΩ	12			12			
SR	Slew Rate (V_{in} = 10V, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)		8	16		8	16		V/µs
t_r	Rise Time (V_{in} = 20mV, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)			0.1			0.1		µs
K_{OV}	Overshoot (V_{in} = 20mV, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)			10			10		%
GBP	Gain Bandwidth Product (f = 100kHz, T_{amb} = 25°C, V_{in} = 10mV, R_L = 2kΩ, C_L = 100pF)		2.5	4		2.5	4		MHz
R_j	Input Resistance			10^{12}			10^{12}		Ω
THD	Total Harmonic Distortion (f = 1kHz, A_V = 20dB, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, V_O = 2V_{PP})			0.01			0.01		%
e_n	Equivalent Input Noise Voltage (f = 1kHz, R_s = 100Ω)			15			15		$\frac{nV}{\sqrt{Hz}}$
Øm	Phase Margin			45			45		Degrees
V_{O1}/V_{O2}	Channel Separation (A_v = 100)			120			120		dB

* The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature.

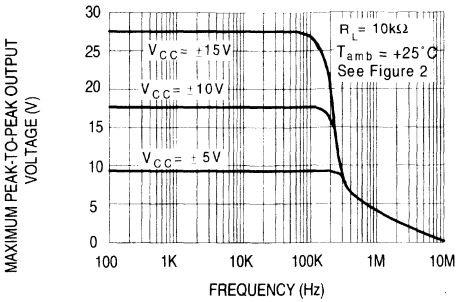
072-03.TBL

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



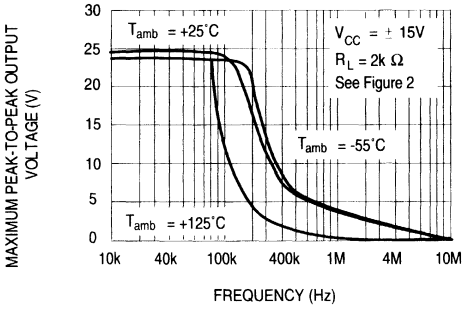
072-04.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



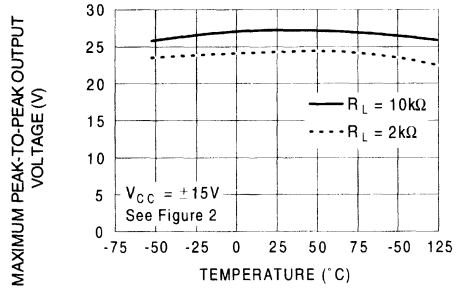
072-05.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



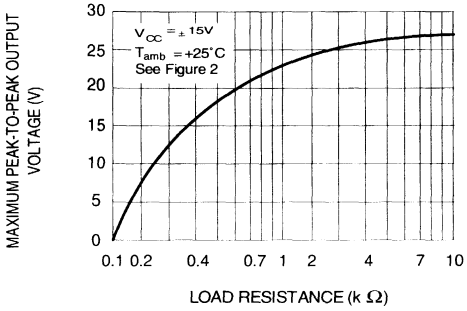
072-06.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREE AIR TEMP.



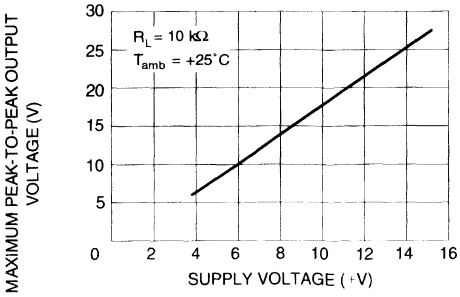
072-07.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS LOAD RESISTANCE



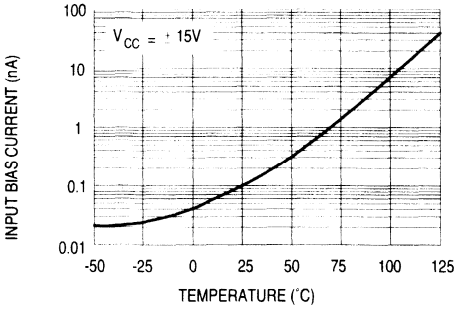
072-08.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS SUPPLY VOLTAGE



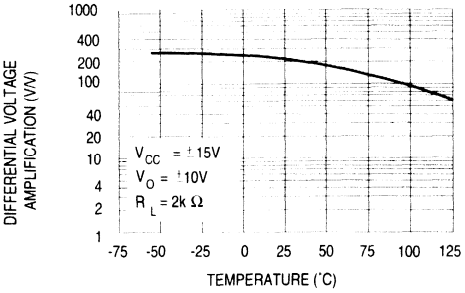
072-09.EPS

INPUT BIAS CURRENT VERSUS FREE AIR TEMPERATURE



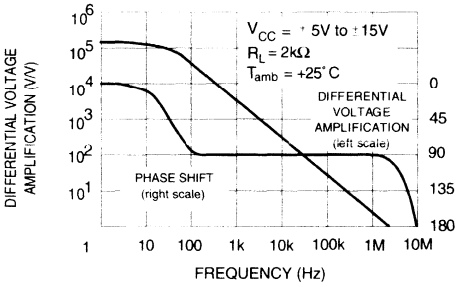
072-10.EPS

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION VERSUS FREE AIR TEMPERATURE



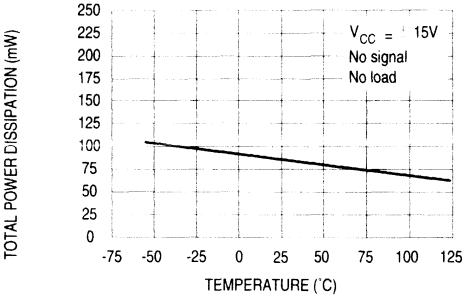
072-11.EPS

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT VERSUS FREQUENCY



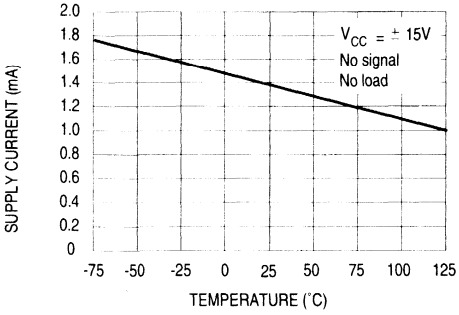
072-12.EPS

TOTAL POWER DISSIPATION VERSUS FREE AIR TEMPERATURE



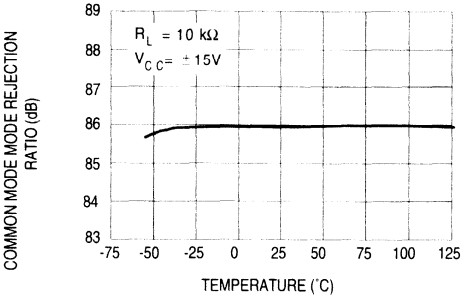
072-13.EPS

SUPPLY CURRENT PER AMPLIFIER VERSUS FREE AIR TEMPERATURE



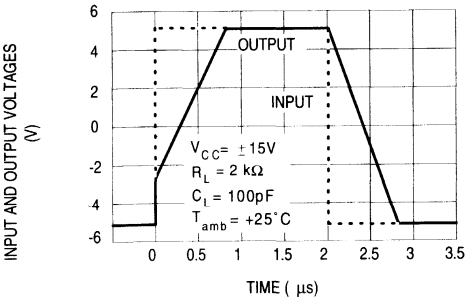
072-14.EPS

COMMON MODE REJECTION RATIO VERSUS FREE AIR TEMPERATURE



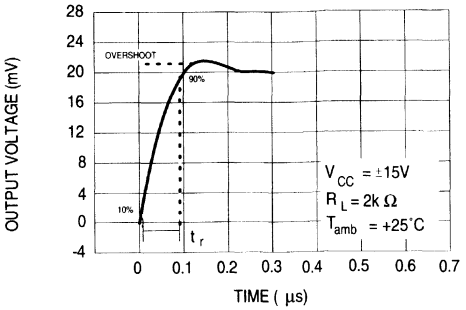
072-15.EPS

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



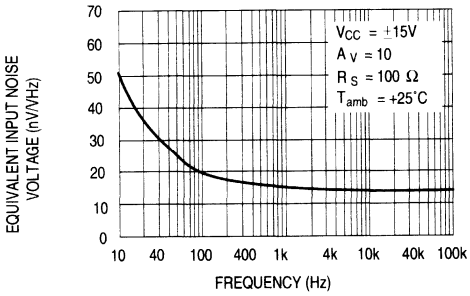
072-16.EPS

OUTPUT VOLTAGE VERSUS ELAPSED TIME



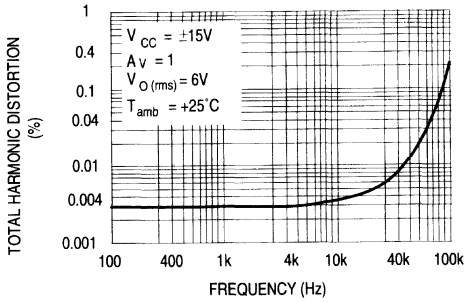
072-17.EPS

EQUIVALENT INPUT NOISE VOLTAGE VERSUS FREQUENCY



072-18.EPS

TOTAL HARMONIC DISTORTION VERSUS FREQUENCY



072-19.EPS

PARAMETER MEASUREMENT INFORMATION

Figure 1 : Voltage Follower

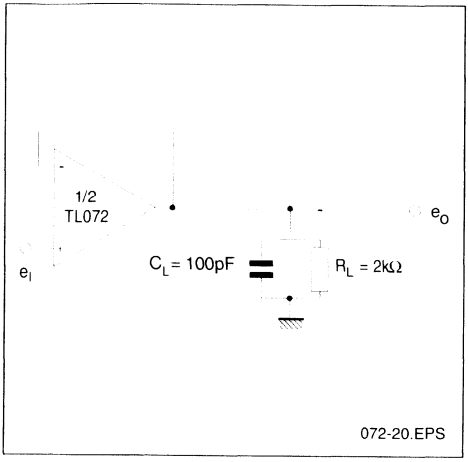
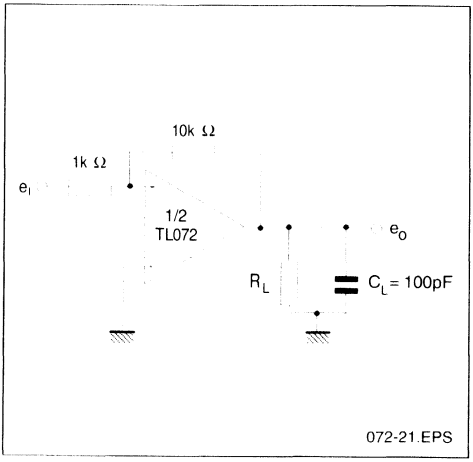
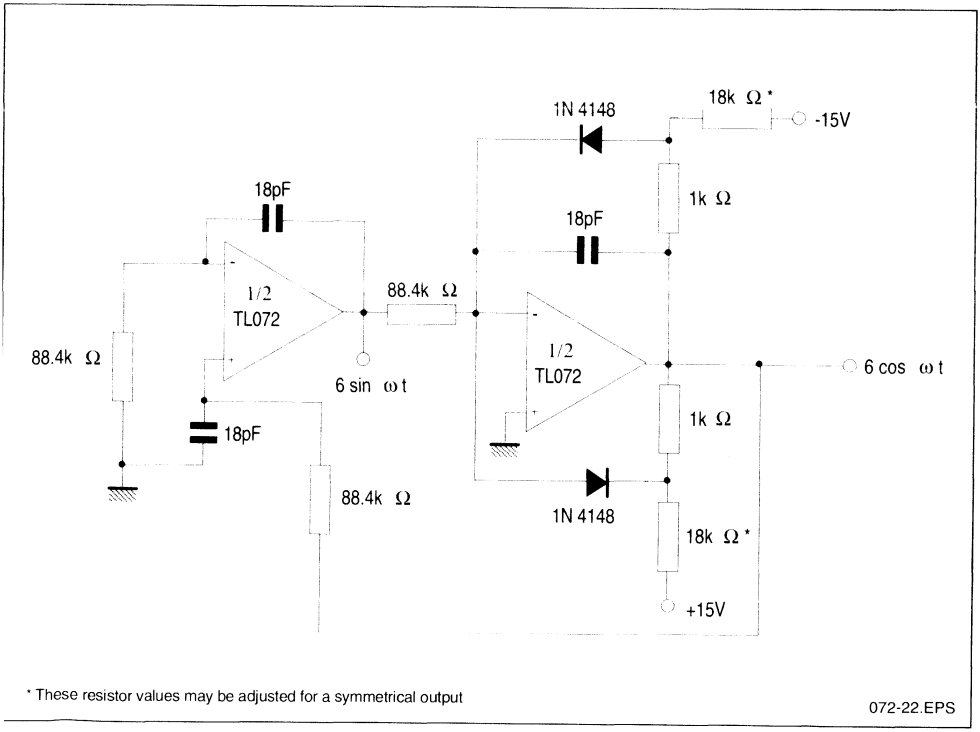


Figure 2 : Gain-of-10 Inverting Amplifier



TYPICAL APPLICATION

100KHz QUADRUPLE OSCILLATOR



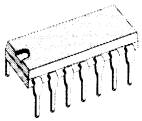
* These resistor values may be adjusted for a symmetrical output

SGS-THOMSON MICROELECTRONICS

TL074
TL074A - TL074B

LOW NOISE QUAD J-FET OPERATIONAL AMPLIFIERS

- LOW POWER CONSUMPTION
- WIDE COMMON-MODE (UP TO V_{CC}^+) AND DIFFERENTIAL VOLTAGE RANGE
- LOW INPUT BIAS AND OFFSET CURRENT
- LOW NOISE e_n = 15nV/√Hz (typ)
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J-FET INPUT STAGE
- LOW HARMONIC DISTORTION : 0.01% (typ)
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : 16V/µs (typ)



N
DIP14
(Plastic Package)
J
CERDIP14
(Cerdip Package)

D
SO14
(Plastic Micropackage)

DESCRIPTION

The TL074, TL074A and TL074B are high speed J-FET input quad operational amplifiers incorporating well matched, high voltage J-FET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.

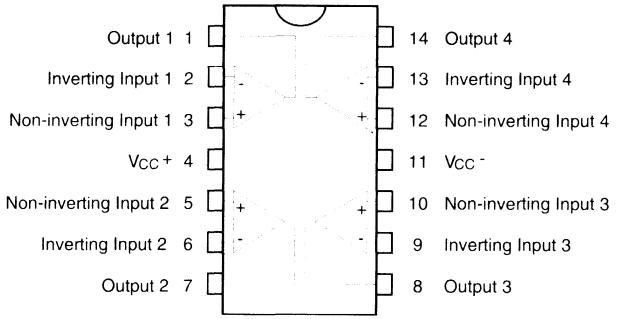
ORDER CODES

Part Number	Temperature	Package		
		N	J	D
TL074M/AM/BM	−55°C, +125°C	•	•	•
TL074I/AI/BI	−40°C, +105°C	•	•	•
TL074C/AC/BC	0°C, +70°C	•	•	•

Examples : TL074MJ, TL074IN

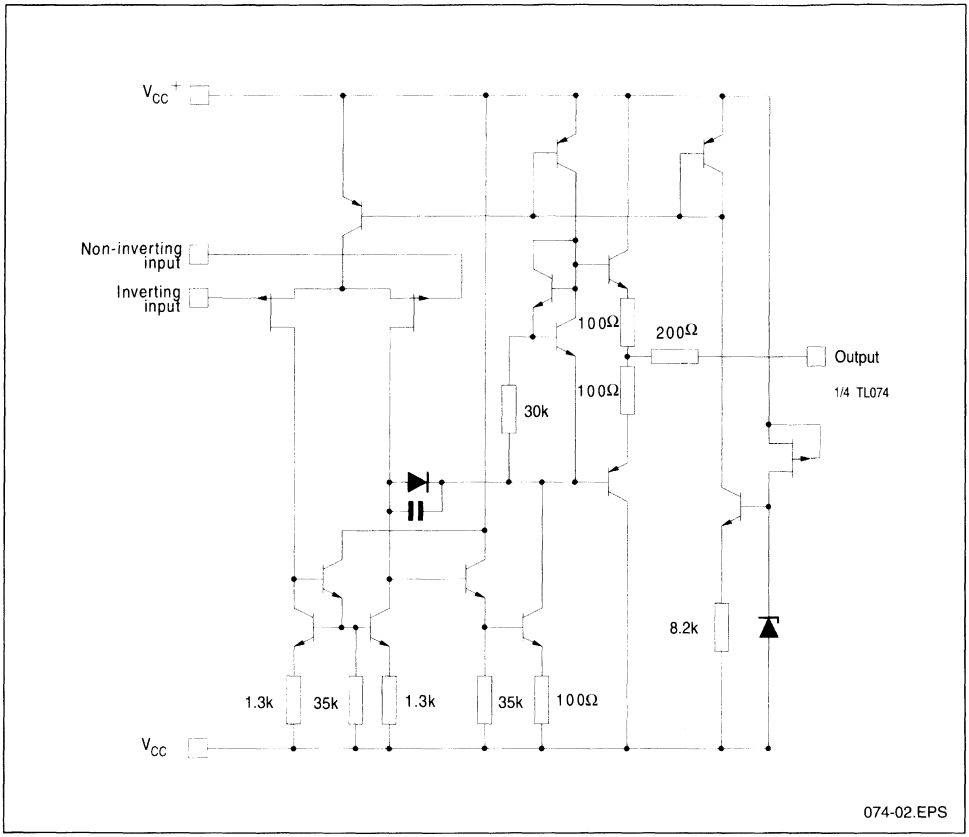
074-01.TBL

PIN CONNECTIONS (top view)



074-01.EPS

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage - (note 1)		±18	V
V_i	Input Voltage - (note 3)		±15	V
V_{id}	Differential Input Voltage - (note 2)		±30	V
P_{tot}	Power Dissipation		680	mW
	Output Short-circuit Duration - (note 4)		Infinite	
T_{oper}	Operating Free Air Temperature Range	TL074C,AC,BC TL074I,AI,BI TL074M,AM,BM	0 to 70 –40 to 105 –55 to 125	°C

Notes :
1. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.
2. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and /or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

ELECTRICAL CHARACTERISTICS

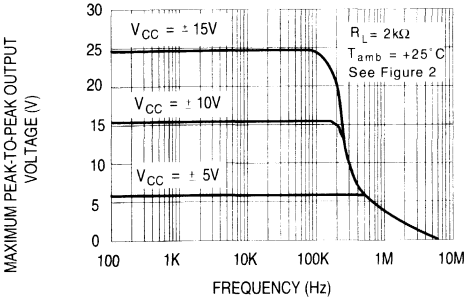
V_{CC} = ±15V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter		TL074I,M,AC,AI, AM,BC,BI,BM			TL074C			Unit
						Min.	Typ.	Max.	
V_{io}	Input Offset Voltage (R_S = 50Ω)								mV
	T_{amb} = 25°C			3	6		3	10	
		TL074BC,BI,BM		1	3				
	$T_{min.} \le T_{amb} \le T_{max.}$				7			13	
		TL074BC,BI,BM			5				
DV_{io}	Input Offset Voltage Drift			10			10		µV/°C
I_{io}	Input Offset Current *								
	T_{amb} = 25°C			5	100		5	100	pA
	$T_{min.} \le T_{amb} \le T_{max.}$				4			10	nA
I_{ib}	Input Bias Current *								
	T_{amb} = 25°C			20	200		30	200	pA
	$T_{min.} \le T_{amb} \le T_{max.}$				20			20	nA
A_{vd}	Large Signal Voltage Gain (R_L = 2kΩ, V_O = ±10V)								V/mV
	T_{amb} = 25°C		50	200		25	200		
	$T_{min.} \le T_{amb} \le T_{max.}$		25			15			
SVR	Supply Voltage Rejection Ratio (R_S = 50Ω)								dB
	T_{amb} = 25°C		80	86		70	86		
	$T_{min.} \le T_{amb} \le T_{max.}$		80			70			
I_{CC}	Supply Current, per Amp, no Load								mA
	T_{amb} = 25°C			1.4	2.5		1.4	2.5	
	$T_{min.} \le T_{amb} \le T_{max.}$				2.5			2.5	
V_{icm}	Input Common Mode Voltage Range		±11	+15 -12		±11	+15 -12		V
CMR	Common Mode Rejection Ratio (R_S = 50Ω)								dB
	T_{amb} = 25°C		80	86		70	86		
	$T_{min.} \le T_{amb} \le T_{max.}$		80			70			
Ios	Output Short-circuit Current								mA
	T_{amb} = 25°C		10	40	60	10	40	60	
	$T_{min.} \le T_{amb} \le T_{max.}$		10		60	10		60	
$\pm V_{OPP}$	Output Voltage Swing								V
	T_{amb} = 25°C	R_L = 2kΩ	10	12		10	12		
		R_L = 10kΩ	12	13.5		12	13.5		
	$T_{min.} \le T_{amb} \le T_{max.}$	R_L = 2kΩ	10			10			
		R_L = 10kΩ	12			12			
SR	Slew Rate (V_{in} = 10V, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)		8	16		8	16		V/µs
t_r	Rise Time (V_{in} = 20mV, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)			0.1			0.1		µs
K_{OV}	Overshoot (V_{in} = 20mV, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)			10			10		%
GBP	Gain Bandwidth Product (f = 100kHz, T_{amb} = 25°C, V_{in} = 10mV, R_l = 2kΩ, C_L = 100pF)		2.5	4		2.5	4		MHz
R_i	Input Resistance			10^{12}			10^{12}		Ω
THD	Total Harmonic Distortion (f = 1kHz, A_V = 20dB, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, V_O = $2V_{PP}$)			0.01			0.01		%
e_n	Equivalent Input Noise Voltage (f = 1kHz, R_s = 100Ω)			15			15		$\frac{nV}{\sqrt{Hz}}$
Øm	Phase Margin			45			45		Degrees
V_{O1}/V_{O2}	Channel Separation (A_v = 100)			120			120		dB

C74-03.TBL

* The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature.

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



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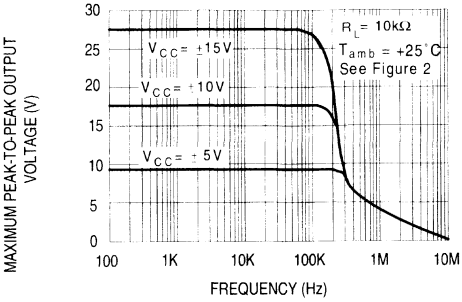
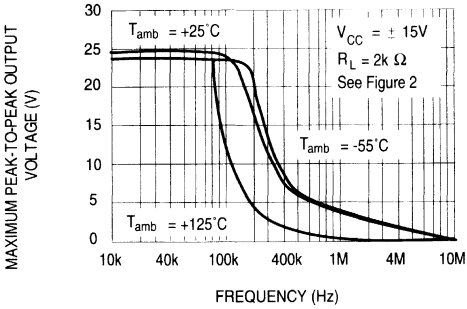
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



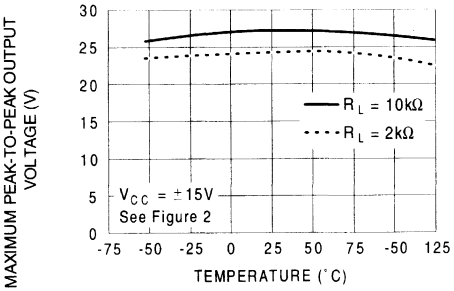
074-04.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



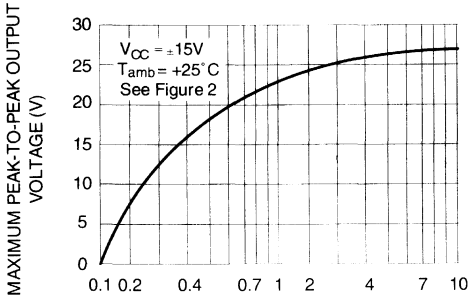
074-05.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREE AIR TEMP.



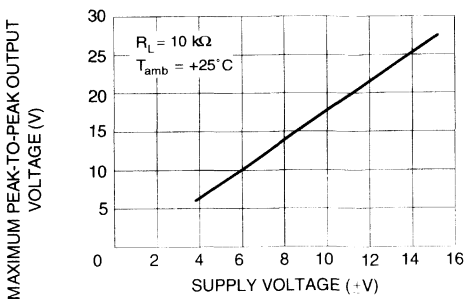
074-06.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS LOAD RESISTANCE



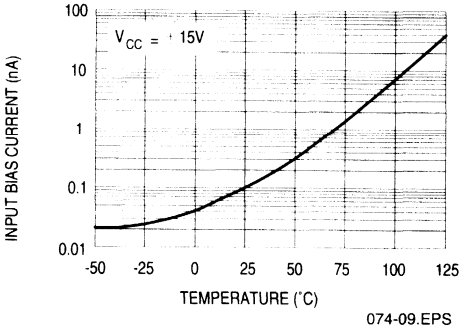
074-07.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS SUPPLY VOLTAGE



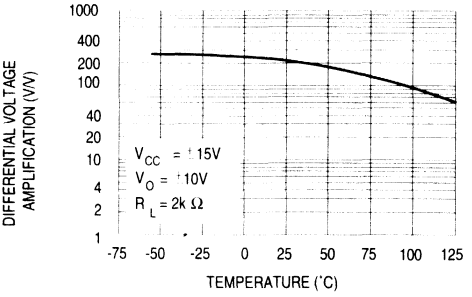
074-08.EPS

INPUT BIAS CURRENT VERSUS FREE AIR TEMPERATURE



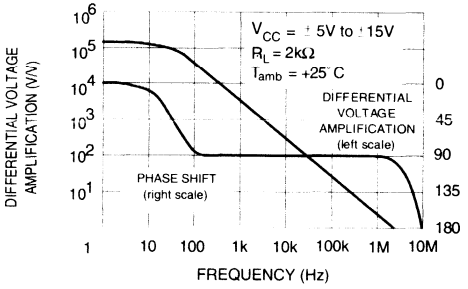
074-09.EPS

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION VERSUS FREE AIR TEMPERATURE



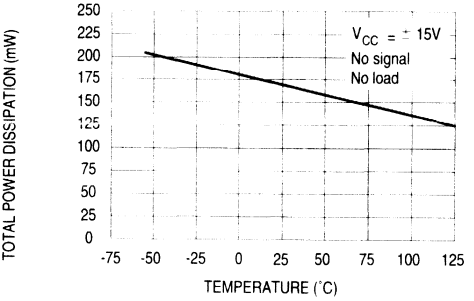
074-10.EPS

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT VERSUS FREQUENCY



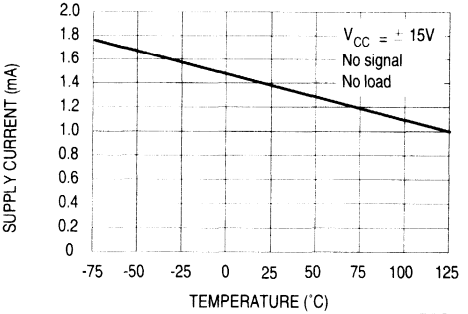
074-11.EPS

TOTAL POWER DISSIPATION VERSUS FREE AIR TEMPERATURE



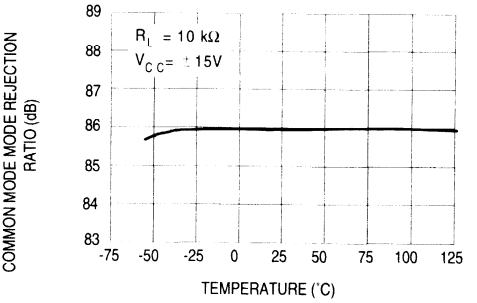
074-12.EPS

SUPPLY CURRENT PER AMPLIFIER VERSUS FREE AIR TEMPERATURE



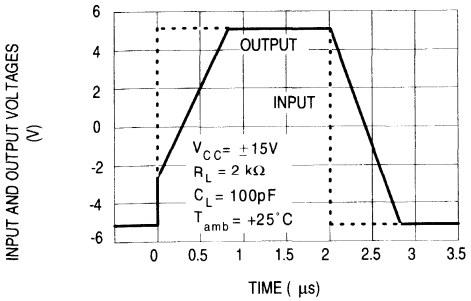
074-13.EPS

COMMON MODE REJECTION RATIO VERSUS FREE AIR TEMPERATURE



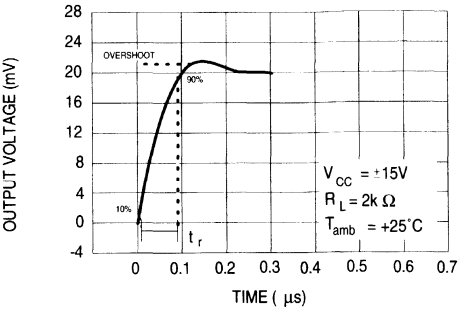
074-14.EPS

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



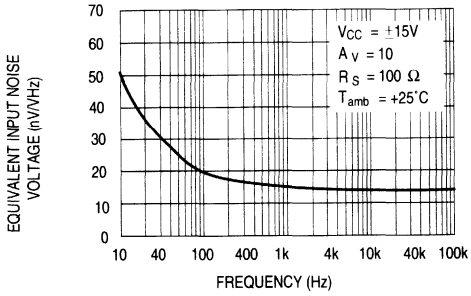
074-15.EPS

OUTPUT VOLTAGE VERSUS ELAPSED TIME



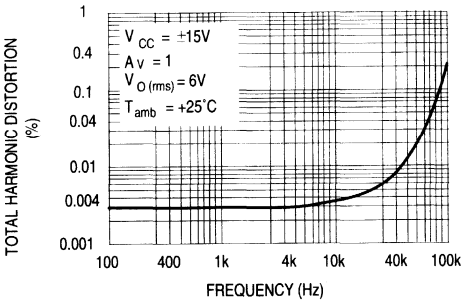
074-16.EPS

EQUIVALENT INPUT NOISE VOLTAGE VERSUS FREQUENCY



074-17.EPS

TOTAL HARMONIC DISTORTION VERSUS FREQUENCY



074-18.EPS

PARAMETER MEASUREMENT INFORMATION

Figure 1 : Voltage Follower

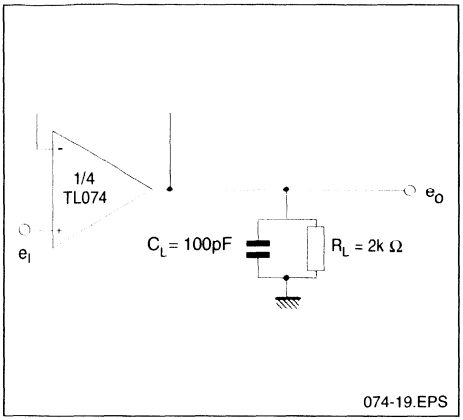
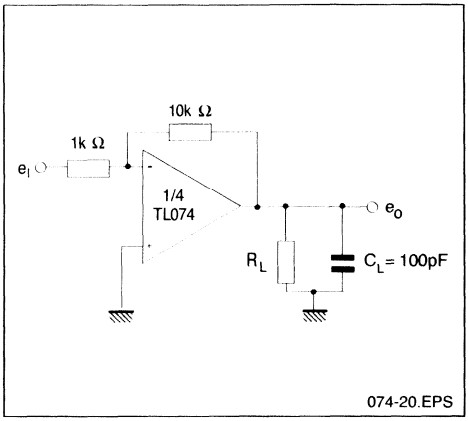
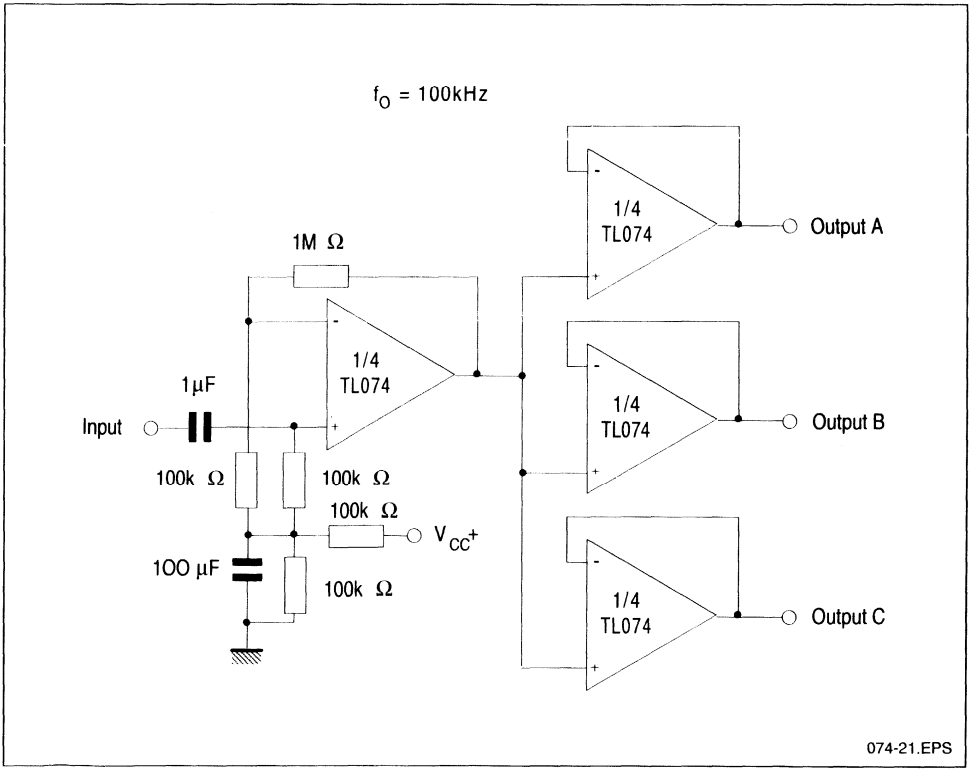


Figure 2 : Gain-of-10 Inverting Amplifier



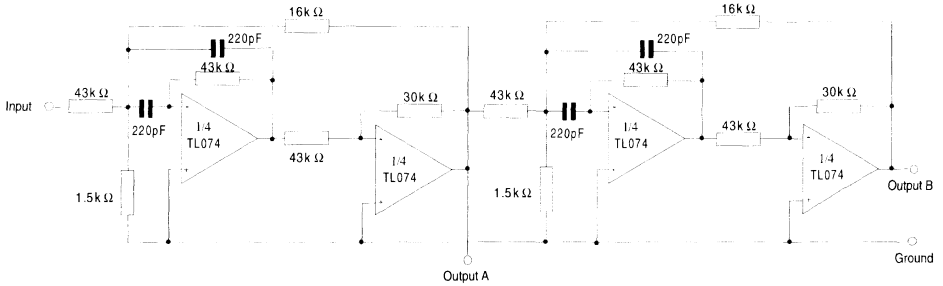
TYPICAL APPLICATIONS

AUDIO DISTRIBUTION AMPLIFIER



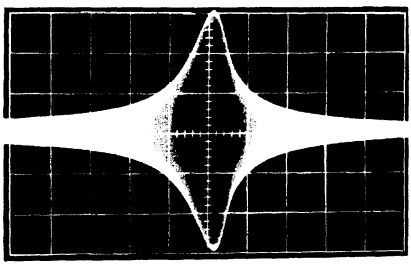
TYPICAL APPLICATIONS (continued)

POSITIVE FEEDBACK BANDPASS FILTER



074-22.EPS

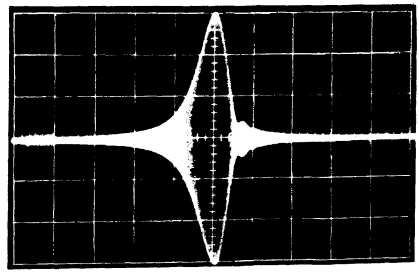
OUTPUT A



074-23.EPS

SECOND ORDER BANDPASS FILTER
fo = 100kHz ; Q = 30 ; Gain = 16

OUTPUT B



074-24.EPS

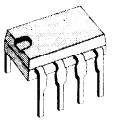
CASCADED BANDPASS FILTER
fo = 100kHz ; Q = 69 ; Gain = 16

SGS-THOMSON MICROELECTRONICS

TL081
TL081A - TL081B

GENERAL PURPOSE SINGLE J-FET OPERATIONAL AMPLIFIERS

- LOW POWER CONSUMPTION
- WIDE COMMON-MODE (UP TO V_{CC}^+) AND DIFFERENTIAL VOLTAGE RANGE
- LOW INPUT BIAS AND OFFSET CURRENT
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J-FET INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : 16V/µs (typ)



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

H
TO99
(Metal Can)

DESCRIPTION

The TL081, TL081A and TL081B are high speed J-FET input single operational amplifiers incorporating well matched, high voltage J-FET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.

ORDER CODES

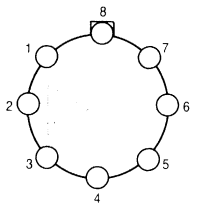
Part Number	Temperature	Package		
		H	N	D
TL081M/AM/BM	–55°C, +125°C	•	•	•
TL081I/AI/BI	–40°C, +105°C	•	•	•
TL081C/AC/BC	0°C, +70°C	•	•	•

Examples : TL081CD, TL081IN

081-01.TBL

PIN CONNECTIONS (top views)

TO99



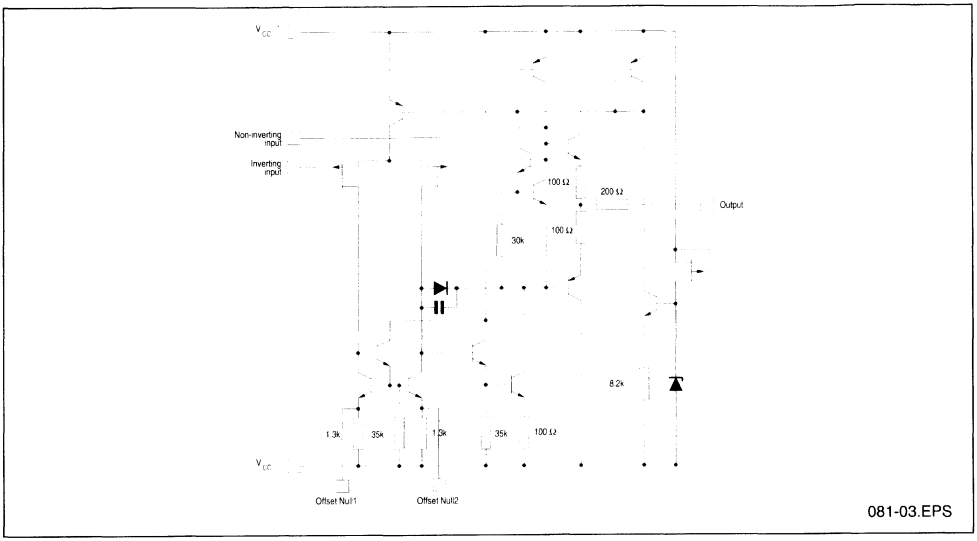
081-01.EPS

DIP8/SO8

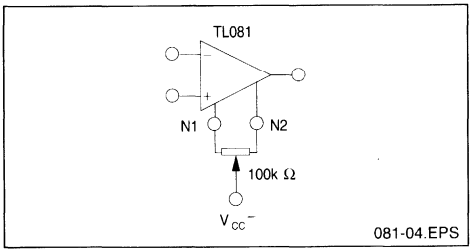
081-02.EPS

1 - Offset Null 1
2 - Inverting input
3 - Non-inverting input
4 - V_{CC}^-
5 - Offset Null 2
6 - Output
7 - V_{CC}^+
8 - N.C.

SCHEMATIC DIAGRAM



INPUT OFFSET VOLTAGE NULL CIRCUITS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage - (note 1)		±18	V
V_i	Input Voltage - (note 3)		±15	V
V_{id}	Differential Input Voltage - (note 2)		±30	V
P_{tot}	Power Dissipation		680	mW
	Output Short-circuit Duration - (note 4)		Infinite	
T_{oper}	Operating Free Air Temperature Range	TL081C,AC,BC TL081I,AI,BI TL081M,AM,BM	0 to 70 –40 to 105 –55 to 125	°C
T_{stg}	Storage Temperature Range		–65 to 150	°C

Notes : 1. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.
2. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and /or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

081-02.TBL

ELECTRICAL CHARACTERISTICS

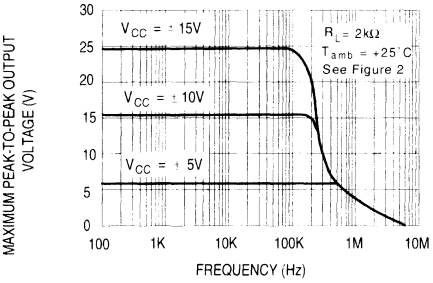
V_{CC} = ±15V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	TL081I,M,AC,AI, AM,BC,BI,BM			TL081C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage (R_S = 50Ω) T_{amb} = 25°C TL081BC,BI,BM $T_{min.} \le T_{amb} \le T_{max.}$ TL081BC,BI,BM		3 1	6 3 7 5		3	10 13	mV
DV_{io}	Input Offset Voltage Drift		10			10		µV/°C
I_{io}	Input Offset Current * T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$		5	100 4		5	100 4	pA nA
I_{ib}	Input Bias Current * T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$		20	200 20		20	400 20	pA nA
A_{vd}	Large Signal Voltage Gain (R_L = 2kΩ, V_O = ±10V) T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$	50 25	200		25 15	200		V/mV
SVR	Supply Voltage Rejection Ratio (R_S = 50Ω) T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$	80 80	86		70 70	86		dB
I_{CC}	Supply Current, no Load T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$		1.4	2.5 2.5		1.4	2.5 2.5	mA
V_{icm}	Input Common Mode Voltage Range	±11	+15 -12		±11	+15 -12		V
CMR	Common Mode Rejection Ratio (R_S = 50Ω) T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$	80 80	86		70 70	86		dB
Ios	Output Short-circuit Current T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$	10 10	40	60 60	10 10	40	60 60	mA
$\pm V_{OPP}$	Output Voltage Swing T_{amb} = 25°C R_L = 2kΩ R_L = 10kΩ $T_{min.} \le T_{amb} \le T_{max.}$ R_L = 2kΩ R_L = 10kΩ	10 12 10 12	12 13.5		10 12 10 12	12 13.5		V
SR	Slew Rate (V_{in} = 10V, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)	8	16		8	16		V/µs
t_r	Rise Time (V_{in} = 20mV, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)		0.1			0.1		µs
K_{OV}	Overshoot (V_{in} = 20mV, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)		10			10		%
GBP	Gain Bandwidth Product (f = 100kHz, T_{amb} = 25°C, V_{in} = 10mV, R_L = 2kΩ, C_L = 100pF)	2.5	4		2.5	4		MHz
R_i	Input Resistance		10^{12}			10^{12}		Ω
THD	Total Harmonic Distortion (f = 1kHz, A_V = 20dB, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, V_O = $2V_{PP}$)		0.01			0.01		%
e_n	Equivalent Input Noise Voltage (f = 1kHz, R_s = 100Ω)		15			15		$\frac{nV}{\sqrt{Hz}}$
Øm	Phase Margin		45			45		Degrees

* The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature.

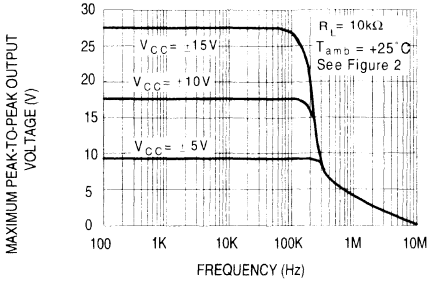
081-03.TBL

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



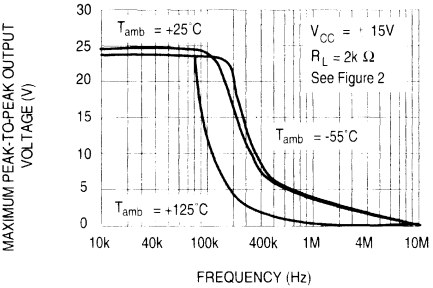
081-05.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



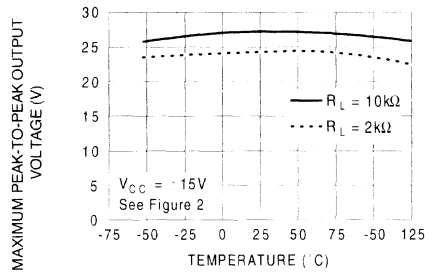
081-06.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



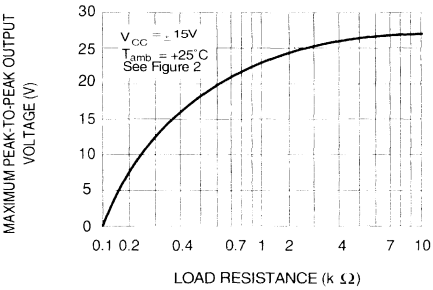
081-07.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREE AIR TEMP.



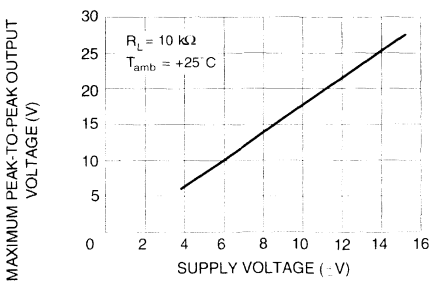
081-08.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS LOAD RESISTANCE



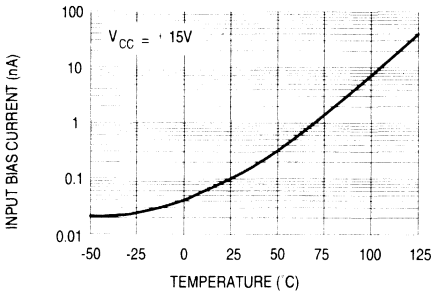
081-09.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS SUPPLY VOLTAGE



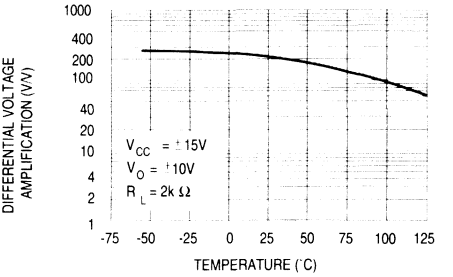
081-10.EPS

INPUT BIAS CURRENT VERSUS FREE AIR TEMPERATURE



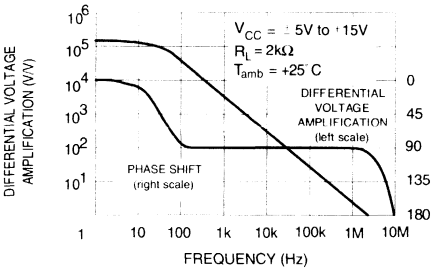
081-11.EPS

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION VERSUS FREE AIR TEMPERATURE



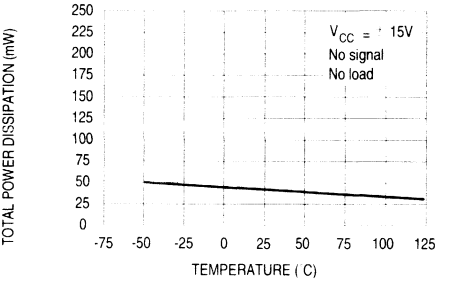
081-12.EPS

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT VERSUS FREQUENCY



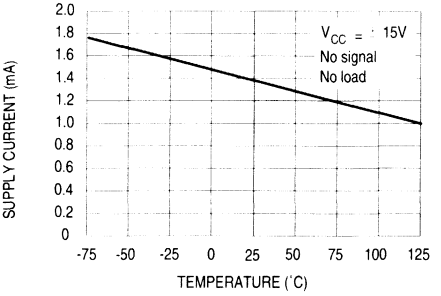
081-13.EPS

TOTAL POWER DISSIPATION VERSUS FREE AIR TEMPERATURE



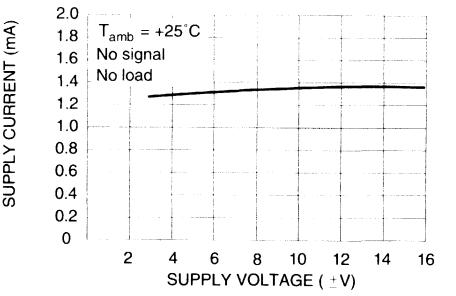
081-14.EPS

SUPPLY CURRENT PER AMPLIFIER VERSUS FREE AIR TEMPERATURE



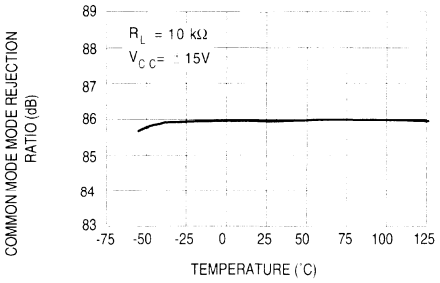
081-15.EPS

SUPPLY CURRENT PER AMPLIFIER VERSUS SUPPLY VOLTAGE



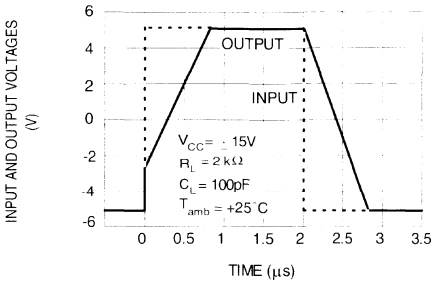
081-16.EPS

COMMON MODE REJECTION RATIO VERSUS FREE AIR TEMPERATURE



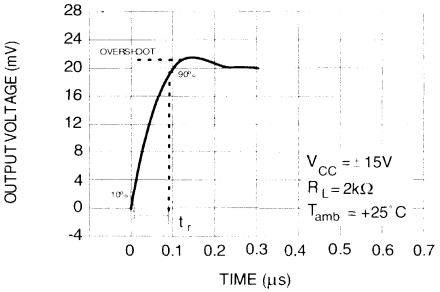
081-17.EPS

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



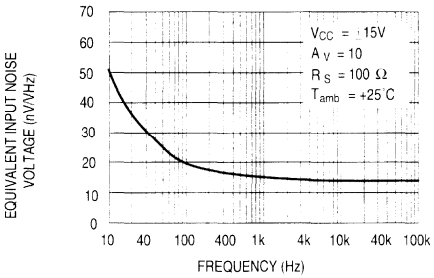
081-18.EPS

OUTPUT VOLTAGE VERSUS ELAPSED TIME



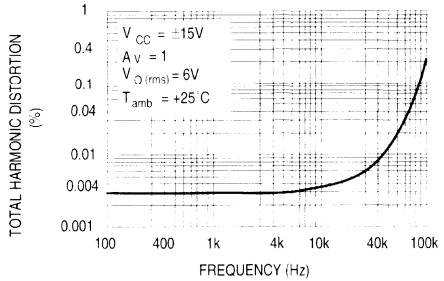
081-19.EPS

EQUIVALENT INPUT NOISE VOLTAGE VERSUS FREQUENCY



081-20.EPS

TOTAL HARMONIC DISTORTION VERSUS FREQUENCY



081-21.EPS

PARAMETER MEASUREMENT INFORMATION

Figure 1 : Voltage Follower

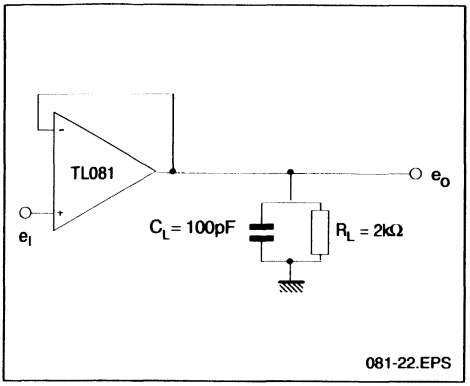
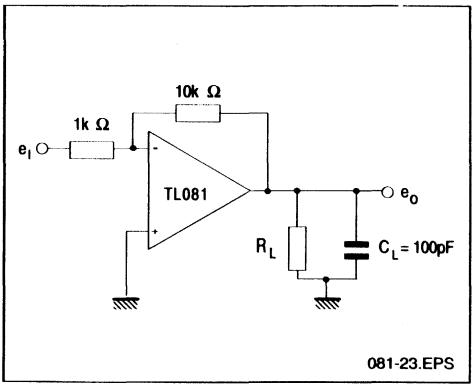
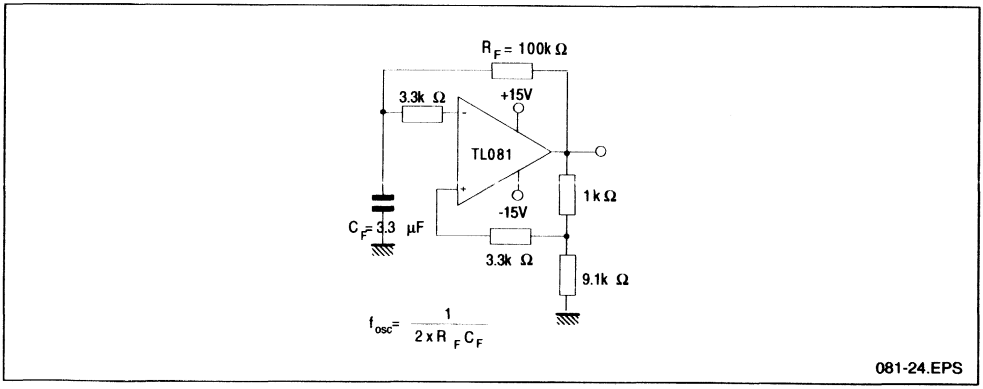


Figure 2 : Gain-of-10 Inverting Amplifier

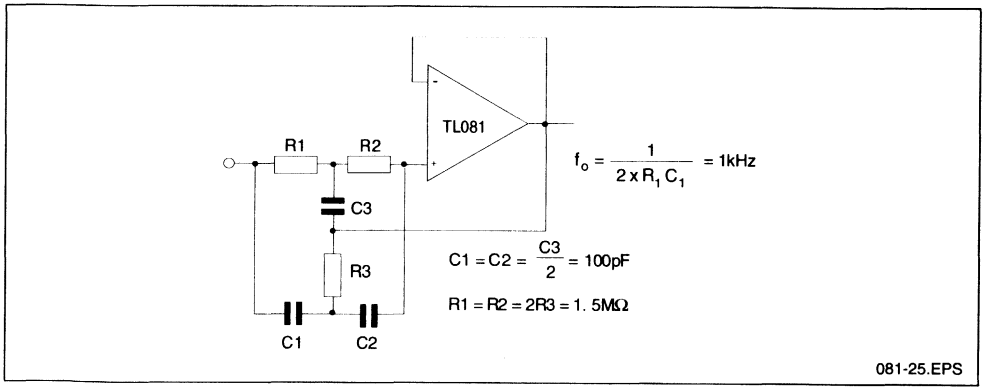


TYPICAL APPLICATIONS

(0.5Hz) SQUARE WAVE OSCILLATOR



HIGH Q NOTCH FILTER

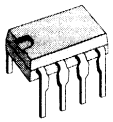


SGS-THOMSON MICROELECTRONICS

TL082
TL082A - TL082B

GENERAL PURPOSE DUAL J-FET OPERATIONAL AMPLIFIERS

- LOW POWER CONSUMPTION
- WIDE COMMON-MODE (UP TO V_{CC}^+) AND DIFFERENTIAL VOLTAGE RANGE
- LOW INPUT BIAS AND OFFSET CURRENT
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J-FET INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : 16V/µs (typ)



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

H
TO99
(Metal Can)

DESCRIPTION

The TL082, TL082A and TL082B are high speed J-FET input dual operational amplifiers incorporating well matched, high voltage J-FET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low input bias and offset current, and low offset voltage temperature coefficient.

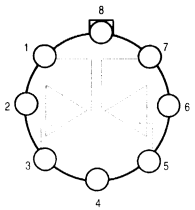
ORDER CODES

Part Number	Temperature	Package		
		H	N	D
TL082M/AM/BM	–55°C, +125°C	•	•	•
TL082I/AI/BI	–40°C, +105°C	•	•	•
TL082C/AC/BC	0°C, +70°C	•	•	•
Examples : TL082CD, TL082IN				

082-01.TBL

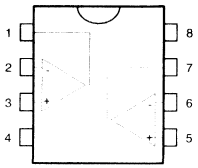
PIN CONNECTIONS (top views)

TO99



082-01.EPS

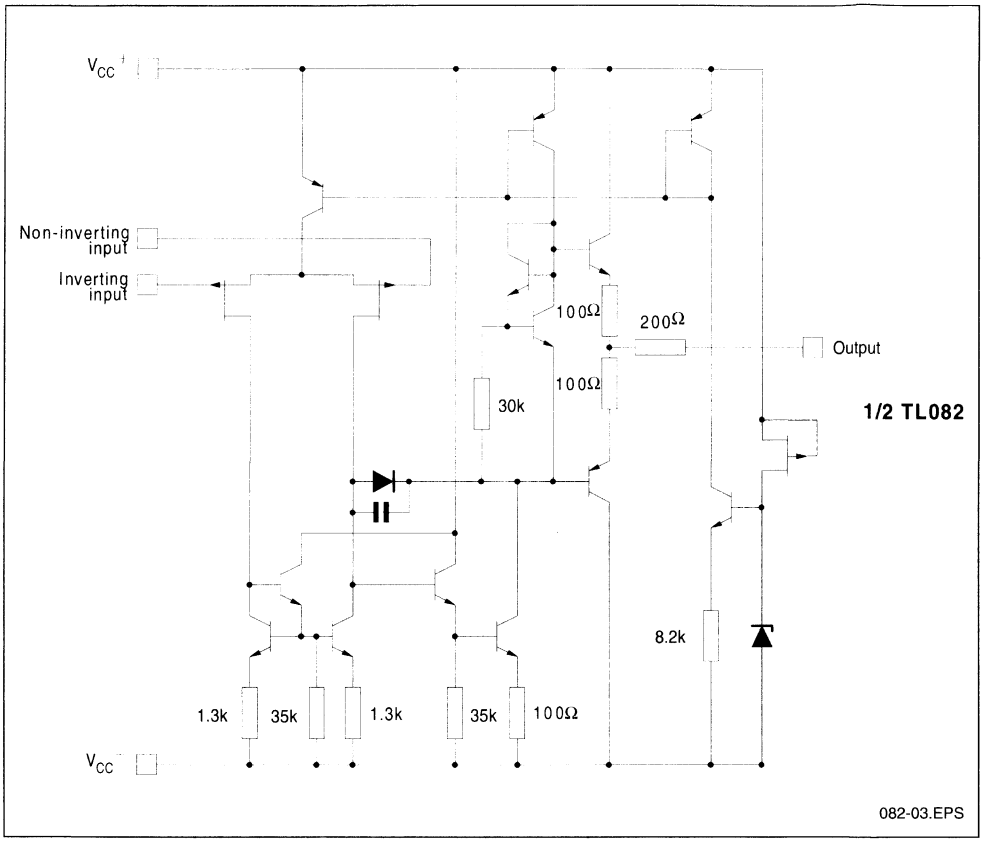
DIP8/CERDIP8
SO8



082-02.EPS

1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^-
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - V_{CC}^+

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage - (note 1)		±18	V
V_i	Input Voltage - (note 3)		±15	V
V_{id}	Differential Input Voltage - (note 2)		±30	V
P_{tot}	Power Dissipation		680	mW
	Output Short-circuit Duration - (note 4)		Infinite	
T_{oper}	Operating Free Air Temperature Range	TL082C,AC,BC TL082I,AI,BI TL082M,AM,BM	0 to 70 –40 to 105 –55 to 125	°C
T_{stg}	Storage Temperature Range		–65 to 150	°C

Notes :
1. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.
2. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and /or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

ELECTRICAL CHARACTERISTICS

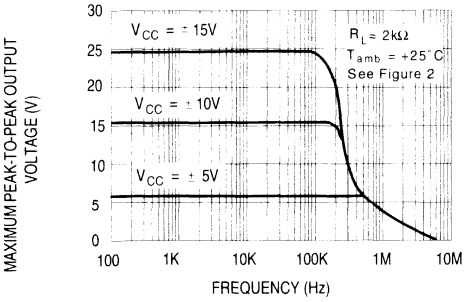
V_{CC} = ±15V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	TL082I,M,AC,AI, AM,BC,BI,BM			TL082C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage (R_S = 50Ω) T_{amb} = 25°C TL082BC,BI,BM $T_{min.} \le T_{amb} \le T_{max.}$ TL082BC,BI,BM		3 1	6 3 7 5		3	10 13	mV
DV_{io}	Input Offset Voltage Drift		10			10		µV/°C
I_{io}	Input Offset Current * T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$		5	100 4		5	100 4	pA nA
I_{ib}	Input Bias Current * T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$		20	200 20		20	400 20	pA nA
A_{vd}	Large Signal Voltage Gain (R_L = 2kΩ, V_O = ±10V) T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$	50 25	200		25 15	200		V/mV
SVR	Supply Voltage Rejection Ratio (R_S = 50Ω) T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$	80 80	86		70 70	86		dB
I_{CC}	Supply Current, per Amp, no Load T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$		1.4	2.5 2.5		1.4	2.5 2.5	mA
V_{icm}	Input Common Mode Voltage Range	±11	+15 -12		±11	+15 -12		V
CMR	Common Mode Rejection Ratio (R_S = 50Ω) T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$	80 80	86		70 70	86		dB
Ios	Output Short-circuit Current T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$	10 10	40	60 60	10 10	40	60 60	mA
$\pm V_{OPP}$	Output Voltage Swing T_{amb} = 25°C R_L = 2kΩ R_L = 10kΩ $T_{min.} \le T_{amb} \le T_{max.}$ R_L = 2kΩ R_L = 10kΩ	10 12 10 12	12 13.5		10 12 10 12	12 13.5		V
SR	Slew Rate (V_{in} = 10V, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)	8	16		8	16		V/µs
t_r	Rise Time (V_{in} = 20mV, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)		0.1			0.1		µs
K_{OV}	Overshoot (V_{in} = 20mV, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)		10			10		%
GBP	Gain Bandwidth Product (f = 100kHz, T_{amb} = 25°C, V_{in} = 10mV, R_L = 2kΩ, C_L = 100pF)	2.5	4		2.5	4		MHz
R_i	Input Resistance		10^{12}			10^{12}		Ω
THD	Total Harmonic Distortion (f = 1kHz, A_V = 20dB, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, V_O = $2V_{PP}$)		0.01			0.01		%
e_n	Equivalent Input Noise Voltage (f = 1kHz, R_s = 100Ω)		15			15		$\frac{nV}{\sqrt{Hz}}$
Øm	Phase Margin		45			45		Degrees
V_{O1}/V_{O2}	Channel Separation (A_v = 100)		120			120		dB

* The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature.

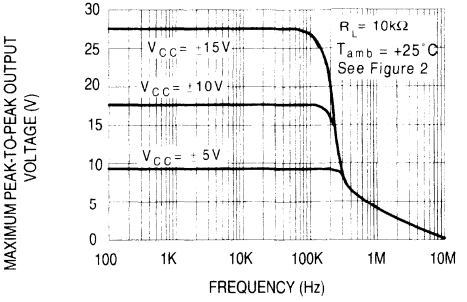
082-03.TBL

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



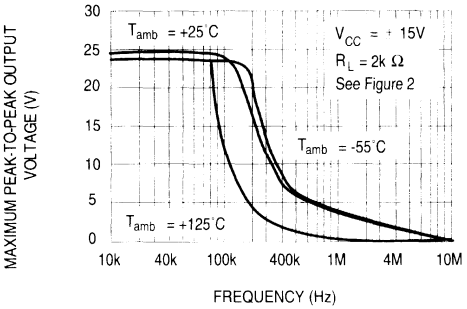
082-04.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



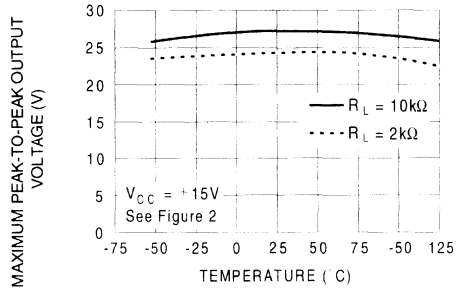
082-05.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



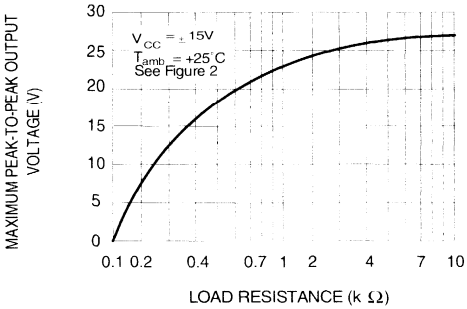
082-06.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREE AIR TEMP.



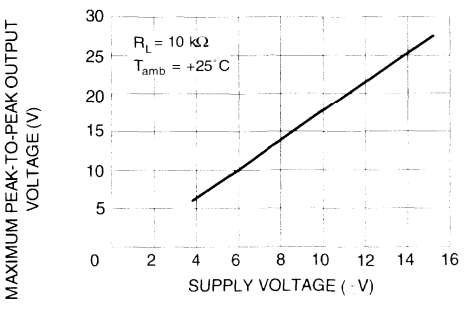
082-07.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS LOAD RESISTANCE



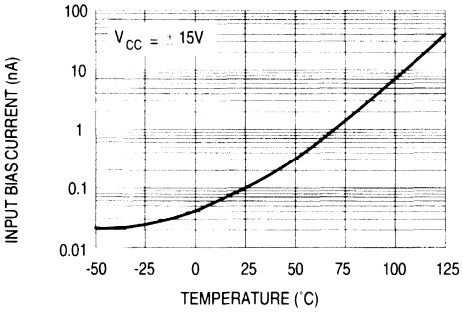
082-08.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS SUPPLY VOLTAGE



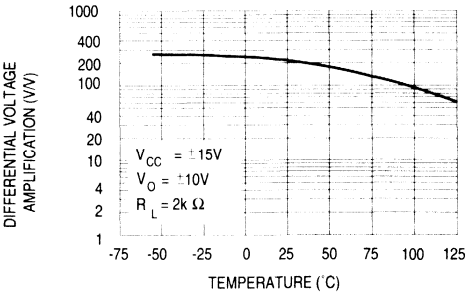
082-09.EPS

INPUT BIAS CURRENT VERSUS FREE AIR TEMPERATURE



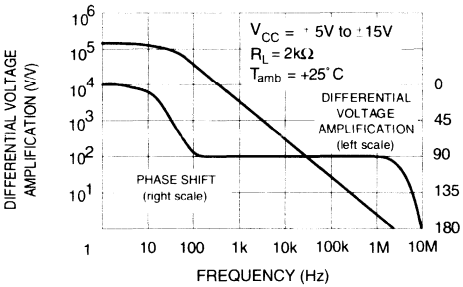
082-10.EPS

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION VERSUS FREE AIR TEMPERATURE



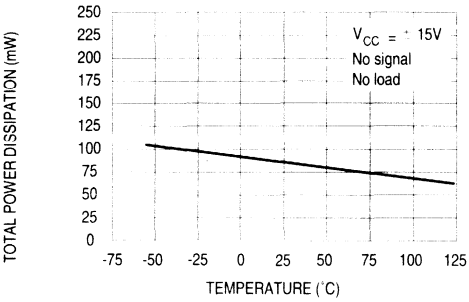
082-11.EPS

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT VERSUS FREQUENCY



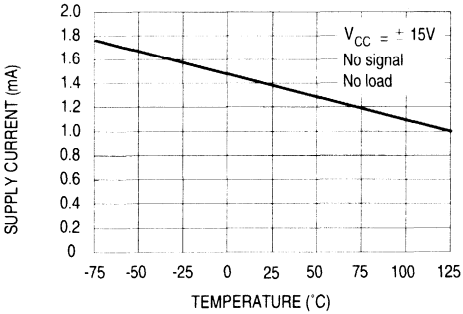
082-12.EPS

TOTAL POWER DISSIPATION VERSUS FREE AIR TEMPERATURE



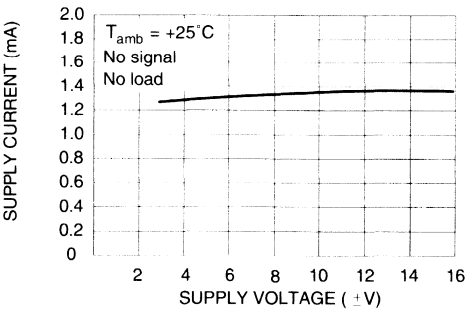
082-13.EPS

SUPPLY CURRENT PER AMPLIFIER VERSUS FREE AIR TEMPERATURE



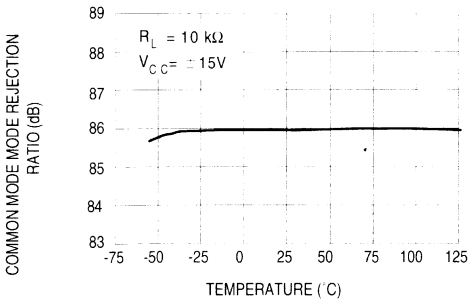
082-14.EPS

SUPPLY CURRENT PER AMPLIFIER VERSUS SUPPLY VOLTAGE



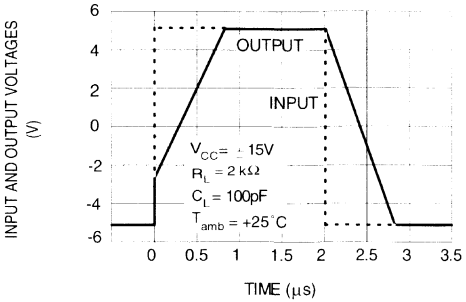
082-15.EPS

COMMON MODE REJECTION RATIO VERSUS FREE AIR TEMPERATURE



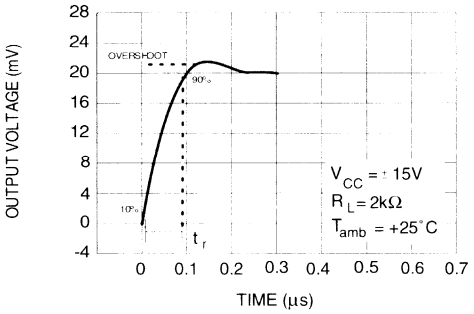
082-16.EPS

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



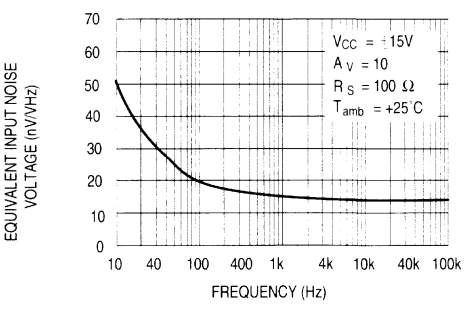
082-17.EPS

OUTPUT VOLTAGE VERSUS ELAPSED TIME



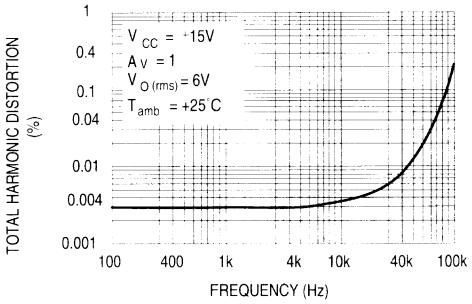
082-18.EPS

EQUIVALENT INPUT NOISE VOLTAGE VERSUS FREQUENCY



082-19.EPS

TOTAL HARMONIC DISTORTION VERSUS FREQUENCY



082-20.EPS

PARAMETER MEASUREMENT INFORMATION

Figure 1 : Voltage Follower

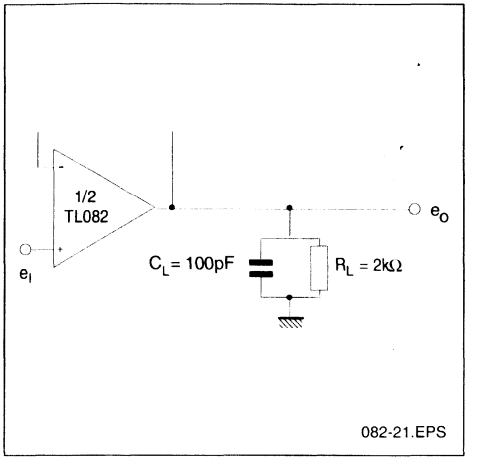
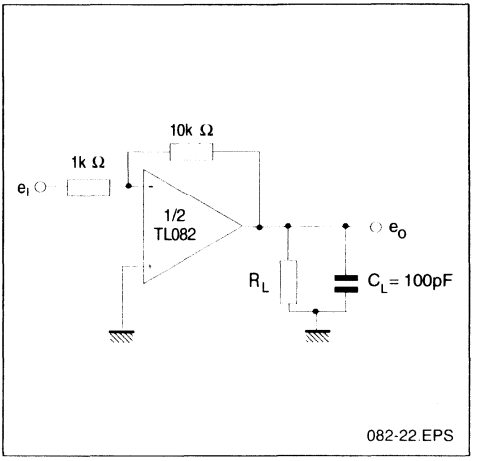
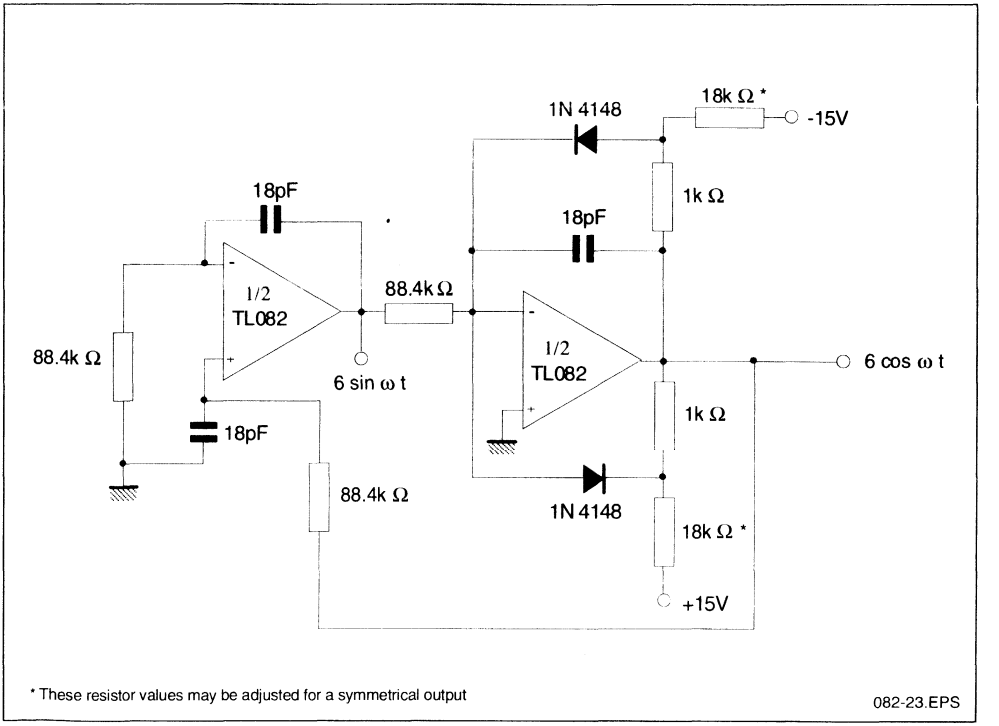


Figure 2 : Gain-of-10 Inverting Amplifier



TYPICAL APPLICATION

100KHz QUADRUPLE OSCILLATOR

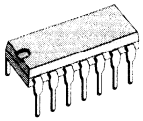


SGS-THOMSON MICROELECTRONICS

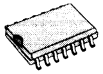
TL084
TL084A - TL084B

GENERAL PURPOSE QUAD J-FET OPERATIONAL AMPLIFIERS

- LOW POWER CONSUMPTION
- WIDE COMMON-MODE (UP TO V_{CC}^+) AND DIFFERENTIAL VOLTAGE RANGE
- LOW INPUT BIAS AND OFFSET CURRENT
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J-FET INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : 16V/µs (typ)



N
DIP14
(Plastic Package)
J
CERDIP14
(Cerdip Package)



D
SO14
(Plastic Micropackage)

DESCRIPTION

The TL084, TL084A and TL084B are high speed J-FET input quad operational amplifiers incorporating well matched, high voltage J-FET and bipolar transistors in a monolithic integrated circuit.

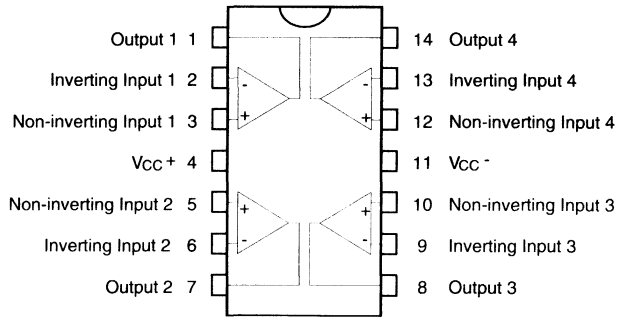
The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.

ORDER CODES

Part Number	Temperature	Package		
		N	J	D
TL084M/AM/BM	–55°C, +125°C	•	•	•
TL084I/AI/BI	–40°C, +105°C	•	•	•
TL084C/AC/BC	0°C, +70°C	•	•	•
Examples : TL084CN, TL084CD				

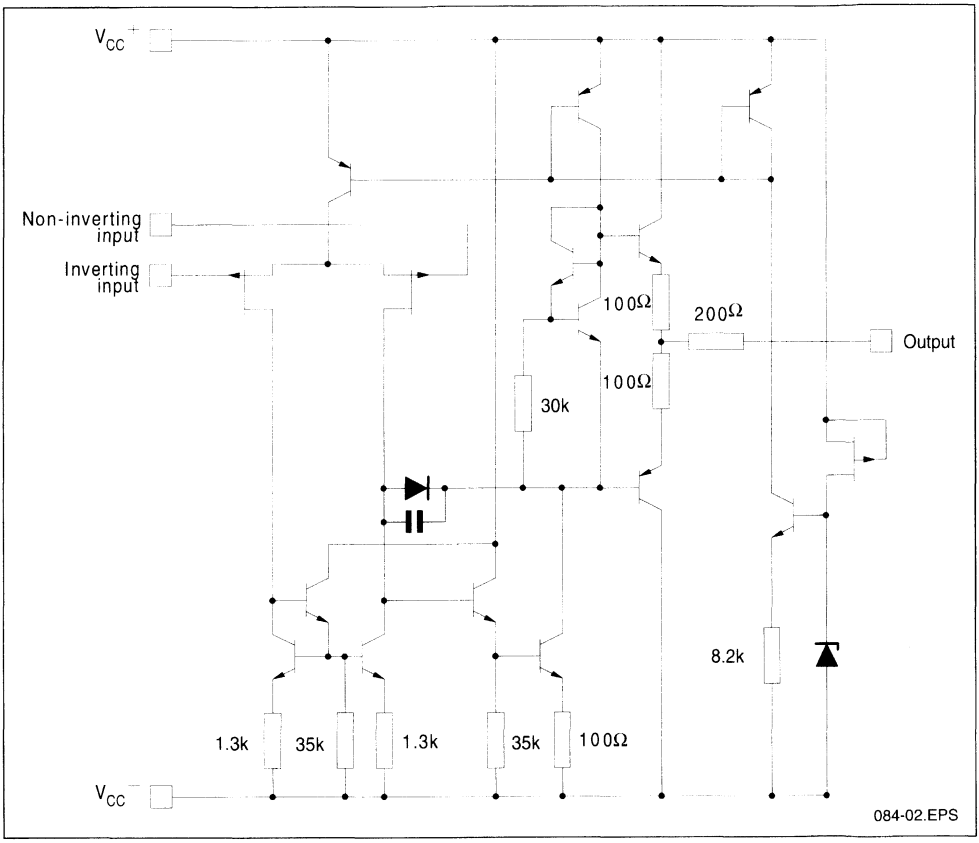
084-01.TBL

PIN CONNECTIONS (top view)



084-01.EPS

SCHEMATIC DIAGRAM (each amplifier)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage - (note 1)		±18	V
V_i	Input Voltage - (note 3)		±15	V
V_{id}	Differential Input Voltage - (note 2)		±30	V
P_{tot}	Power Dissipation		680	mW
	Output Short-circuit Duration - (note 4)		Infinite	
T_{oper}	Operating Free Air Temperature Range	TL084C,AC,BC TL084I,AI,BI TL084M,AM,BM	0 to 70 –40 to 105 –55 to 125	°C
T_{stg}	Storage Temperature Range		–65 to 150	°C

Notes :
1. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.
2. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and /or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

084-02 TRI

ELECTRICAL CHARACTERISTICS

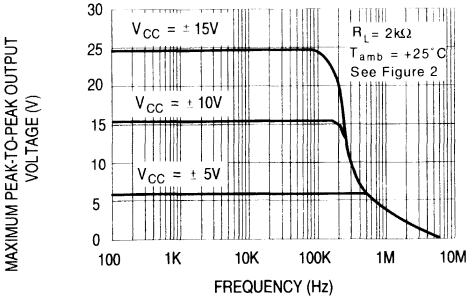
V_{CC} = ±15V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	TL084I,M,AC,AI, AM,BC,BI,BM			TL084C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage (R_S = 50Ω) T_{amb} = 25°C TL084BC,BI,BM $T_{min.} \le T_{amb} \le T_{max.}$ TL084BC,BI,BM		 3 1	 6 3 7 5		 3	 10 13	mV
DV_{io}	Input Offset Voltage Drift		10			10		µV/°C
I_{io}	Input Offset Current * T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$		 5	 100 4		 5	 100 4	 pA nA
I_{ib}	Input Bias Current * T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$		 20	 200 20		 30	 400 20	 pA nA
A_{vd}	Large Signal Voltage Gain (R_L = 2kΩ, V_O = ±10V) T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$	 50 25	 200		 25 15	 200		V/mV
SVR	Supply Voltage Rejection Ratio (R_S = 50Ω) T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$	 80 80	 86		 70 70	 86		dB
I_{CC}	Supply Current, per Amp, no Load T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$		 1.4	 2.5 2.5		 1.4	 2.5 2.5	mA
V_{icm}	Input Common Mode Voltage Range	±11	+15 -12		±11	+15 -12		V
CMR	Common Mode Rejection Ratio (R_S = 50Ω) T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$	 80 80	 86		 70 70	 86		dB
Ios	Output Short-circuit Current T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$	 10 10	 40	 60 60	 10 10	 40	 60 60	mA
$\pm V_{OPP}$	Output Voltage Swing T_{amb} = 25°C R_L = 2kΩ R_L = 10kΩ $T_{min.} \le T_{amb} \le T_{max.}$ R_L = 2kΩ R_L = 10kΩ	 10 12 10 12	 12 13.5		 10 12 10 12	 12 13.5		V
SR	Slew Rate (V_{in} = 10V, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)	8	16		8	16		V/µs
t_r	Rise Time (V_{in} = 20mV, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)		0.1			0.1		µs
K_{OV}	Overshoot (V_{in} = 20mV, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)		10			10		%
GBP	Gain Bandwidth Product (f = 100kHz, T_{amb} = 25°C, V_{in} = 10mV, R_L = 2kΩ, C_L = 100pF)	2.5	4		2.5	4		MHz
R_i	Input Resistance		10^{12}			10^{12}		Ω
THD	Total Harmonic Distortion (f = 1kHz, A_V = 20dB, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, V_O = 2V_{PP})		0.01			0.01		%
e_n	Equivalent Input Noise Voltage (f = 1kHz, R_s = 100Ω)		15			15		$\frac{nV}{\sqrt{Hz}}$
Øm	Phase Margin		45			45		Degrees
V_{O1}/V_{O2}	Channel Separation (A_v = 100)		120			120		dB

* The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature.

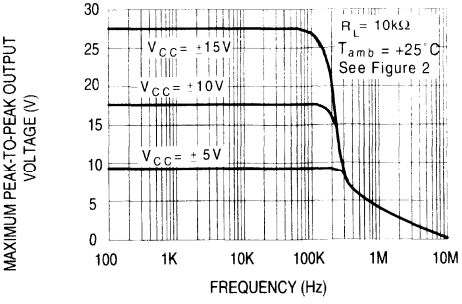
084-03.TBL

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



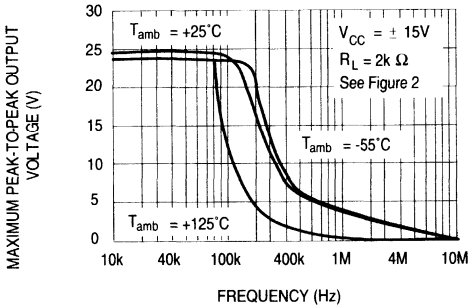
084-03.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



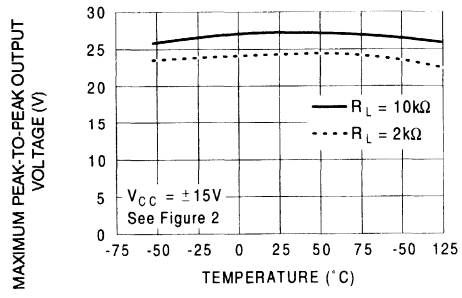
084-04.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



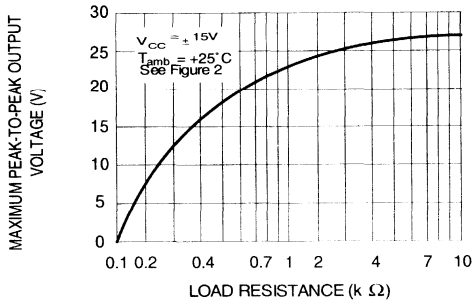
084-05.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREE AIR TEMP.



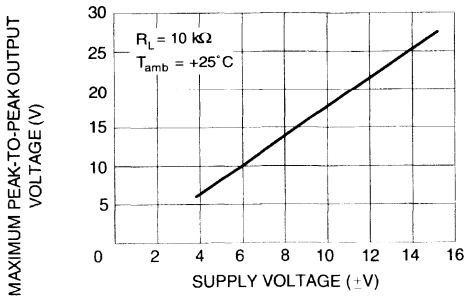
084-06.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS LOAD RESISTANCE



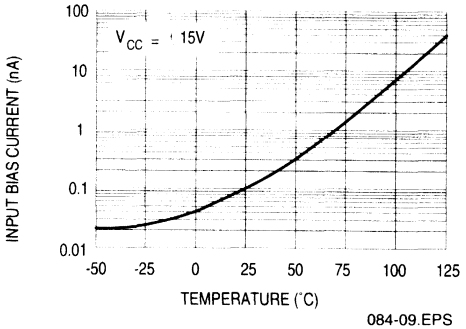
084-07.EPS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS SUPPLY VOLTAGE



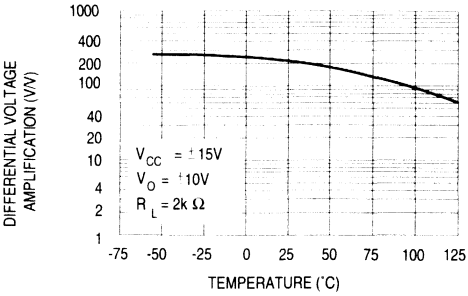
084-08.EPS

INPUT BIAS CURRENT VERSUS FREE AIR TEMPERATURE



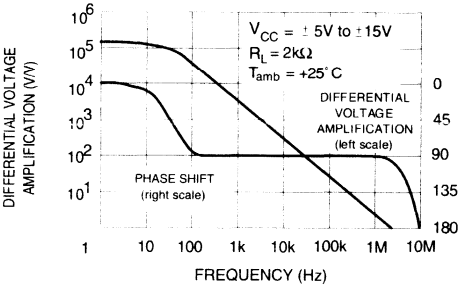
084-09.EPS

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION VERSUS FREE AIR TEMPERATURE



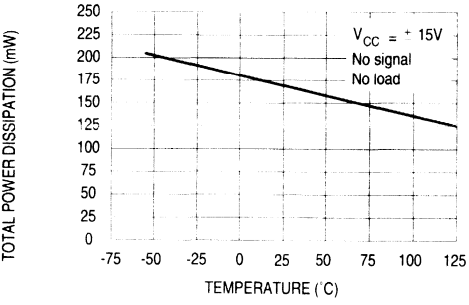
084-10.EPS

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT VERSUS FREQUENCY



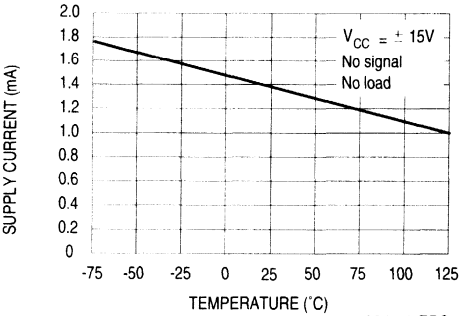
084-11.EPS

TOTAL POWER DISSIPATION VERSUS FREE AIR TEMPERATURE



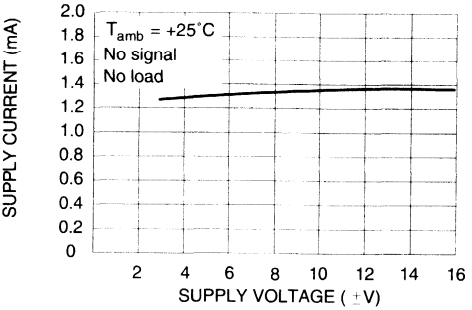
084-12.EPS

SUPPLY CURRENT PER AMPLIFIER VERSUS FREE AIR TEMPERATURE



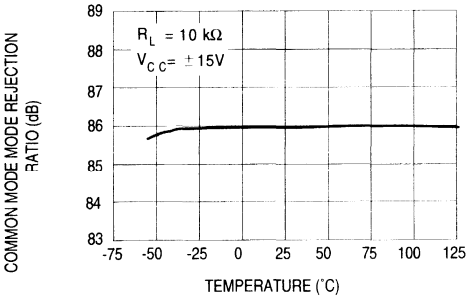
084-13.EPS

SUPPLY CURRENT PER AMPLIFIER VERSUS SUPPLY VOLTAGE



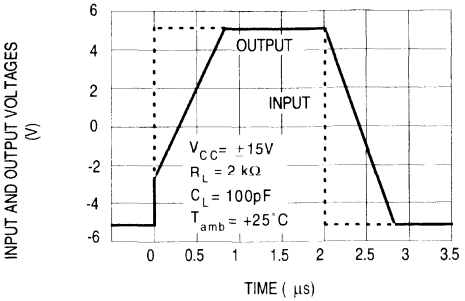
084-14.EPS

COMMON MODE REJECTION RATIO VERSUS FREE AIR TEMPERATURE



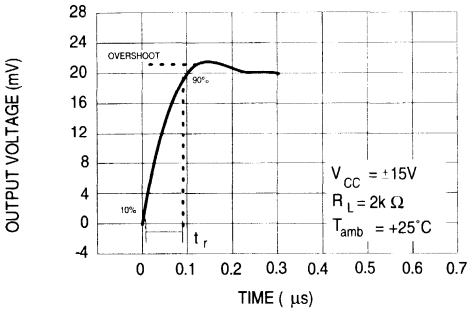
084-15.EPS

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



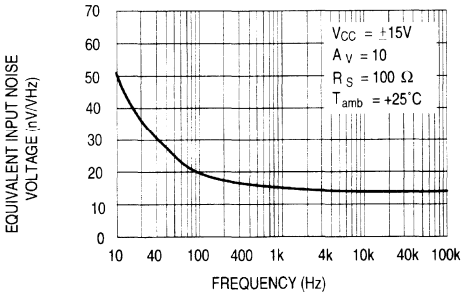
084-16.EPS

OUTPUT VOLTAGE VERSUS ELAPSED TIME



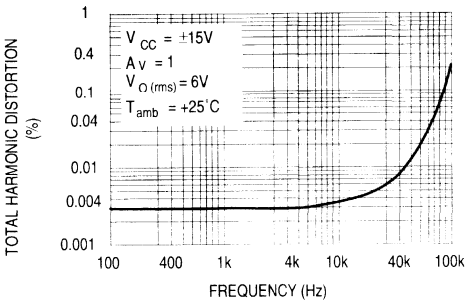
084-17.EPS

EQUIVALENT INPUT NOISE VOLTAGE VERSUS FREQUENCY



084-18.EPS

TOTAL HARMONIC DISTORTION VERSUS FREQUENCY



084-19.EPS

PARAMETER MEASUREMENT INFORMATION

Figure 1 : Voltage Follower

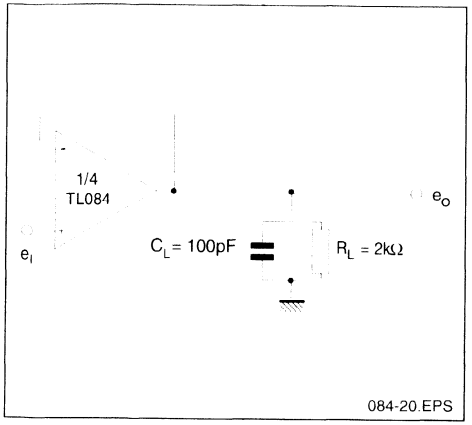
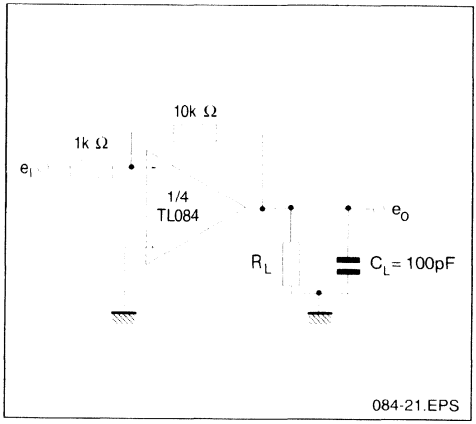
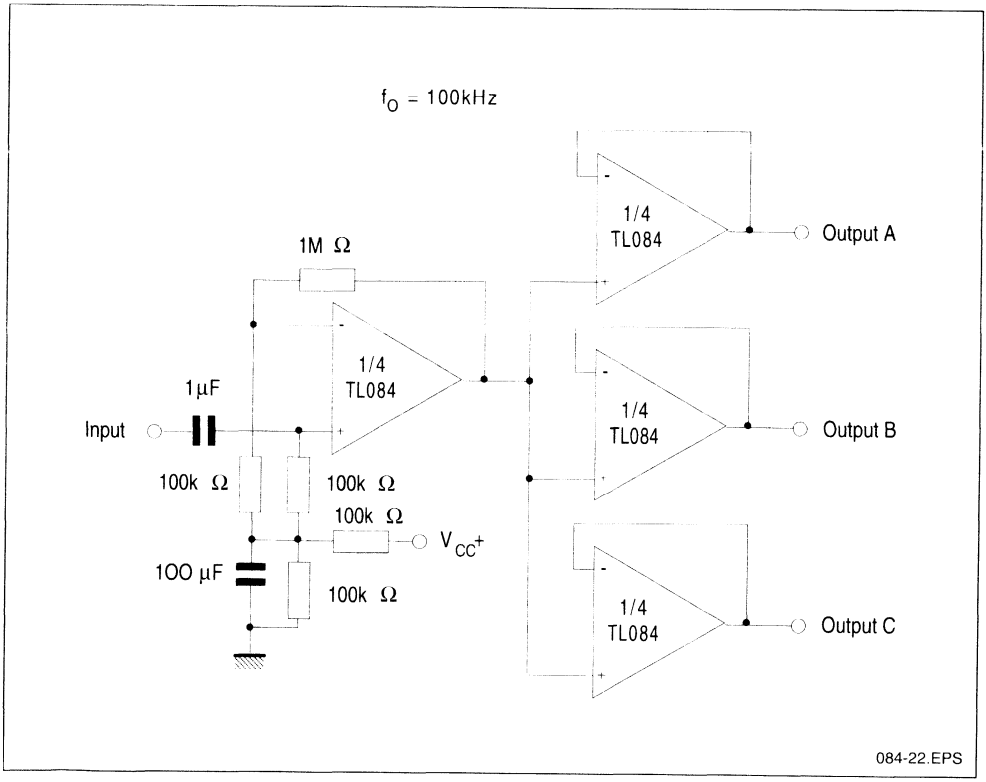


Figure 2 : Gain-of-10 Inverting Amplifier



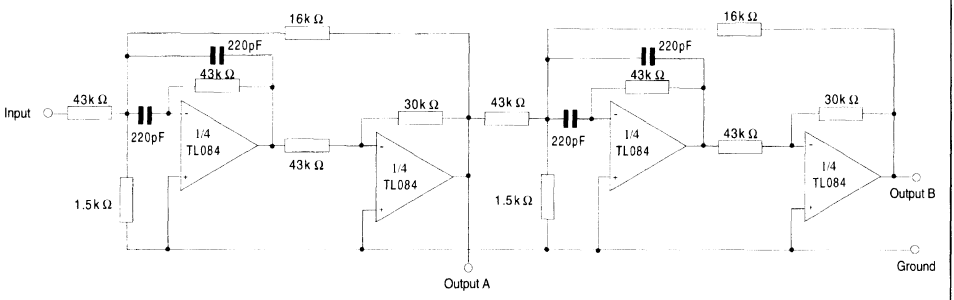
TYPICAL APPLICATIONS

AUDIO DISTRIBUTION AMPLIFIER



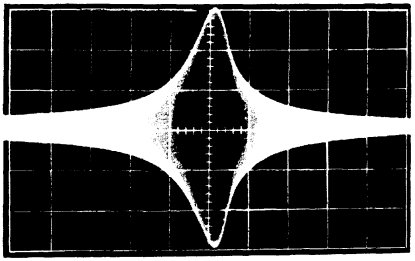
TYPICAL APPLICATIONS (continued)

POSITIVE FEEDBACK BANDPASS FILTER



084-23.EPS

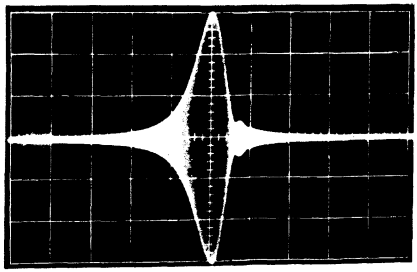
OUTPUT A



084-24.EPS

SECOND ORDER BANDPASS FILTER
fo = 100kHz ; Q = 30 ; Gain = 4

OUTPUT B



084-25.EPS

CASCADED BANDPASS FILTER
fo = 100kHz ; Q = 69 ; Gain = 16

SUPPLY VOLTAGE SUPERVISORS

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST/1)

- POWER-ON RESET GENERATOR
- AUTOMATIC RESET GENERATION AFTER VOLTAGE DROP
- WIDE SUPPLY VOLTAGE RANGE ... 3 V TO 18 V
- PRECISION VOLTAGE SENSOR
- TEMPERATURE-COMPENSATED VOLTAGE REFERENCE
- TRUE AND COMPLEMENT RESET OUTPUTS
- EXTERNALLY ADJUSTABLE PULSE WIDTH

Minidip

SO8

ORDERING NUMBERS		
Temperature Range	Minidip	SO8
0 to 70 °C	TL77XXACP	TL77XXACD
– 25 to 85 °C	TL77XXAIP	TL77XXAID

DESCRIPTION

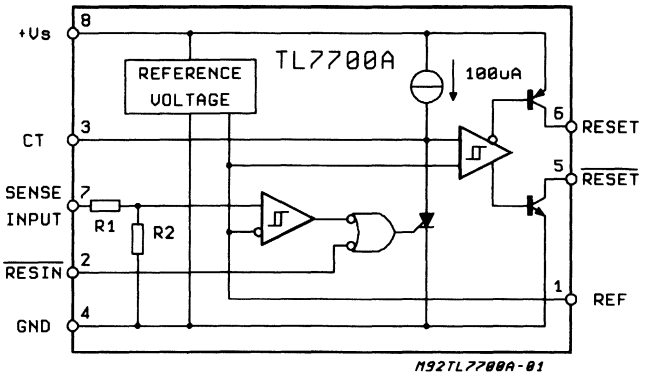
The TL7700A series are monolithic integrated circuit supply voltage supervisors specifically desi-gned for use as reset controllers in microcomputer and microprocessor systems. During power-up the device tests the supply voltage and keeps the RESET and $\overline{\text{RESET}}$ outputs active (high and low, respectively) as long as the supply voltage has not reached its nominal voltage value. Taking $\overline{\text{RESIN}}$ low has the same effect. To ensure that the microcomputer system has reset. the TL7700A then initiates an internal time delay that delays the return of the reset outputs to their inactive states. Since the time delay for most microcomputers and microprocessors is in the order of several machine cycles, the device internal time delay is determined by an external time delay is determined by an external capacitor connected to the C_T input (pin 3).

$t_d = 1.3 \times 10^4 \times C_T$

Where : C_T is in farads (F) and t_d in seconds (s). In addition, when the supply voltage drops below the nominal value, the outputs will be active until the supply voltage returns to the nominal value. An external capacitor (typically 0.1 µF) must be connected to the REF output (pin 1) to reduce the influence of fast transients in the supply voltage.

The TL7700AI series is characterized for operation from – 25°C to 85°C ; the TL7700AC series is characterized from 0°C to 70°C.

BLOCK DIAGRAM



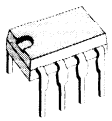
* TL7702A R1 = 0Ω, R2 = open ; TL7705A R1 = 7.8 KΩ, R2 = 10 KΩ ; TL7709A R1 = 19.7 KΩ, R2 = 10 KΩ ; TL7712A R1 = 32.7 KΩ, R2 = 10 KΩ ; TL7715A R1 = 43.4 KΩ, R2 = 10 KΩ.

SGS-THOMSON MICROELECTRONICS

TS3V555C/I/AC/AI

LOW POWER SINGLE CMOS TIMERS

- DEDICATED FOR 3.3V OR BATTERY SUPPLY (Specified at 3V and 5V plus 1.5V for A version)
- VERY LOW POWER CONSUMPTION : 90µA at V_{CC} = 3V
- PIN-TO-PIN AND FUNCTIONALLY COMPATIBLE WITH BIPOLAR NE555 AND CMOS TS555
- VOLTAGE RANGE : +1.5V to +18V
- HIGH OUTPUT CURRENT CAPABILITY
- SUPPLY CURRENT SPIKES REDUCED DURING OUTPUT TRANSITIONS
- HIGH INPUT IMPEDANCE : 10^{12} Ω
- OUTPUT COMPATIBLE WITH TTL,CMOS AND LOGIC MOS



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

DESCRIPTION

The TS3V555 with its low consumption (90µA at V_{CC} = 3V) is a single CMOS timer dedicated for 3.3V or battery supply (specified at 3V and 5V plus 1.5V for A version) offering also a high frequency ($f_{(max)}$ 2MHz at V_{CC} = 3V and 2.7 MHz at V_{CC} = 5V). Thus, either in monostable or astable mode, timing remains very accurate.

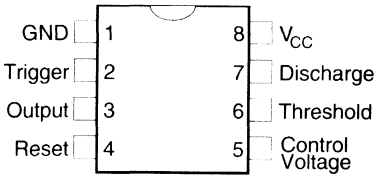
Timing capacities can also be minimized due to high input impedance (10^{12} Ω).

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS3V555C/AC	0, +70°C	●	●
TS3V555I/AI	-40, +105°C	●	●

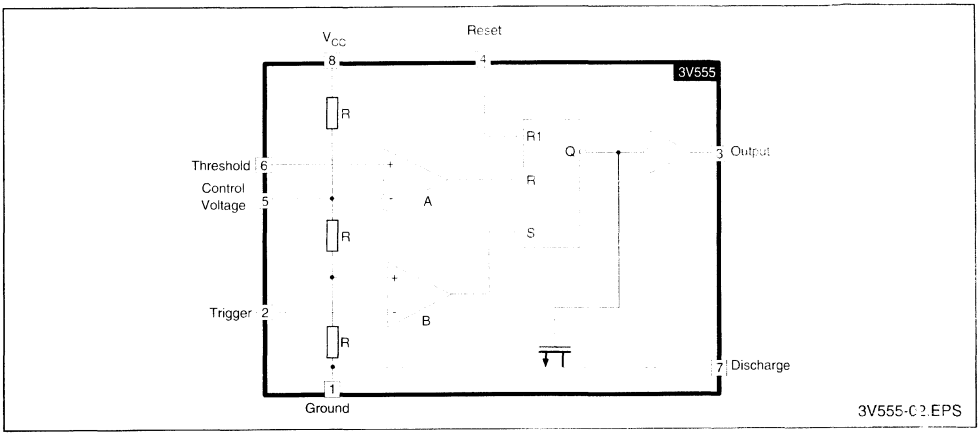
3V555-01.TBL

PIN CONNECTIONS (top view)



3V555-01.EPS

BLOCK DIAGRAM



FUNCTION TABLE

RESET	TRIGGER	THRESHOLD	OUTPUT
Low	x	x	Low
High	Low	x	High
High	High	High	Low
High	High	Low	Previous State

LOW ↔ Level Voltage ≤ Min voltage specified

HIGH ↔ Level Voltage ≥ Max voltage specified

X ↔ Irrelevant

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	+18	V
T_J	Junction Temperature	+150	°C

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
T_{oper}	Operating Temperature Range TS3V555C,AC TS3V555I,AI	 0 to +70 -40 to +105	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	+1.5 to +16	V

ELECTRICAL CHARACTERISTICS

V_{CC} = +3V , T_{amb} = +25°C , Reset to V_{CC} (unless otherwise specified)

STATIC

Symbol	Parameter	TS3V555C,I,AC,AI			Unit
		Min.	Typ.	Max.	
I_{CC}	Supply Current - (no load, High and Low States) T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$		90	230 230	µA
V_{CL}	Control Voltage T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$	1.8 1.7	2	2.2 2.3	V
V_{DIS}	Discharge Saturation Voltage (I_{DIS} = 1mA) T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$		0.05 -	0.2 0.25	V
V_{OL}	Low Level Output Voltage (I_{SINK} = 1mA) T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$		0.1	0.3 0.35	V
V_{OH}	High Level Output Voltage (I_{SOURCE} = -0.3mA) T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$	2.5 2.5	2.9		V
V_{TRIG}	Trigger Voltage T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$	0.9 0.8	1	1.1 1.2	V
I_{TRIG}	Trigger Current		10		pA
I_{TH}	Threshold Current		10		pA
V_{RESET}	Reset Voltage T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$	0.4 0.3	1.1	1.5 2.0	V
I_{RESET}	Reset Current		10		pA
I_{DIS}	Discharge Pin Leakage Current		1	100	nA

3V555-06.TBL

DYNAMIC

Symbol	Parameter	TS3V555C,I,AC,AI			Unit
		Min.	Typ.	Max.	
	Timing Accuracy (Monostable) R = 10kΩ , C = 0.1µF - (note 1)		1		%
	Timing Shift with supply voltage variations (Monostable) R = 10kΩ , C = 0.1µF, V_{CC} = +3V +/-0.3V		0.5		%/V
	Timing Shift with temperature $T_{min.} \le T_{amb} \le T_{max.}$		75		ppm/°C
fmax	Maximum astable frequency R_A = 470Ω , R_B = 200Ω, C = 200pF		2		MHz
	Astable frequency accuracy - (note 2) $R_A = R_B$ = 1kΩ to 100kΩ, C = 0.1µF		5		%
	Timing Shift with supply voltage variations (Astable mode) $R_A = R_B$ = 10kΩ, C = 0.1µF, V_{CC} = +3 to+5V		0.5		%/V
t_r	Output Rise Time (C_{LOAD} = 10pF)		25		ns
t_f	Output Fall Time (C_{LOAD} = 10pF)		20		ns
t_{PD}	Trigger Propagation Delay		100		ns
t_{RPW}	Minimum Reset Pulse Width (V_{TRIG} = +3V)		350		ns

3V555-07.TBL

Note : 1. See Figure 2
2. See Figure 4

ELECTRICAL CHARACTERISTICS

V_{CC} = +5V , T_{amb} = +25°C , Reset to V_{CC} (unless otherwise specified)

STATIC

Symbol	Parameter	TS3V555C,I,AC,AI			Unit
		Min.	Typ.	Max.	
I_{CC}	Supply Current - (no load, High and Low States) T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$		110	250 250	µA
V_{CL}	Control Voltage T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$	2.9 2.8	3.3	3.8 3.9	V
V_{DIS}	Discharge Saturation Voltage (I_{DIS} = 10mA) T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$		0.2	0.3 0.35	V
V_{OL}	Low Level Output Voltage (I_{SINK} = 8mA) T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$		0.3	0.6 0.8	V
V_{OH}	High Level Output Voltage (I_{SOURCE} = -2mA) T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$	4.4 4.4	4.6		V
V_{TRIG}	Trigger Voltage T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$	1.36 1.26	1.67	1.96 2.06	V
I_{TRIG}	Trigger Current		10		pA
I_{TH}	Threshold Current		10		pA
V_{RESET}	Reset Voltage T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$	0.4 0.3	1.1	1.5 2.0	V
I_{RESET}	Reset Current		10		pA
I_{DIS}	Discharge Pin Leakage Current		1	100	nA

DYNAMIC

Symbol	Parameter	TS3V555C,I,AC,AI			Unit
		Min.	Typ.	Max.	
	Timing Accuracy (Monostable) R = 10kΩ , C = 0.1µF - (note 1)		2		%
	Timing Shift with supply voltage variations (Monostable) R = 10kΩ , C = 0.1µF, V_{CC} = +5V +/-1V		0.38		%/V
	Timing Shift with temperature $T_{min.} \le T_{amb} \le T_{max.}$		75		ppm/°C
fmax	Maximum astable frequency R_A = 470Ω , R_B = 200Ω, C = 200pF		2.7		-
	Astable frequency accuracy - (note 2) R_A = R_B = 1kΩ to 100kΩ, C = 0.1µF		3		%
	Timing Shift with supply voltage variations (Astable mode) R_A = R_B = 10kΩ, C = 0.1µF, V_{CC} = +5V to+12V		0.1		%/V
t_r	Output Rise Time (C_{LOAD} = 10pF)		25		ns
t_f	Output Fall Time (C_{LOAD} = 10pF)		20		ns
t_{PD}	Trigger Propagation Delay		100		ns
t_{RPW}	Minimum Reset Pulse Width (V_{TRIG} = +5V)		350		ns

Note : 1. See Figure 2
2. See Figure 4

ELECTRICAL CHARACTERISTICS

TS3V555AC,AI only

V_{CC} = +1.5V , T_{amb} = +25°C, Reset to V_{CC} (unless otherwise specified)

STATIC

Symbol	Parameter	TS3V555AC,AI			Unit
		Min.	Typ.	Max.	
I_{CC}	Supply Current - (no load, High and Low States) T_{amb} = +25°C		50	150	µA
V_{CL}	Control Voltage T_{amb} = +25°C	0.8	1.0	1.2	V
V_{DIS}	Discharge Saturation Voltage (I_{DIS} = 1mA) T_{amb} = +25°C		75	150	mV
V_{OL}	Low Level Output Voltage (I_{SINK} = 1mA) T_{amb} = +25°C		0.2	0.4	V
V_{OH}	High Level Output Voltage (I_{SOURCE} = -0.25mA) T_{amb} = +25°C	1.0	1.25		V
V_{TRIG}	Trigger Voltage T_{amb} = +25°C	0.4	0.5	0.6	V
I_{TRIG}	Trigger Current		10		pA
I_{TH}	Threshold Current		10		pA
V_{RESET}	Reset Voltage T_{amb} = +25°C	0.4	1.1	1.4	V
I_{RESET}	Reset Current		10		pA

3V555-10.TBL

DYNAMIC

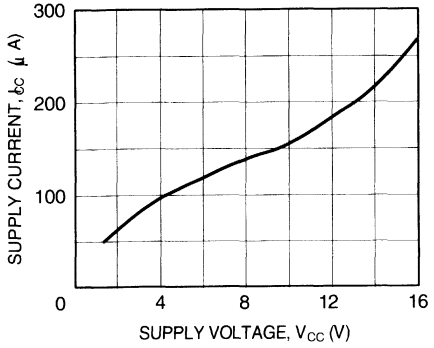
Symbol	Parameter	TS3V555AC,AI			Unit
		Min.	Typ.	Max.	
	Timing Accuracy (Monostable) R = 10kΩ , C = 0.1µF - (note 1)		4		%

3V555-11.TBL

Note : 1. See Figure 2

TYPICAL CHARACTERISTICS

Figure 1 : Supply Current (each timer) versus supply voltage.



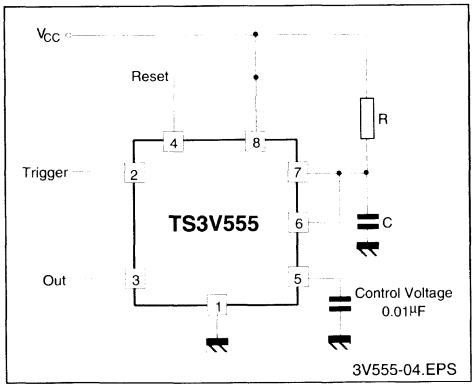
3V555-03.EPS

APPLICATION INFORMATION

MONOSTABLE OPERATION

In the monostable mode,the timer functions as a one-shot. Referring to figure 2 the external capacitor is initially held discharged by a transistor inside the timer.

Figure 2



3V555-04.EPS

The circuit triggers on a negative-going input signal when the level reaches 1/3 V_{CC}. Once triggered,the circuit remains in this state until the set time has elapsed,even if it is triggered again during this interval. The duration of the output HIGH state is given by t = 1.1 R x C.

Notice that since the charge rate and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the Reset terminal (pin 4) and the Trigger terminal (pin 2) during the timing cycle discharges the external capacitor and causes the cycle to start over. The timing cycle now starts on the positive edge of the reset pulse. During the time the reset pulse is applied, the output is driven to its LOW state.

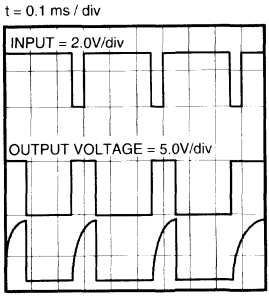
When a negative trigger pulse is applied to pin 2, the flip-flop is set, releasing the short circuit across the external capacitor and driving the output HIGH. The voltage across the capacitor increases exponentially with the time constant τ = R x C.

When the voltage across the capacitor equals 2/3 V_{CC}, the comparator resets the flip-flop which then discharges the capacitor rapidly and drives the output to its LOW state.

Figure 3 shows the actual waveforms generated in this mode of operation.

When Reset is not used, it should be tied high to avoid any possible or false triggering.

Figure 3



3V555-05.EPS

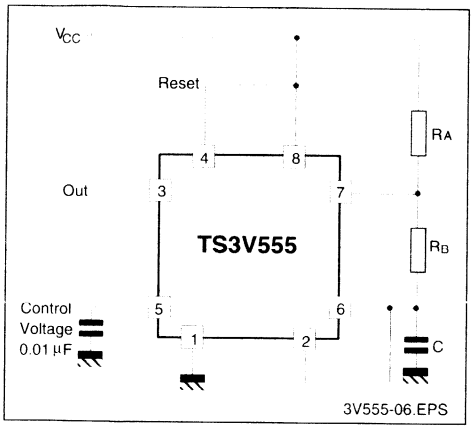
ASTABLE OPERATION

When the circuit is connected as shown in figure 4 (pin 2 and 6 connected) it triggers itself and free runs as a multivibrator. The external capacitor charges through R_A and R_B and discharges through R_B only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

In the astable mode of operation, C charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times and therefore frequency, are independent of the supply voltage.

Figure 5 shows actual waveforms generated in this mode of operation.

Figure 4



The charge time (output HIGH) is given by :

$t1 = 0.693 (R_A + R_B) C$

and the discharge time (output LOW) by :

$t2 = 0.693 (R_B) C$

Thus the total period T is given by :

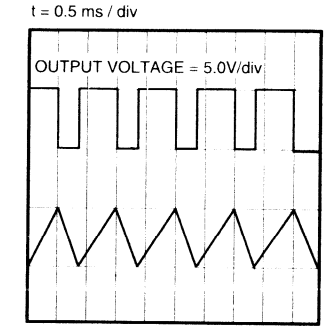
$T = t1 + t2 = 0.693 (R_A + 2R_B) C$

The frequency of oscillation is then :

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B) C}$$

The duty cycle is given by : $D = \frac{R_B}{R_A + 2R_B}$

Figure 5

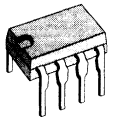


SGS-THOMSON MICROELECTRONICS

TS27L2C/I/M

VERY LOW POWER DUAL CMOS OPERATIONAL AMPLIFIERS

- EXCELLENT PHASE MARGIN ON
- CAPACITIVE LOADS
- SYMETRICAL OUTPUT CURRENTS
- LOW OUTPUT DYNAMIC IMPEDANCE
- THE TRANSFER FUNCTION IS LINEAR
- PIN TO PIN COMPATIBLE WITH STANDARD DUAL OP-AMPs (TL082 -LM358)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS27L2C/AC/BC	0°C, +70°C	•	•
TS27L2I/AI/BI	-40°C, +105°C	•	•
TS27L2M/AM/BM	-55°C, +125°C	•	•
Example : TS27L2ACN			

27L2-01.TBL

DESCRIPTION

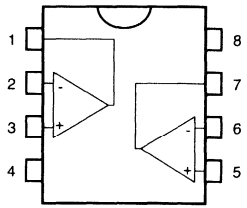
The TS272 series are low cost, low power dual operational amplifiers designed to operate with single or dual supplies. These operational amplifiers use the SGS-THOMSON silicon gate LIN MOS process giving them an excellent consumption-speed ratio. These series are ideally suited for low consumption applications.

Three power consumptions are available allowing to have always the best consumption-speed ratio :

- I_{CC}= 10µA/amp. : TS27L2 (very low power)
- I_{CC}= 150µA/amp. : TS27M2 (low power)
- I_{CC}= 1mA/amp. : TS272 (high speed)

These CMOS amplifiers offer very high input impedance and extremely low input currents. The major advantage versus JFET devices is the very low input currents drift with temperature (see figure 2).

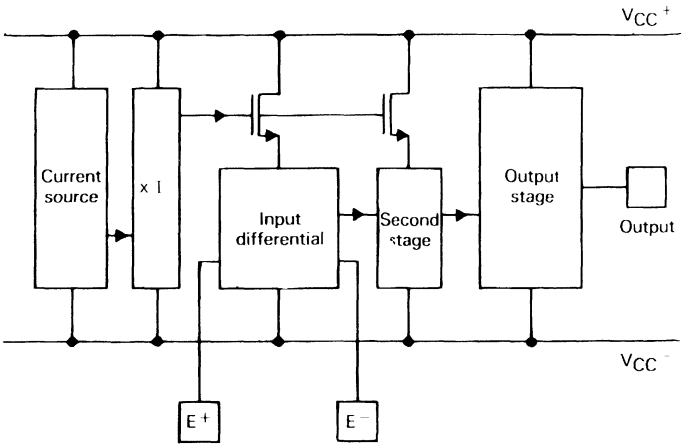
PIN CONNECTIONS (top view)



1 - Output 1
2 - Inverting Input 1
3 - Non-inverting Input 1
4 - V_{CC}^-
5 - Non-inverting Input 2
6 - Inverting Input 2
7 - Output 2
8 - V_{CC}^+

27L2-01.EPS

BLOCK DIAGRAM



27L2-02.EPS

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage - (note 1)	18	V
V_{id}	Differential Input Voltage - (note 2)	±18	V
V_i	Input Voltage - (note 3)	-0.3 to 18	V
I_O	Output Current for $V_{CC}^+ \geq 15V$	±30	mA
I_{in}	Input Current	±5	mA
T_{oper}	Operating Free-Air Temperature Range TS27L2C/AC/BC TS27L2I/AI/BI TS27L2M/AM/BM	 0 to +70 -40 to +105 -55 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

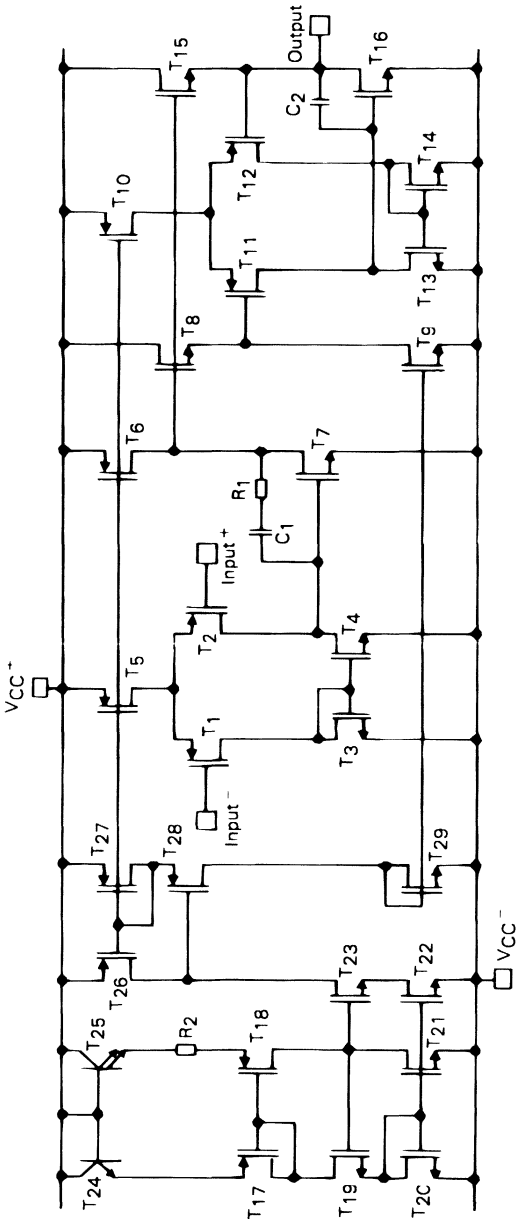
Notes : 1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input and the output voltages must never exceed the magnitude of the positive supply voltage.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage	3 * to 16	V
V_{icm}	Common Mode Input Voltage Range	0 to V_{CC}^+ - 1.5	V

* Selected devices only.

SCHEMATIC DIAGRAM (for 1/2 TS27L2)



27L2-03.EPS

ELECTRICAL CHARACTERISTICS

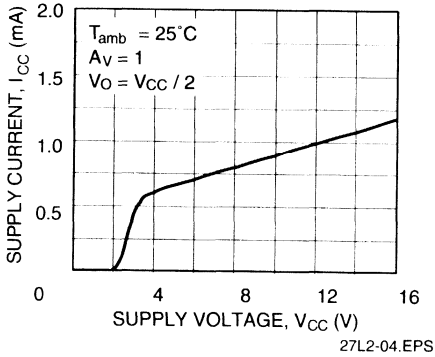
$V_{CC}^+ = +10V$, $V_{CC}^- = 0V$, $T_{amb} = 25°C$ (unless otherwise specified)

Symbol	Parameter	TS27L2C/AC/BC			TS27L2I/AI/BI TS27L2M/AM/BM			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage $V_O = 1.4V$, $V_{ic} = 0V$ TS27L2C/I/M TS27L2AC/AI/AM TS27L2BC/BI/BM $T_{min.} \le T_{amb} \le T_{max.}$ TS27L2C/I/M TS27L2AC/AI/AM TS27L2BC/BI/BM		 1.1 0.9 0.25 	 10 5 2 12 6.5 3		 1.1 0.9 0.25 	 10 5 2 12 6.5 3.5	mV
DV_{io}	Input Offset Voltage Drift		0.7			0.7		µV/°C
I_{io}	Input Offset Current - (note 1) $V_{ic} = 5V$, $V_o = 5V$ $T_{min.} \le T_{amb} \le T_{max.}$		1	 100		1	 200	pA
I_{ib}	Input Bias Current - (note 1) $V_{ic} = 5V$, $V_o = 5V$ $T_{min.} \le T_{amb} \le T_{max.}$		1	 150		1	 300	pA
V_{OH}	High Level Output Voltage $V_{id} = 100mV$, $R_L = 1M\Omega$ $T_{min.} \le T_{amb} \le T_{max.}$	8.8 8.7	9		8.8 8.6	9		V
V_{OL}	Low Level Output Voltage $V_{id} = -100mV$			50			50	mV
A_{vd}	Large Signal Voltage Gain $V_o = 1V$ to $6V$, $R_L = 1M\Omega$, $V_{ic} = 5V$ $T_{min.} \le T_{amb} \le T_{max.}$	60 45	100		60 40	100		V/mV
GBP	Gain Bandwidth Product $A_v = 40dB$, $R_L = 1M\Omega$, $C_L = 100pF$ $f_{in} = 10kHz$		0.1			0.1		MHz
CMR	Common Mode Rejection Ratio $V_o = 1.4V$, $V_{ic} = 1V$ to $7.4V$	65	80		65	80		dB
SVR	Supply Voltage Rejection Ratio $V_{CC}^+ = 5V$ to $10V$, $V_o = 1.4V$	60	80		60	80		dB
I_{CC}	Supply Current (per amplifier) $A_v = 1$, no load, $V_o = 5V$ $T_{min.} \le T_{amb} \le T_{max.}$		10	15 17		10	15 18	µA
I_o	Output Short Circuit Current $V_{id} = 100mV$, $V_o = 0V$	45	60	85	45	60	85	mA
I_{sink}	Output Sink Current $V_{id} = -100mV$, $V_o = V_{CC}$	35	45	65	35	45	65	mA
SR	Slew-Rate at Unity Gain $R_L = 1M\Omega$, $C_L = 100pF$, $V_i = 3$ to $7V$		0.04			0.04		V/µs
Øm	Phase Margin at Unity Gain $A_v = 40dB$, $R_L = 1M\Omega$, $C_L = 100pF$		45			45		Degrees
K_{ov}	Overshoot Factor		30			30		%
e_n	Equivalent Input Noise Voltage $f = 1kHz$, $R_S = 100\Omega$		68			68		$\frac{nV}{\sqrt{Hz}}$
V_{O1}/V_{O2}	Channel Separation		120			120		dB

Note : 1. Maximum values including unavoidable inaccuracies of the industrial test.

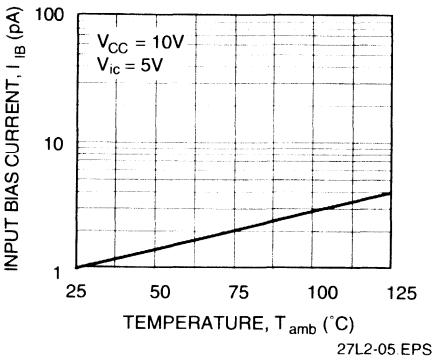
TYPICAL CHARACTERISTICS

Figure 1 : Supply Current (each amplifier) versus Supply Voltage



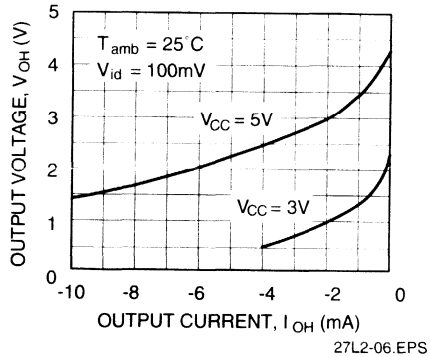
27L2-04.EPS

Figure 2 : Input Bias Current versus Free Air Temperature



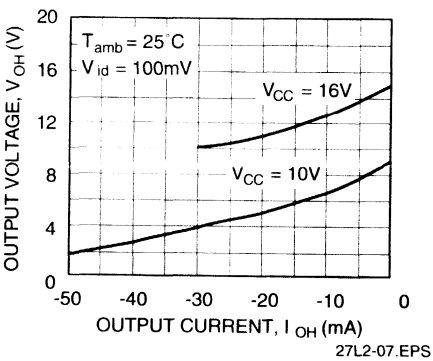
27L2-05.EPS

Figure 3a : High Level Output Voltage versus High Level Output Current



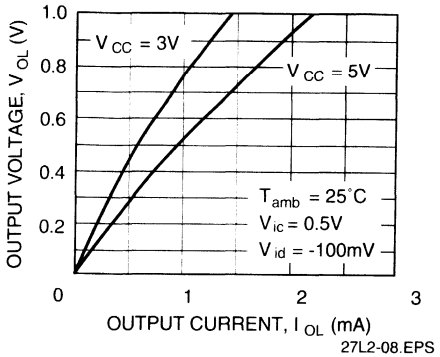
27L2-06.EPS

Figure 3b : High Level Output Voltage versus High Level Output Current



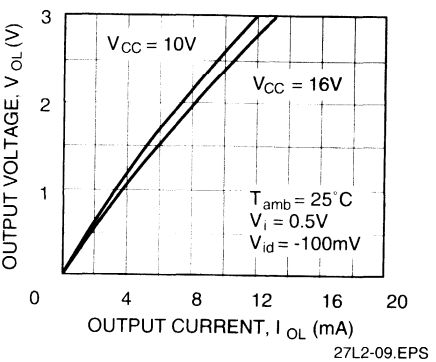
27L2-07.EPS

Figure 4a : Low Level Output Voltage versus Low Level Output Current



27L2-08.EPS

Figure 4b : Low Level Output Voltage versus Low Level Output Current



27L2-09.EPS

TYPICAL CHARACTERISTICS (continued)

Figure 5 : Open Loop Frequency Response and Phase Shift

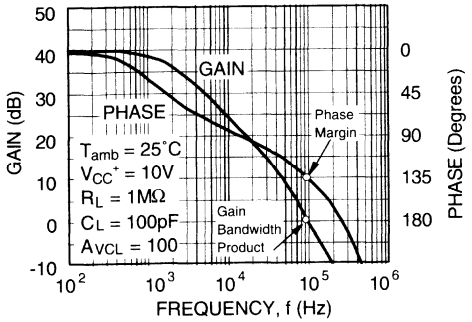


Figure 6 : Gain Bandwidth Product versus Supply Voltage

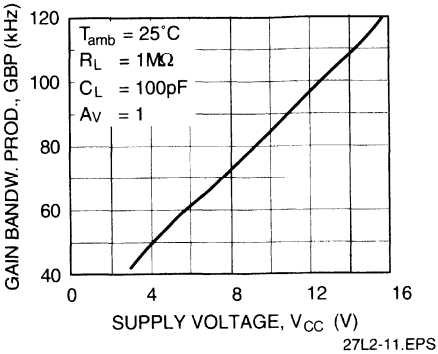


Figure 7 : Phase Margin versus Supply Voltage

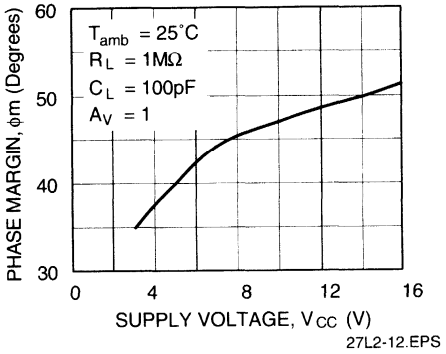


Figure 8 : Phase Margin versus Capacitive Load

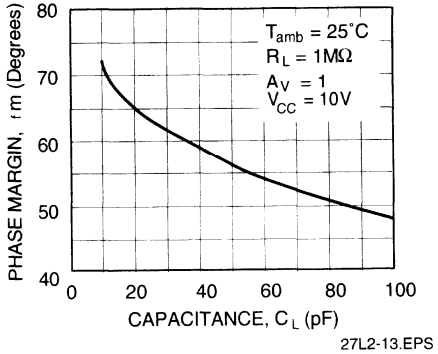


Figure 9 : Slew Rates versus Supply Voltage

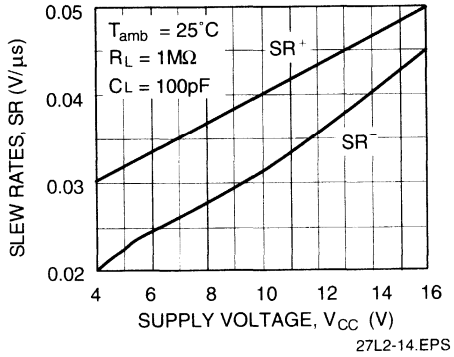
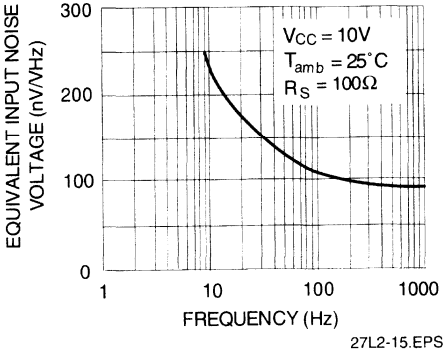


Figure 10 : Input Voltage Noise versus Frequency

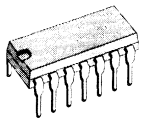


SGS-THOMSON MICROELECTRONICS

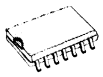
TS27L4C/I/M

VERY LOW POWER QUAD CMOS OPERATIONAL AMPLIFIERS

- EXCELLENT PHASE MARGIN ON CAPACITIVE LOADS
- SYMETRICAL OUTPUT CURRENTS
- LOW OUTPUT DYNAMIC IMPEDANCE
- THE TRANSFER FUNCTION IS LINEAR
- PIN TO PIN COMPATIBLE WITH STANDARD QUAD OP-AMPs (TL084 -LM324)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS



N
DIP14
(Plastic Package)



D
SO14
(Plastic Micropackage)

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS27L4C/AC/BC	0°C, +70°C	•	•
TS27L4I/AI/BI	-40°C, +105°C	•	•
TS27L4M/AM/BM	-55°C, +125°C	•	•
Example : TS27L4ACN			

27L4-01.TBL

DESCRIPTION

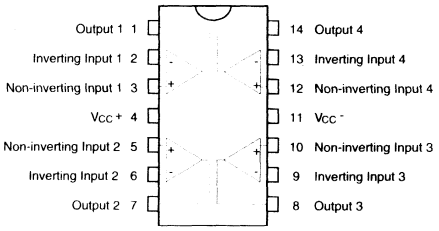
The TS274 series are low cost, low power quad operational amplifiers designed to operate with single or dual supplies. These operational amplifiers use the SGS-THOMSON silicon gate LIN MOS process giving them an excellent consumption-speed ratio. These series are ideally suited for low consumption applications.

Three power consumptions are available allowing to have always the best consumption-speed ratio :

- I_{CC}= 10µA/amp. : TS27L4 (very low power)
- I_{CC}= 150µA/amp. : TS27M4 (low power)
- I_{CC}= 1mA/amp. : TS274 (high speed)

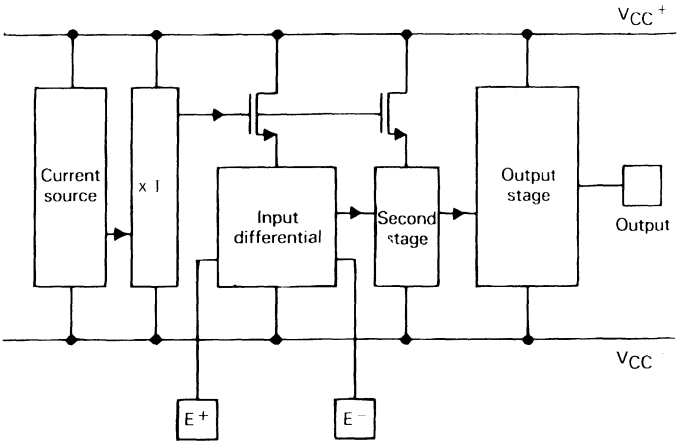
These CMOS amplifiers offer very high input impedance and extremely low input currents. The major advantage versus JFET devices is the very low input currents drift with temperature (see figure 2).

PIN CONNECTIONS (top view)



27L4-01.EPS

BLOCK DIAGRAM



27L4-02.EPS

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage - (note 1)	18	V
V_{id}	Differential Input Voltage - (note 2)	±18	V
V_i	Input Voltage - (note 3)	-0.3 to 18	V
I_O	Output Current for $V_{CC}^+ \geq 15V$	±30	mA
I_{in}	Input Current	±5	mA
T_{oper}	Operating Free-Air Temperature Range TS27L4C/AC/BC TS27L4I/AI/BI TS27L4M/AM/BM	 0 to +70 -40 to +105 -55 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

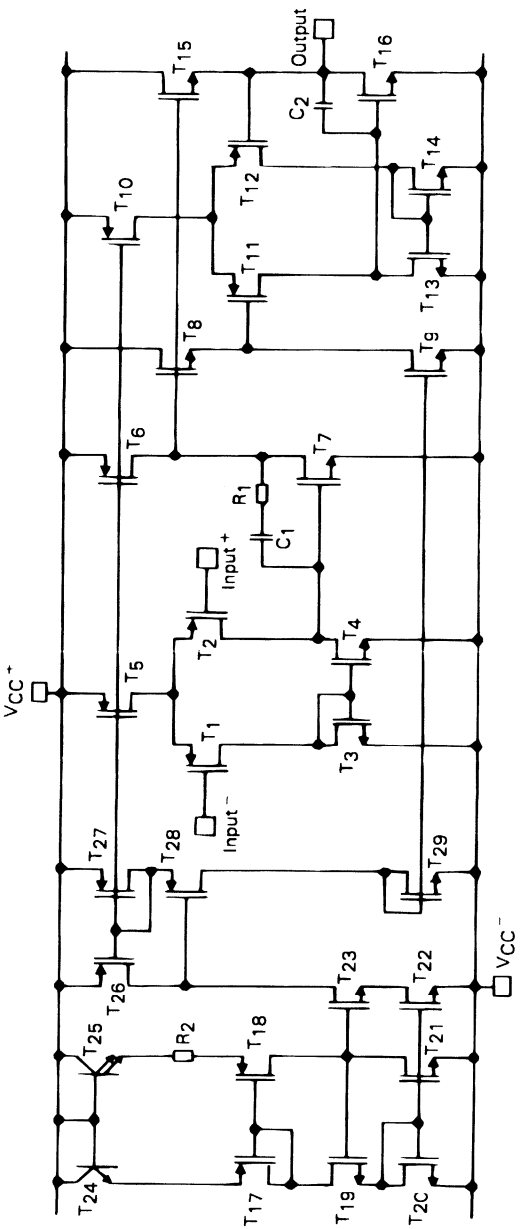
Notes : 1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input and the output voltages must never exceed the magnitude of the positive supply voltage.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage	3 * to 16	V
V_{icm}	Common Mode Input Voltage Range	0 to V_{CC}^+ - 1.5	V

* Selected devices only.

SCHEMATIC DIAGRAM (for 1/4 TS27L4)



27L4-03.EPS

ELECTRICAL CHARACTERISTICS

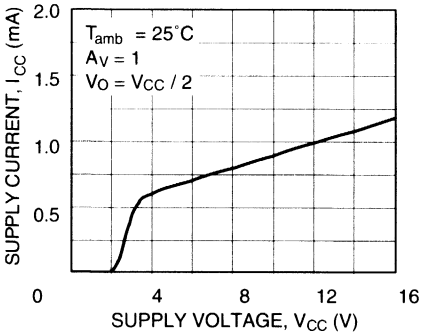
$V_{CC}^+ = +10V$, $V_{CC}^- = 0V$, $T_{amb} = 25^oC$ (unless otherwise specified)

Symbol	Parameter	TS27L4C/AC/BC			TS27L4I/AI/BI TS27L4M/AM/BM			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage $V_O = 1.4V$, $V_{ic} = 0V$ TS27L4C/I/M TS27L4AC/AI/AM TS27L4BC/BI/BM $T_{min.} \leq T_{amb} \leq T_{max.}$ TS27L4C/I/M TS27L4AC/AI/AM TS27L4BC/BI/BM		 1.1 0.9 0.25	 10 5 2 12 6.5 3		 1.1 0.9 0.25	 10 5 2 12 6.5 3.5	mV
DV_{io}	Input Offset Voltage Drift		0.7			0.7		µV/°C
I_{io}	Input Offset Current - (note 1) $V_{ic} = 5V$, $V_o = 5V$ $T_{min.} \leq T_{amb} \leq T_{max.}$		1	 100		1	 200	pA
I_{ib}	Input Bias Current - (note 1) $V_{ic} = 5V$, $V_o = 5V$ $T_{min.} \leq T_{amb} \leq T_{max.}$		1	 150		1	 300	pA
V_{OH}	High Level Output Voltage $V_{id} = 100mV$, $R_L = 1M\Omega$ $T_{min.} \leq T_{amb} \leq T_{max.}$	8.8 8.7	9		8.8 8.6	9		V
V_{OL}	Low Level Output Voltage $V_{id} = -100mV$			50			50	mV
A_{vd}	Large Signal Voltage Gain $V_o = 1V$ to $6V$, $R_L = 1M\Omega$, $V_{ic} = 5V$ $T_{min.} \leq T_{amb} \leq T_{max.}$	60 45	100		60 40	100		V/mV
GBP	Gain Bandwidth Product $A_v = 40dB$, $R_L = 1M\Omega$, $C_L = 100pF$ $f_{in} = 10kHz$		0.1			0.1		MHz
CMR	Common Mode Rejection Ratio $V_o = 1.4V$, $V_{ic} = 1V$ to $7.4V$	65	80		65	80		dB
SVR	Supply Voltage Rejection Ratio $V_{CC}^+ = 5V$ to $10V$, $V_o = 1.4V$	60	80		60	80		dB
I_{CC}	Supply Current (per amplifier) $A_v = 1$, no load, $V_o = 5V$ $T_{min.} \leq T_{amb} \leq T_{max.}$		10	15 17		10	15 18	µA
I_o	Output Short Circuit Current $V_{id} = 100mV$, $V_o = 0V$	45	60	85	45	60	85	mA
I_{sink}	Output Sink Current $V_{id} = -100mV$, $V_o = V_{CC}$	35	45	65	35	45	65	mA
SR	Slew-Rate at Unity Gain $R_L = 1M\Omega$, $C_L = 100pF$, $V_i = 3$ to $7V$		0.04			0.04		V/µs
$\varnothing m$	Phase Margin at Unity Gain $A_v = 40dB$, $R_L = 1M\Omega$, $C_L = 100pF$		45			45		Degrees
K_{ov}	Overshoot Factor		30			30		%
e_n	Equivalent Input Noise Voltage $f = 1kHz$, $R_S = 100\Omega$		68			68		$\frac{nV}{\sqrt{Hz}}$
V_{O1}/V_{O2}	Channel Separation		120			120		dB

Note : 1. Maximum values including unavoidable inaccuracies of the industrial test.

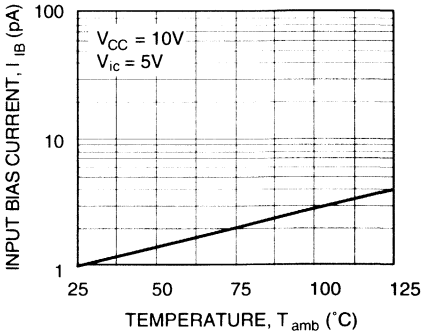
TYPICAL CHARACTERISTICS

Figure 1 : Supply Current (each amplifier) versus Supply Voltage



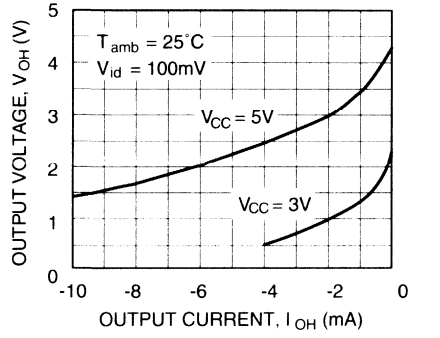
27L4-04.EPS

Figure 2 : Input Bias Current versus Free Air Temperature



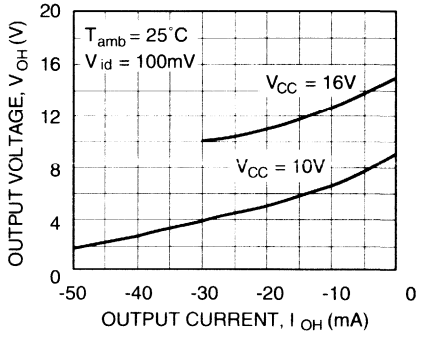
27L4-05.EPS

Figure 3a : High Level Output Voltage versus High Level Output Current



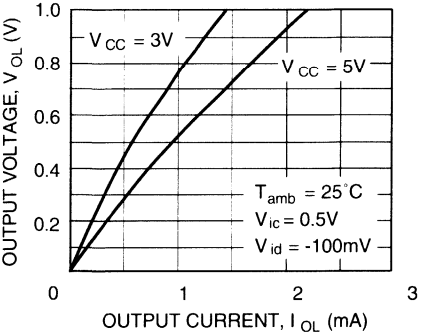
27L4-06.EPS

Figure 3b : IHigh Level Output Voltage versus High Level Output Current



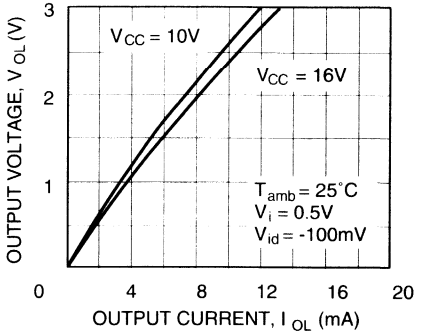
27L4-07.EPS

Figure 4a : Low Level Output Voltage versus Low Level Output Current



27L4-08.EPS

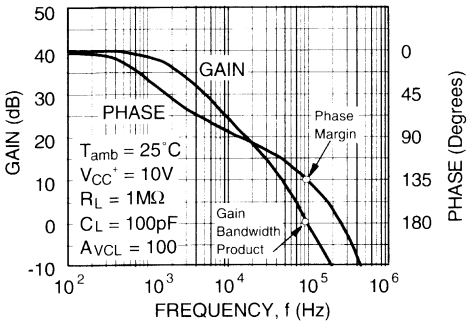
Figure 4b : Low Level Output Voltage versus Low Level Output Current



27L4-09.EPS

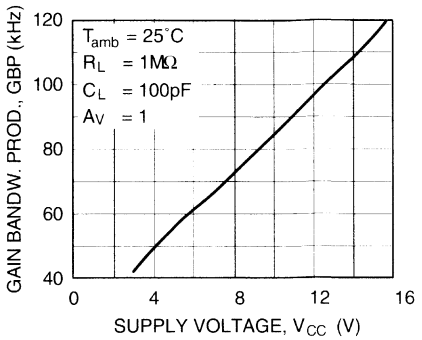
TYPICAL CHARACTERISTICS (continued)

Figure 5 : Open Loop Frequency Response and Phase Shift



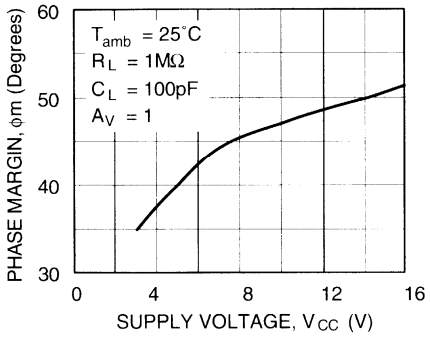
27L4-10.EPS

Figure 6 : Gain Baindwidth Product versus Supply Voltage



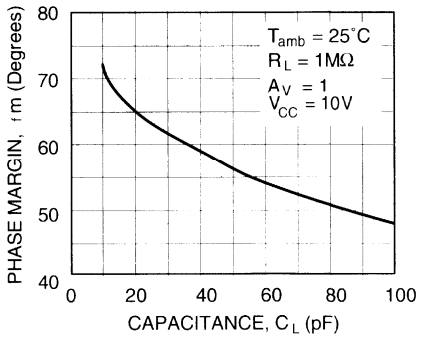
27L4-11.EPS

Figure 7 : Phase Margin versus Supply Voltage



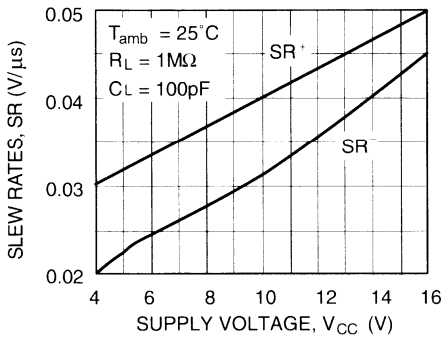
27L4-12.EPS

Figure 8 : Phase Margin versus Capacitive Load



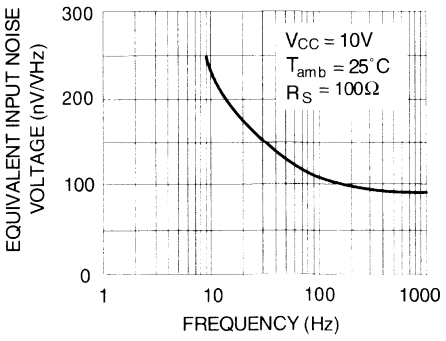
27L4-13.EPS

Figure 9 : Slew Rates versus Supply Voltage



27L4-14.EPS

Figure 10 : Input Voltage Noise versus Frequency



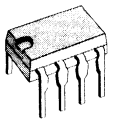
27L4-15.EPS

SGS-THOMSON MICROELECTRONICS

TS27M2C/I/M

LOW POWER DUAL CMOS OPERATIONAL AMPLIFIERS

- EXCELLENT PHASE MARGIN ON CAPACITIVE LOADS
- SYMETRICAL OUTPUT CURRENTS
- LOW OUTPUT DYNAMIC IMPEDANCE
- THE TRANSFER FUNCTION IS LINEAR
- PIN TO PIN COMPATIBLE WITH STANDARD DUAL OP-AMPs (TL082 -LM358)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS27M2C/AC/BC	0°C, +70°C	•	•
TS27M2I/AI/BI	-40°C, +105°C	•	•
TS27M2M/AM/BM	-55°C, +125°C	•	•

Example : TS27M2ACN

27M2-01.TBL

DESCRIPTION

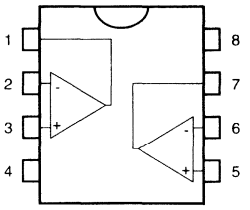
The TS272 series are low cost, low power dual operational amplifiers designed to operate with single or dual supplies: These operational amplifiers use the SGS-THOMSON silicon gate LIN MOS process giving them an excellent consumption-speed ratio. These series are ideally suited for low consumption applications.

Three power consumptions are available allowing to have always the best consumption-speed ratio :

- I_{CC}= 10µA/amp. : TS27L2 (very low power)
- I_{CC}= 150µA/amp. : TS27M2 (low power)
- I_{CC}= 1mA/amp. : TS272 (high speed)

These CMOS amplifiers offer very high input impedance and extremely low input currents. The major advantage versus JFET devices is the very low input currents drift with temperature (see figure 2).

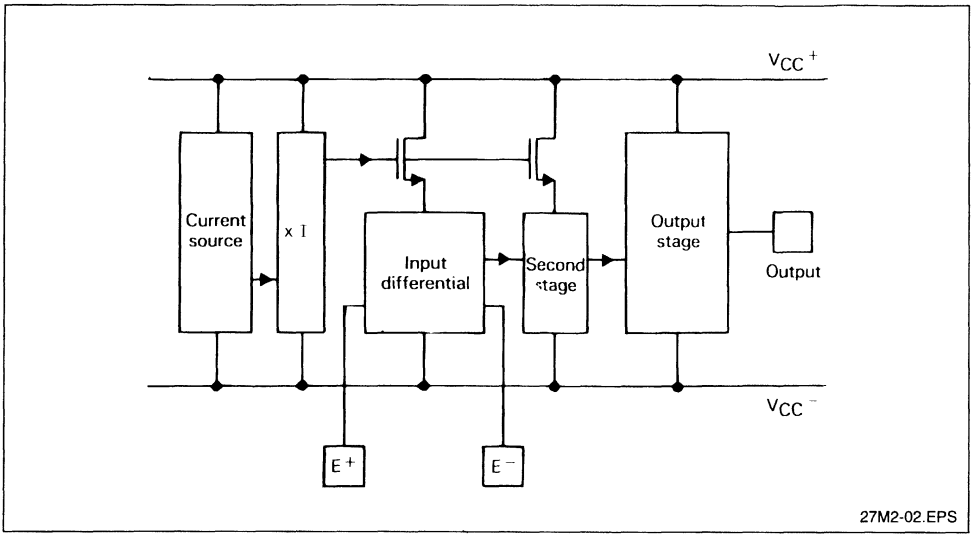
PIN CONNECTIONS (top view)



1 - Output 1
2 - Inverting Input 1
3 - Non-inverting Input 1
4 - V_{CC}^-
5 - Non-inverting Input 2
6 - Inverting Input 2
7 - Output 2
8 - V_{CC}^+

27M2-01.EPS

BLOCK DIAGRAM



MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage - (note 1)	18	V
V_{id}	Differential Input Voltage - (note 2)	±18	V
V_i	Input Voltage - (note 3)	-0.3 to 18	V
I_O	Output Current for $V_{CC}^+ \geq 15V$	±30	mA
I_{in}	Input Current	±5	mA
T_{oper}	Operating Free-Air Temperature Range TS27M2C/AC/BC TS27M2I/AI/BI TS27M2M/AM/BM	 0 to +70 -40 to +105 -55 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

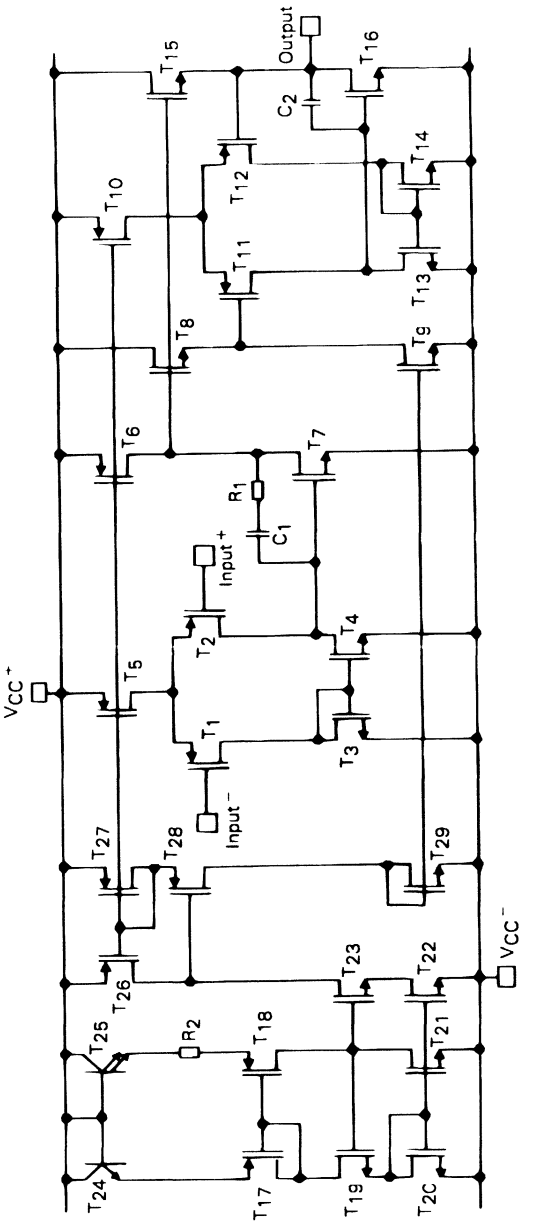
Notes : 1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input and the output voltages must never exceed the magnitude of the positive supply voltage.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage	3 * to 16	V
V_{icm}	Common Mode Input Voltage Range	0 to V_{CC}^+ - 1.5	V

* Selected devices only.

SCHEMATIC DIAGRAM (for 1/2 TS27M2)



27M2-03.EPS

ELECTRICAL CHARACTERISTICS

$V_{CC}^+ = +10V$, $V_{CC}^- = 0V$, $T_{amb} = 25^oC$ (unless otherwise specified)

Symbol	Parameter	TS27M2C/AC/BC			TS27M2I/AI/BI TS27M2M/AM/BM			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage							mV
	$V_O = 1.4V$, $V_{ic} = 0V$ TS27M2C/I/M		1.1	10		1.1	10	
	TS27M2AC/AI/AM		0.9	5		0.9	5	
	TS27M2BC/BI/BM		0.25	2		0.25	2	
	$T_{min.} \le T_{amb} \le T_{max.}$ TS27M2C/I/M			12			12	
	TS27M2AC/AI/AM			6.5			6.5	
	TS27M2BC/BI/BM			3			3.5	
DV_{io}	Input Offset Voltage Drift		2			2		µV/°C
I_{io}	Input Offset Current - (note 1)							pA
	$V_{ic} = 5V$, $V_o = 5V$		1			1		
	$T_{min.} \le T_{amb} \le T_{max.}$			100			200	
I_{ib}	Input Bias Current - (note 1)							pA
	$V_{ic} = 5V$, $V_o = 5V$		1			1		
	$T_{min.} \le T_{amb} \le T_{max.}$			150			300	
V_{OH}	High Level Output Voltage							V
	$V_{id} = 100mV$, $R_L = 100k\Omega$	8.7	8.9		8.7	8.9		
	$T_{min.} \le T_{amb} \le T_{max.}$	8.6			8.5			
V_{OL}	Low Level Output Voltage							mV
	$V_{id} = -100mV$			50			50	
A_{vd}	Large Signal Voltage Gain							V/mV
	$V_o = 1V$ to $6V$, $R_L = 100k\Omega$, $V_{ic} = 5V$	30	50		30	50		
	$T_{min.} \le T_{amb} \le T_{max.}$	20			10			
GBP	Gain Bandwidth Product							MHz
	$A_v = 40dB$, $R_L = 100k\Omega$, $C_L = 100pF$		1			1		
	$f_{in} = 100kHz$							
CMR	Common Mode Rejection Ratio							dB
	$V_o = 1.4V$, $V_{ic} = 1V$ to $7.4V$	65	80		65	80		
SVR	Supply Voltage Rejection Ratio							dB
	$V_{CC}^+ = 5V$ to $10V$, $V_o = 1.4V$	60	80		60	80		
I_{CC}	Supply Current (per amplifier)							µA
	$A_v = 1$, no load, $V_o = 5V$		150	200		150	200	
	$T_{min.} \le T_{amb} \le T_{max.}$			250			300	
I_o	Output Short Circuit Current							mA
	$V_{id} = 100mV$, $V_o = 0V$	45	60	85	45	60	85	
I_{sink}	Output Sink Current							mA
	$V_{id} = -100mV$, $V_o = V_{CC}$	35	45	65	35	45	65	
SR	Slew-Rate at Unity Gain							V/µs
	$R_L = 100k\Omega$, $C_L = 100pF$, $V_i = 3$ to $7V$		0.6			0.6		
Øm	Phase Margin at Unity Gain							Degrees
	$A_v = 40dB$, $R_L = 100k\Omega$, $C_L = 100pF$		45			45		
K_{ov}	Overshoot Factor		30			30		%
e_n	Equivalent Input Noise Voltage							$\frac{nV}{\sqrt{Hz}}$
	$f = 1kHz$, $R_S = 100\Omega$		38			38		
V_{O1}/V_{O2}	Channel Separation		120			120		dB

Note : 1. Maximum values including unavoidable inaccuracies of the industrial test.

TYPICAL CHARACTERISTICS

Figure 1 : Supply Current (each amplifier) versus Supply Voltage

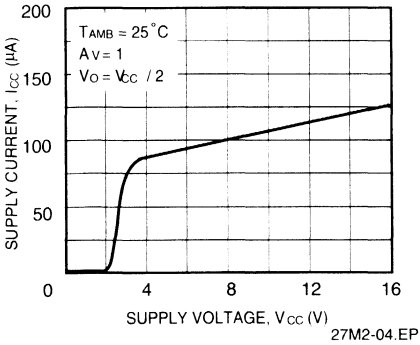


Figure 2 : Input Bias Current versus Free Air Temperature

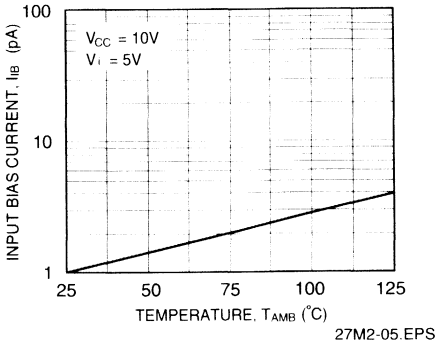


Figure 3a : High Level Output Voltage versus High Level Output Current

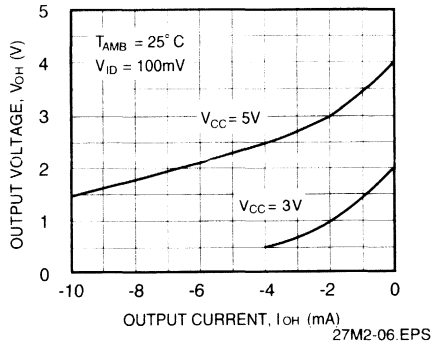


Figure 3b : High Level Output Voltage versus High Level Output Current

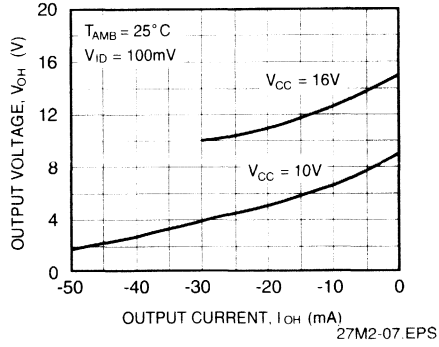


Figure 3a : Low Level Output Voltage versus Low Level Output Current

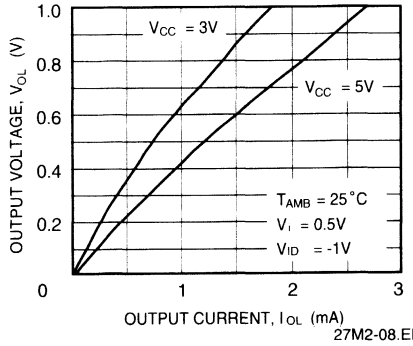
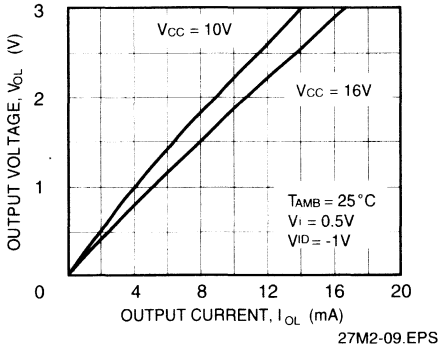


Figure 3b : Low Level Output Voltage versus Low Level Output Current



TYPICAL CHARACTERISTICS (continued)

Figure 5 : Open Loop Frequency Response and Phase Shift

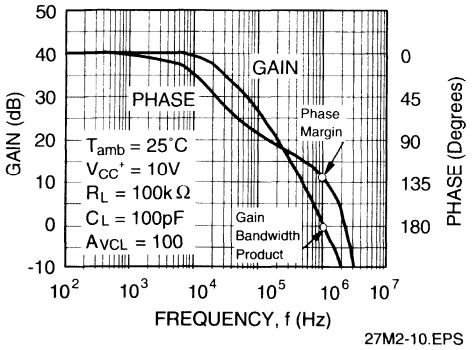


Figure 6 : Gain Bandwidth Product versus Supply Voltage

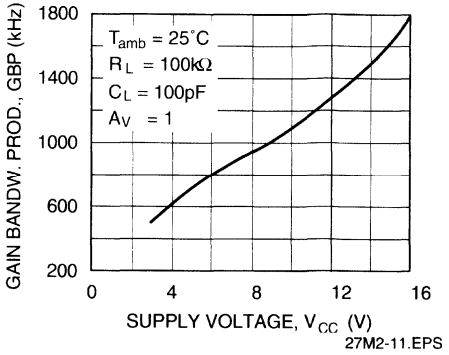


Figure 7 : Phase Margin versus Supply Voltage

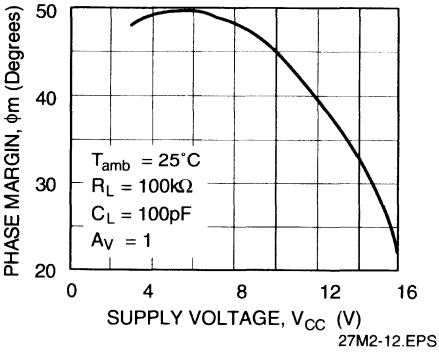


Figure 8 : Phase Margin versus Capacitive Load

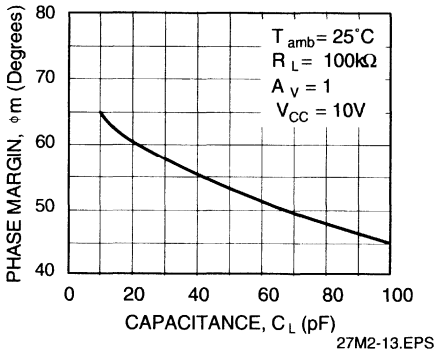


Figure 9 : Slew Rate versus Supply Voltage

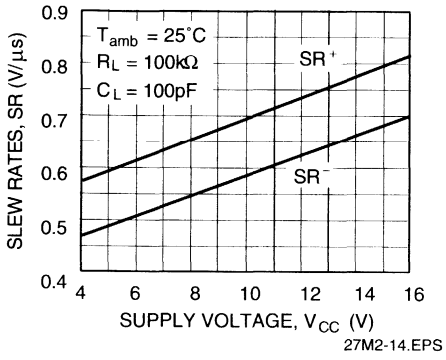
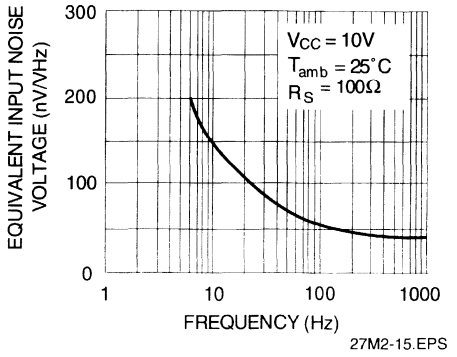


Figure 10 : Input Voltage Noise versus Frequency

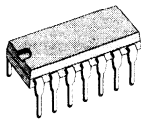


SGS-THOMSON MICROELECTRONICS

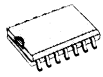
TS27M4C/I/M

LOW POWER QUAD CMOS OPERATIONAL AMPLIFIERS

- EXCELLENT PHASE MARGIN ON CAPACITIVE LOADS
- SYMETRICAL OUTPUT CURRENTS
- LOW OUTPUT DYNAMIC IMPEDANCE
- THE TRANSFER FUNCTION IS LINEAR
- PIN TO PIN COMPATIBLE WITH STANDARD QUAD OP-AMPs (TL084 -LM324)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS



N
DIP14
(Plastic Package)



D
SO14
(Plastic Micropackage)

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS27M4C/AC/BC	0°C, +70°C	•	•
TS27M4I/AI/BI	-40°C, +105°C	•	•
TS27M4M/AM/BM	-55°C, +125°C	•	•
Example : TS27M4ACN			

27M4-01.TBL

DESCRIPTION

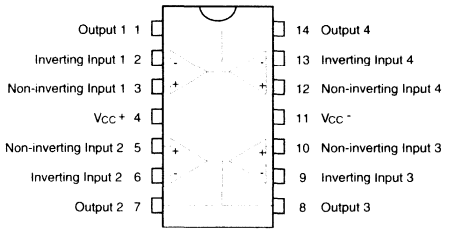
The TS274 series are low cost, low power quad operational amplifiers designed to operate with single or dual supplies. These operational amplifiers use the SGS-THOMSON silicon gate LIN MOS process giving them an excellent consumption-speed ratio. These series are ideally suited for low consumption applications.

Three power consumptions are available allowing to have always the best consumption-speed ratio :

- I_{CC}= 10µA/amp. : TS27L4 (very low power)
- I_{CC}= 150µA/amp. : TS27M4 (low power)
- I_{CC}= 1mA/amp. : TS274 (high speed)

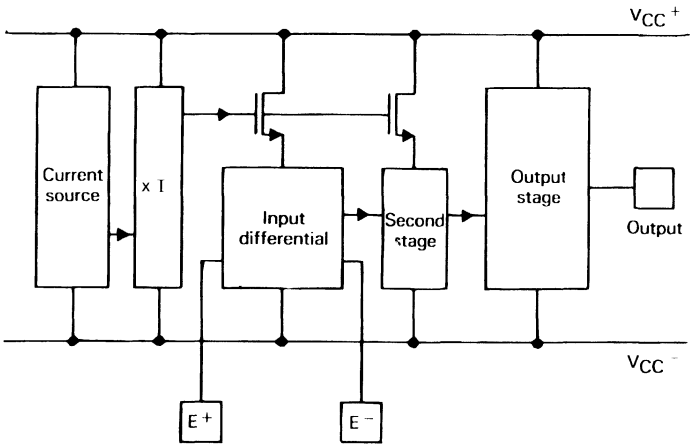
These CMOS amplifiers offer very high input impedance and extremely low input currents. The major advantage versus JFET devices is the very low input currents drift with temperature (see figure 2).

PIN CONNECTIONS (top view)



27M4-01.EPS

BLOCK DIAGRAM



27M4-02.EPS

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage - (note 1)	18	V
V_{id}	Differential Input Voltage - (note 2)	±18	V
V_i	Input Voltage - (note 3)	-0.3 to 18	V
I_O	Output Current for $V_{CC}^+ \geq 15V$	±30	mA
I_{in}	Input Current	±5	mA
T_{oper}	Operating Free-Air Temperature Range TS27M4C/AC/BC TS27M4I/AI/BI TS27M4M/AM/BM	 0 to +70 -40 to +105 -55 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

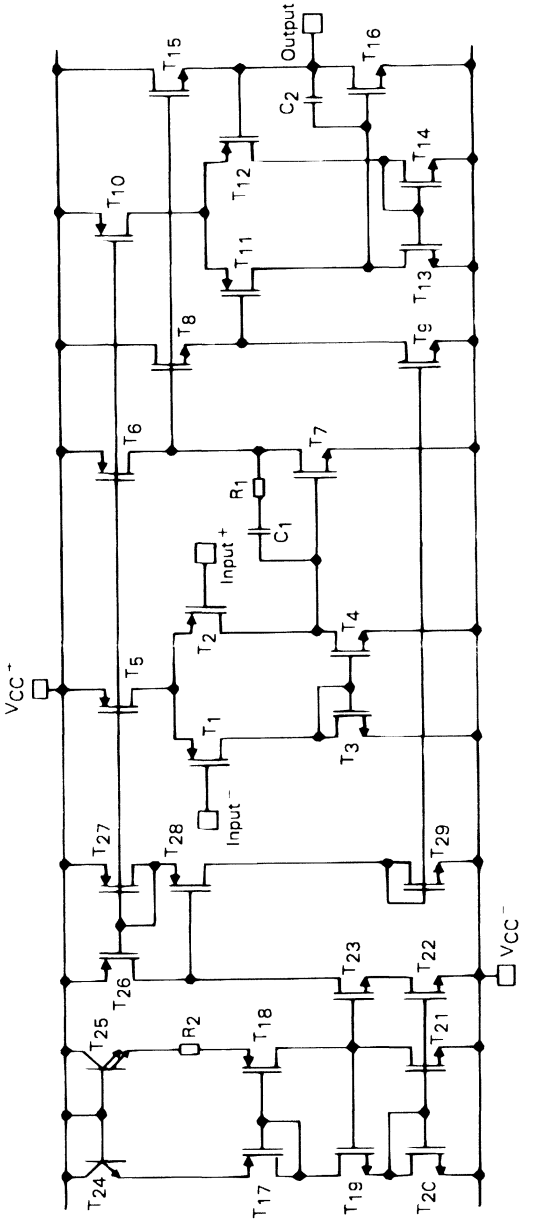
Notes :
1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input and the output voltages must never exceed the magnitude of the positive supply voltage

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage	3 * to 16	V
V_{icm}	Common Mode Input Voltage Range	0 to V_{CC}^+ - 1.5	V

* Selected devices only.

SCHEMATIC DIAGRAM (for 1/4 TS27M4)



27M4-03.EPS

ELECTRICAL CHARACTERISTICS

$V_{CC}^+ = +10V$, $V_{CC}^- = 0V$, $T_{amb} = 25°C$ (unless otherwise specified)

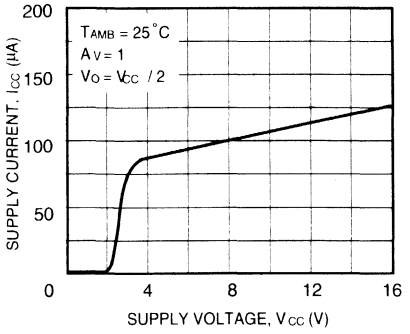
Symbol	Parameter	TS27M4C/AC/BC			TS27M4I/AI/BI TS27M4M/AM/BM			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage $V_O = 1.4V$, $V_{ic} = 0V$ TS27M4C/I/M TS27M4AC/AI/AM TS27M4BC/BI/BM $T_{min.} \le T_{amb} \le T_{max.}$ TS27M4C/I/M TS27M4AC/AI/AM TS27M4BC/BI/BM		 1.1 0.9 0.25	 10 5 2 12 6.5 3		 1.1 0.9 0.25	 10 5 2 12 6.5 3.5	mV
DV_{io}	Input Offset Voltage Drift		2			2		µV/°C
I_{io}	Input Offset Current - (note 1) $V_{ic} = 5V$, $V_o = 5V$ $T_{min.} \le T_{amb} \le T_{max.}$		1	 100		1	 200	pA
I_{ib}	Input Bias Current - (note 1) $V_{ic} = 5V$, $V_o = 5V$ $T_{min.} \le T_{amb} \le T_{max.}$		1	 150		1	 300	pA
V_{OH}	High Level Output Voltage $V_{id} = 100mV$, $R_L = 100k\Omega$ $T_{min.} \le T_{amb} \le T_{max.}$	8.7 8.6	8.9		8.7 8.5	8.9		V
V_{OL}	Low Level Output Voltage $V_{id} = -100mV$			50			50	mV
A_{vd}	Large Signal Voltage Gain $V_o = 1V$ to $6V$, $R_L = 100k\Omega$, $V_{ic} = 5V$ $T_{min.} \le T_{amb} \le T_{max.}$	30 20	50		30 10	50		V/mV
GBP	Gain Bandwidth Product $A_v = 40dB$, $R_L = 100k\Omega$, $C_L = 100pF$ $f_{in} = 100kHz$		1			1		MHz
CMR	Common Mode Rejection Ratio $V_o = 1.4V$, $V_{ic} = 1V$ to $7.4V$	65	80		65	80		dB
SVR	Supply Voltage Rejection Ratio $V_{CC}^+ = 5V$ to $10V$, $V_o = 1.4V$	60	80		60	80		dB
I_{CC}	Supply Current (per amplifier) $A_v = 1$, no load, $V_o = 5V$ $T_{min.} \le T_{amb} \le T_{max.}$		150	200 250		150	200 300	µA
I_o	Output Short Circuit Current $V_{id} = 100mV$, $V_o = 0V$	45	60	85	45	60	85	mA
I_{sink}	Output Sink Current $V_{id} = -100mV$, $V_o = V_{CC}$	35	45	65	35	45	65	mA
SR	Slew-Rate at Unity Gain $R_L = 100k\Omega$, $C_L = 100pF$, $V_i = 3$ to $7V$		0.6			0.6		V/µs
$\varnothing m$	Phase Margin at Unity Gain $A_v = 40dB$, $R_L = 100k\Omega$, $C_L = 100pF$		45			45		Degrees
K_{ov}	Overshoot Factor		30			30		%
e_n	Equivalent Input Noise Voltage $f = 1kHz$, $R_S = 100\Omega$		38			38		$\frac{nV}{\sqrt{Hz}}$
V_{O1}/V_{O2}	Channel Separation		120			120		dB

Note : 1. Maximum values including unavoidable inaccuracies of the industrial test.

27M4-04.TBL

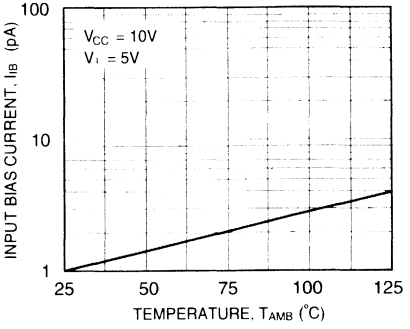
TYPICAL CHARACTERISTICS

Figure 1 : Supply Current (each amplifier) versus Supply Voltage



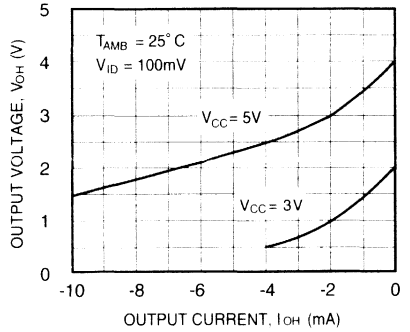
27M4-04.EPS

Figure 2 : Input Bias Current versus Free Air Temperature



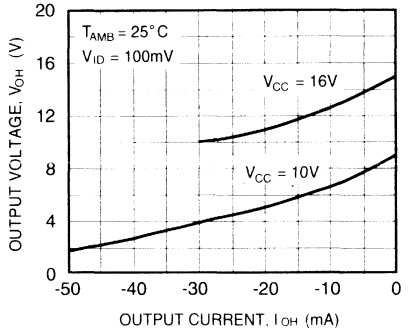
27M4-05.EPS

Figure 3a : High Level Output Voltage versus High Level Output Current



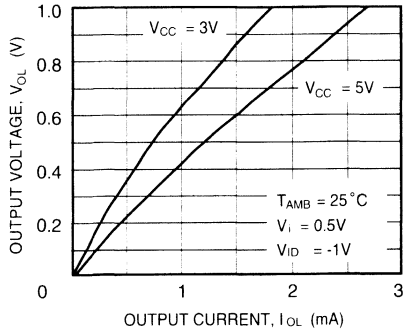
27M4-06.EPS

Figure 3b : High Level Output Voltage versus High Level Output Current



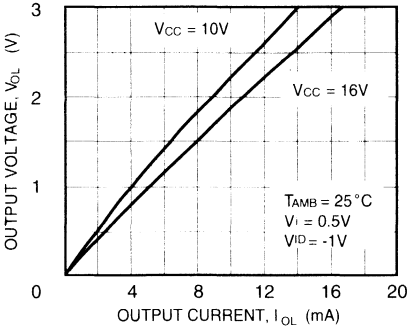
27M4-07.EPS

Figure 4a : Low Level Output Voltage versus Low Level Output Current



27M4-08.EPS

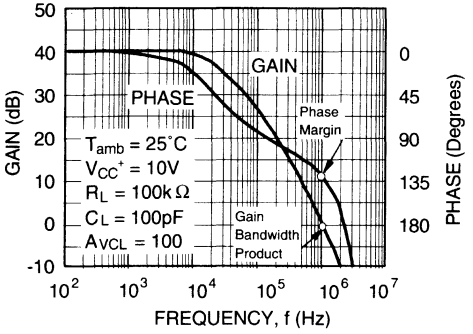
Figure 4b : Low Level Output Voltage versus Low Level Output Current



27M4-09.EPS

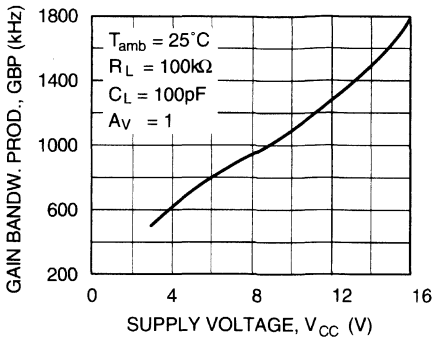
TYPICAL CHARACTERISTICS (continued)

Figure 5 : Open Loop Frequency Response and Phase Shift



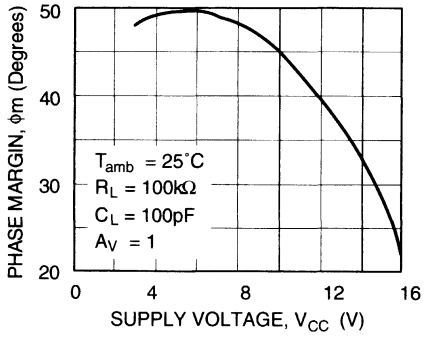
27M4-10.EPS

Figure 6 : Gain Bandwidth Product versus Supply Voltage



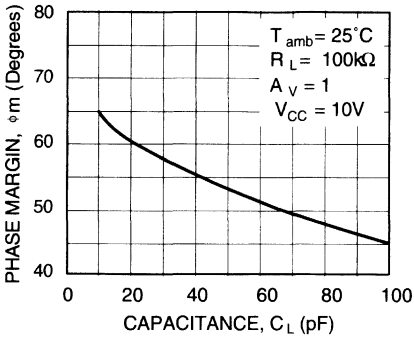
27M4-11.EPS

Figure 7 : Phase Margin versus Supply Voltage



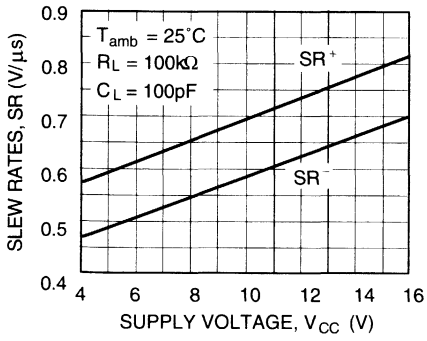
27M4-12.EPS

Figure 8 : Phase Margin versus Capacitive Load



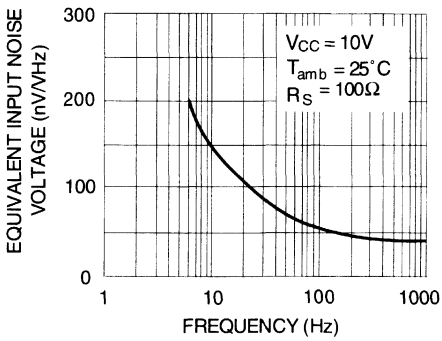
27M4-13.EPS

Figure 9 : Slew Rates versus Supply Voltage



27M4-14.EPS

Figure 10 : Input Voltage Noise versus Frequency



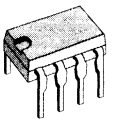
27M4-15.EPS

SGS-THOMSON MICROELECTRONICS

TS271C/I/M

PROGRAMMABLE SINGLE CMOS OPERATIONAL AMPLIFIERS

- OFFSET NULL CAPABILITY (by external compensation)
- SYMMETRICAL OUTPUT CURRENTS
- HIGH GAIN BANDWIDTH PRODUCT
- THE TRANSFER FUNCTION IS LINEAR
- CONSUMPTION CURRENT AND DYNAMIC PARAMETERS ARE STABLE REGARDING THE VOLTAGE POWER SUPPLY VARIATIONS
- DYNAMIC CHARACTERISTICS ADJUSTABLE BY I_{SET}
- VERY LARGE I_{SET} RANGE
- PIN TO PIN COMPATIBLE WITH SINGLE OPERATIONAL AMPLIFIER UA776
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS271C/AC/BC	0°C, +70°C	•	•
TS271I/AI/BI	-40°C, +105°C	•	•
TS271M/AM/BM	-55°C, +125°C	•	•

Example : TS271ACN

271-01.TBL

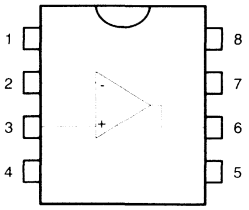
DESCRIPTION

The TS271 is a low cost, low power single operational amplifier designed to operate with single or dual supplies. This operational amplifier uses the SGS-THOMSON silicon gate LIN MOS process giving it an excellent consumption-speed ratio. This amplifier is ideally suited for low consumption applications.

The power supply is externally programmable with a resistor connected between pins 8 and 4. It allows to choose the best consumption-speed ratio and supply current can be minimized according to the required speed. This device is specified for the following I_{SET} current values : 1.5µA, 25µA, 130µA.

This CMOS amplifier offers very high input impedance and extremely low input currents. The major advantage versus JFET devices is the very low input currents drift with temperature (see figure 3).

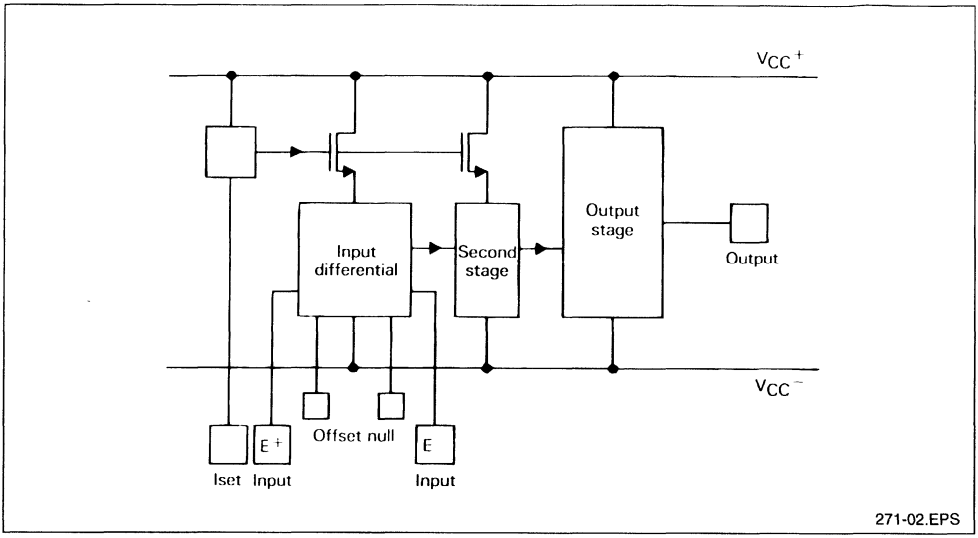
PIN CONNECTIONS (top view)



1 - Offset Null 1
2 - Inverting Input
3 - Non-inverting Input
4 - V_{CC} -
5 - Offset Null 2
6 - Output
7 - V_{CC} +
8 - I_{SET}

271-01.EPS

BLOCK DIAGRAM



MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage - (note 1)	18	V
V_{id}	Differential Input Voltage - (note 2)	±18	V
V_i	Input Voltage - (note 3)	-0.3 to 18	V
I_O	Output Current for $V_{CC}^+ \geq 15V$	±30	mA
I_{in}	Input Current	±5	mA
T_{oper}	Operating Free-Air Temperature Range TS271C/AC/BC TS271I/AI/BI TS271M/AM/BM	 0 to +70 -40 to +105 -55 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

271-02.TBL

Notes : 1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input and the output voltages must never exceed the magnitude of the positive supply voltage.

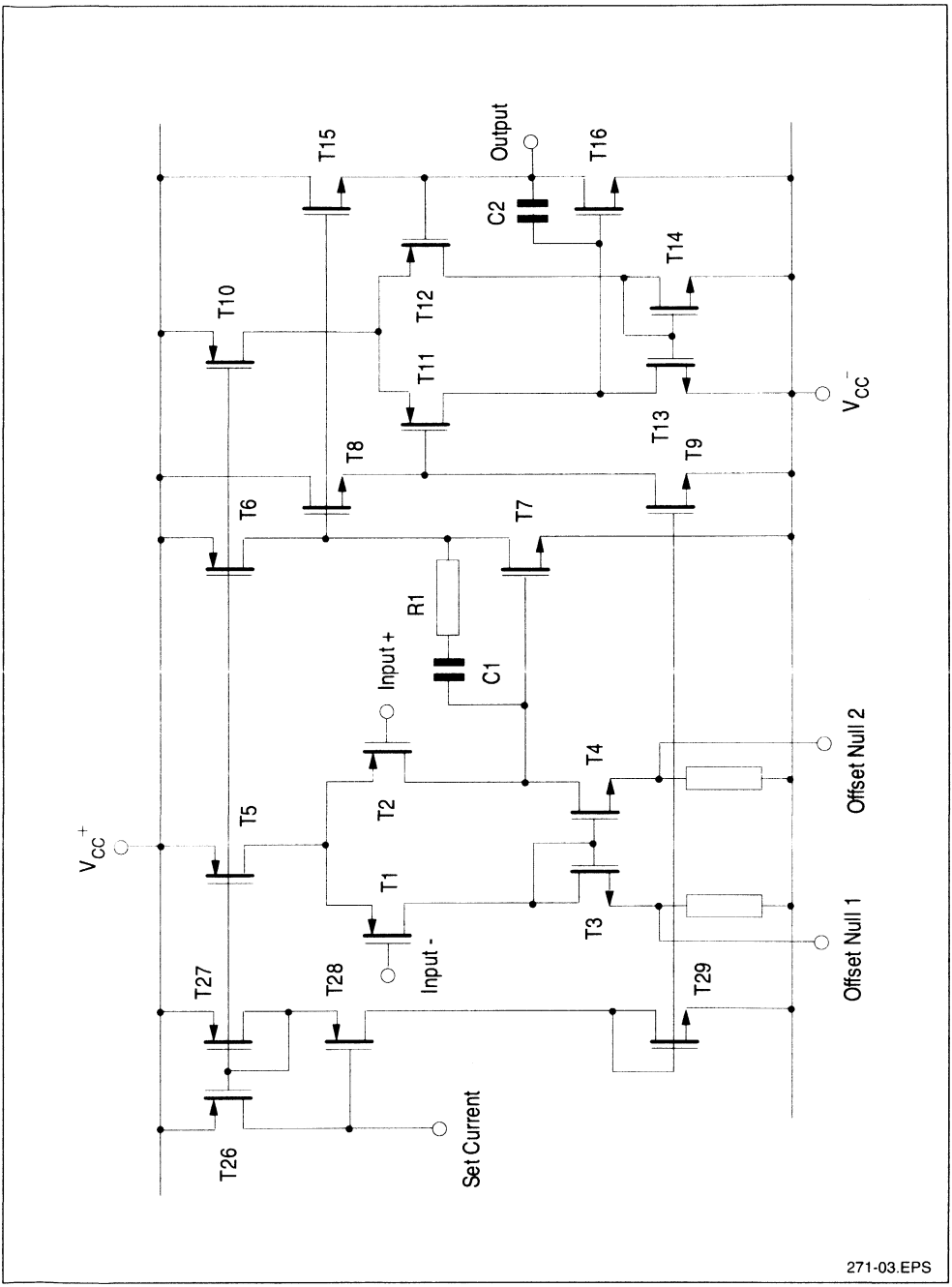
OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage	3* to 16	V
V_{icm}	Common Mode Input Voltage Range	0 to V_{CC}^+ - 1.5	V

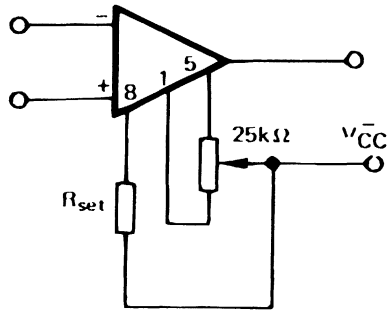
271-03.TBL

* Selected devices only.

SCHEMATIC DIAGRAM



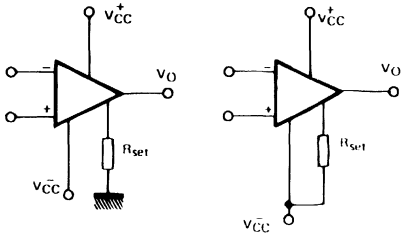
OFFSET VOLTAGE NULL CIRCUIT



OFFSET COMPENSATION GUARANTEED FOR TS271BCX (I_{SET} > 25µA),TS271ACX (I_{SET}> 90µA)

271-04.EPS

RESISTOR BIASING

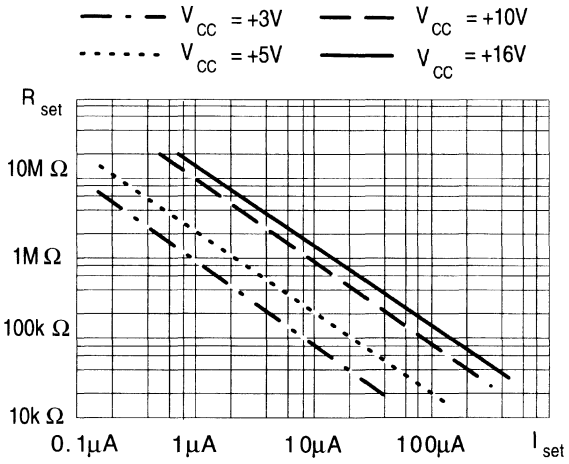


R_{SET} CONNECTED TO GROUND

R_{SET} CONNECTED TO V_{CC}^- (R_{SET} VALUE : SEE Fig.1)

271-05.EPS

Figure 1 : R_{SET} Connected to V_{CC}^-.



271-06.EPS

ELECTRICAL CHARACTERISTICS FOR I_{SET} = 1.5µA

V_{CC}^+ = +10V, V_{CC}^- = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	TS271C/AC/BC			TS271I/AI/BI TS271M/AM/BM			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage							mV
	V_O = 1.4V, V_{ic} = 0V TS271C/I/M		1.1	10		1.1	10	
	TS271AC/AI/AM		0.9	5		0.9	5	
	TS271BC/BI/BM		0.25	2		0.25	2	
	$T_{min.} \le T_{amb} \le T_{max.}$ TS271C/I/M			12			12	
	TS271AC/AI/AM			6.5			6.5	
	TS271BC/BI/BM			3			3.5	
DV_{io}	Input Offset Voltage Drift		0.7			0.7		µV/°C
I_{io}	Input Offset Current - (note 1)							pA
	V_{ic} = 5V, V_o = 5V		1			1		
	$T_{min.} \le T_{amb} \le T_{max.}$			100			200	
I_{ib}	Input Bias Current - (note 1)							pA
	V_{ic} = 5V, V_o = 5V		1			1		
	$T_{min.} \le T_{amb} \le T_{max.}$			150			300	
V_{OH}	High Level Output Voltage							V
	V_{id} = 100mV, R_L = 1MΩ	8.8	9		8.8	9		
	$T_{min.} \le T_{amb} \le T_{max.}$	8.7			8.6			
V_{OL}	Low Level Output Voltage (V_{id} = -100mV)			50			50	mV
A_{vd}	Large Signal Voltage Gain							V/mV
	V_o = 1V to 6V, R_L = 1MΩ, V_{ic} = 5V	30	100		30	100		
	$T_{min.} \le T_{amb} \le T_{max.}$	20			20			
GBP	Gain Bandwidth Product (A_v = 40dB,							MHz
	R_L = 1MΩ, C_L = 100pF, f_{in} = 10kHz)		0.1			0.1		
CMR	Common Mode Rejection Ratio							dB
	V_o = 1.4V, V_{ic} = 1V to 7.4V	60	80		60	80		
SVR	Supply Voltage Rejection Ratio							dB
	V_{CC}^+ = 5V to 10V ,V_o = 1.4V	60	80		60	80		
I_{CC}	Supply Current							µA
	A_v = 1, no load, V_o = 5V		10	15		10	15	
	$T_{min.} \le T_{amb} \le T_{max.}$			17			18	
I_o	Output Short Circuit Current							mA
	V_{id} = 100mV, V_o = 0V	45	60	85	45	60	85	
I_{sink}	Output Sink Current							mA
	V_{id} = -100mV, V_o = V_{CC}	35	45	65	35	45	65	
SR	Slew-Rate at Unity Gain							V/µs
	R_L = 1MΩ, C_L= 100pF, V_i = 3 to 7V		0.04			0.04		
∅m	Phase Margin at Unity Gain							Degrees
	A_v = 40dB, R_L = 1MΩ							
	C_L= 10pF		35			35		
	C_L= 100pF		10			10		
K_{ov}	Overshoot Factor							%
	C_L = 10pF		40			40		
	C_L = 100pF		70			70		
e_n	Equivalent Input Noise Voltage							$\frac{nV}{\sqrt{Hz}}$
	f = 1kHz, R_S = 100Ω		68			68		

271-04 TBL

Note : 1. Maximum values including unavoidable inaccuracies of the industrial test.

TYPICAL CHARACTERISTICS FOR I_{SET} = 1.5µA

Figure 2 : Supply Current versus Supply Voltage

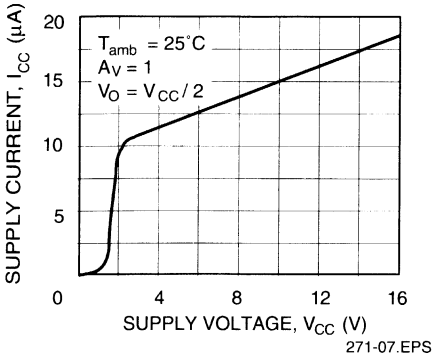


Figure 3 : Input Bias Current versus Free Air Temperature

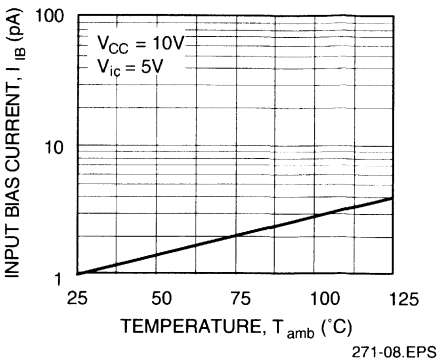


Figure 4a : High Level Output Voltage versus High Level Output Current

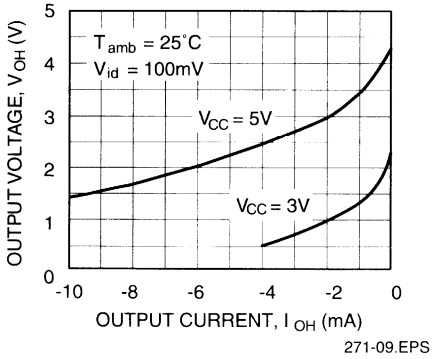


Figure 4b : High Level Output Voltage versus High Level Output Current

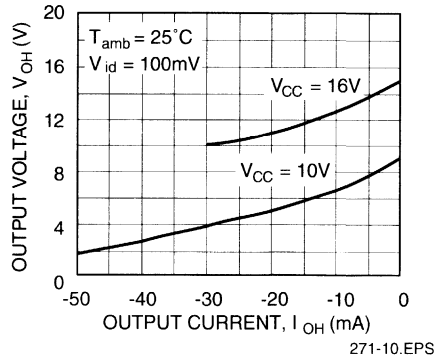


Figure 5a : Low Level Output Voltage versus Low Level Output Current

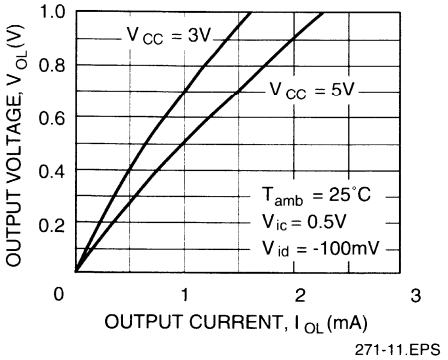
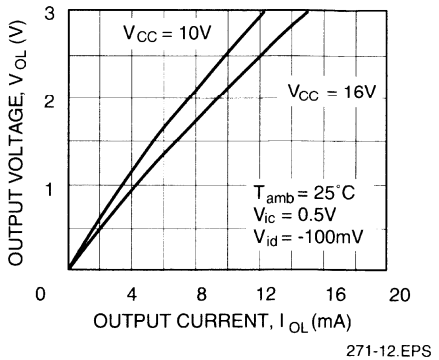


Figure 5b : Low Level Output Voltage versus Low Level Output Current



TYPICAL CHARACTERISTICS FOR I_{SET} = 1.5µA (continued)

Figure 6 : Open Loop Frequency Response and Phase Shift

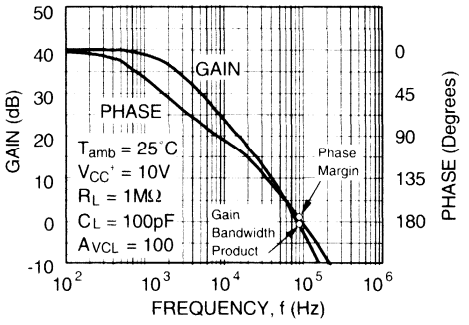


Figure 7 : Gain Bandwidth Product versus Supply voltage

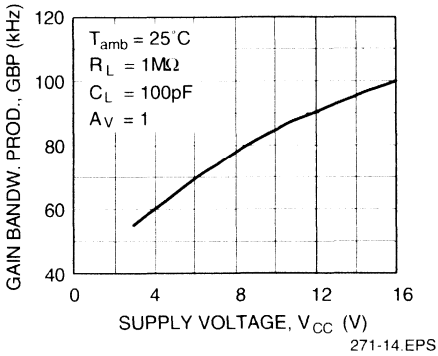


Figure 8 : Phase Margin versus Supply Voltage

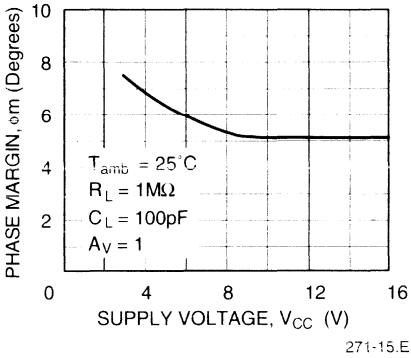


Figure 9 : Phase Margin versus Capacitive Load

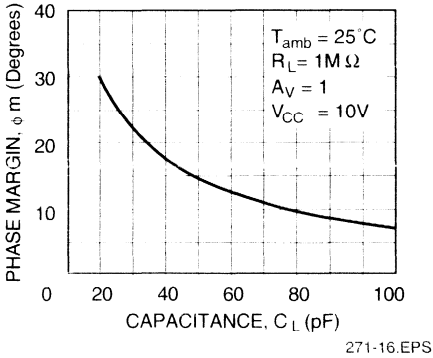
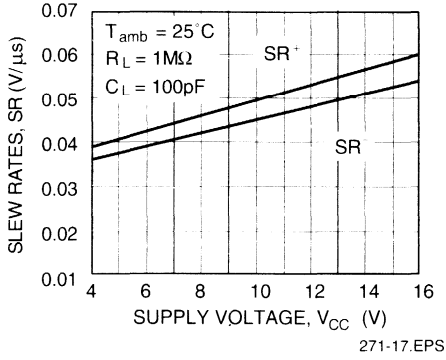


Figure 10 : Slew Rates versus Supply Voltage



ELECTRICAL CHARACTERISTICS FOR I_{SET} = 25µA

V_{CC}^+ = +10V, V_{CC}^- = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	TS271C/AC/BC			TS271I/AI/BI TS271M/AM/BM			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_O = 1.4V, V_{ic} = 0V TS271C/I/M TS271AC/AI/AM TS271BC/BI/BM $T_{min.} \le T_{amb} \le T_{max.}$ TS271C/I/M TS271AC/AI/AM TS271BC/BI/BM		1.1 0.9 0.25	10 5 2 12 6.5 3		1.1 0.9 0.25	10 5 2 12 6.5 3.5	mV
DV_{io}	Input Offset Voltage Drift		2			2		µV/°C
I_{io}	Input Offset Current - (note 1) V_{ic} = 5V, V_o = 5V $T_{min.} \le T_{amb} \le T_{max.}$		1	 100		1	 200	pA
I_{ib}	Input Bias Current - (note 1) V_{ic} = 5V, V_o = 5V $T_{min.} \le T_{amb} \le T_{max.}$		1	 150		1	 300	pA
V_{OH}	High Level Output Voltage V_{id} = 100mV, R_L = 100kΩ $T_{min.} \le T_{amb} \le T_{max.}$	8.7 8.6	8.9		8.7 8.5	8.9		V
V_{OL}	Low Level Output Voltage (V_{id} = -100mV)			50			50	mV
A_{vd}	Large Signal Voltage Gain V_o = 1V to 6V, R_L = 100kΩ, V_{ic} = 5V $T_{min.} \le T_{amb} \le T_{max.}$	30 20	50		30 10	50		V/mV
GBP	Gain Bandwidth Product (A_v = 40dB, R_L = 100kΩ, C_L = 100pF, f_{in} = 100kHz)		0.7			0.7		MHz
CMR	Common Mode Rejection Ratio V_o = 1.4V, V_{ic} = 1V to 7.4V	60	80		60	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC}^+ = 5V to 10V ,V_o = 1.4V	60	80		60	80		dB
I_{CC}	Supply Current A_v = 1, no load, V_o = 5V $T_{min.} \le T_{amb} \le T_{max.}$		150	200 250		150	200 300	µA
I_o	Output Short Circuit Current V_{id} = 100mV, V_o = 0V	45	60	85	45	60	85	mA
I_{sink}	Output Sink Current V_{id} = -100mV, V_o = V_{CC}	35	45	65	35	45	65	mA
SR	Slew-Rate at Unity Gain R_L = 100kΩ, C_L= 100pF, V_i = 3 to 7V		0.6			0.6		V/µs
Øm	Phase Margin at Unity Gain A_v = 40dB, R_L = 100kΩ C_L = 10pF C_L= 100pF		 50 30			 50 30		degrees
K_{ov}	Overshoot Factor C_L = 10pF C_L = 100pF		30 50			30 50		%
e_n	Equivalent Input Noise Voltage f = 1kHz, R_S = 100Ω		38			38		$\frac{nV}{\sqrt{Hz}}$

271-05.TBL

Note : 1. Maximum values including unavoidable inaccuracies of the industrial test.

TYPICAL CHARACTERISTICS FOR I_{SET} = 25µA

Figure 11 : Supply Current versus Supply Voltage

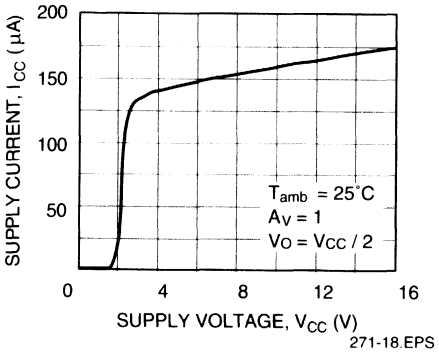


Figure 12 : Input Bias Current versus Free Air Temperature

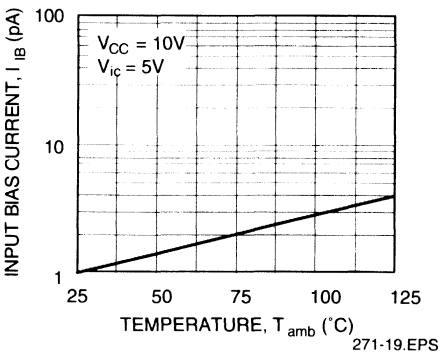


Figure 13a : High Level Output Voltage versus High Level Output Current

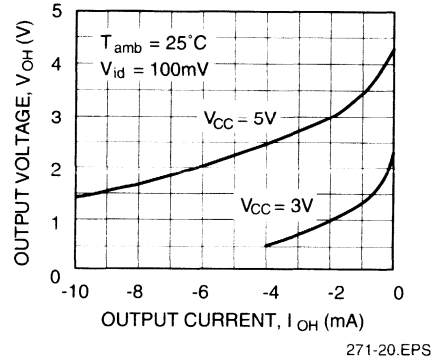


Figure 13b : High Level Output Voltage versus High Level Output Current

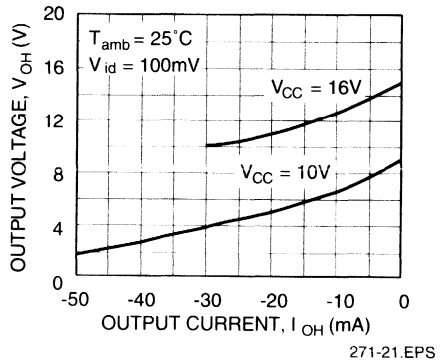


Figure 14a : Low Level Output Voltage versus Low Level Output Current

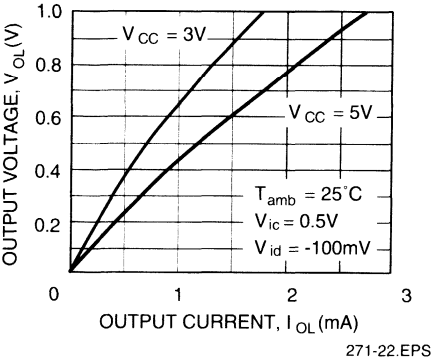
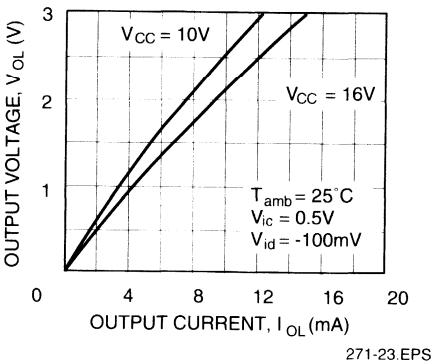
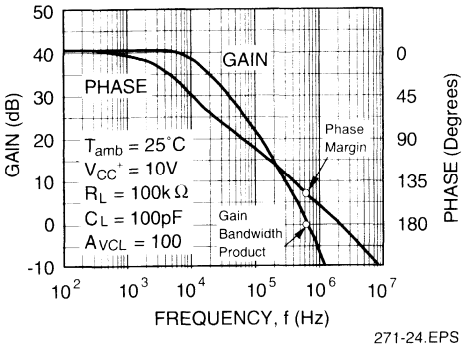


Figure 14b : Low Level Output Voltage versus Low Level Output Current



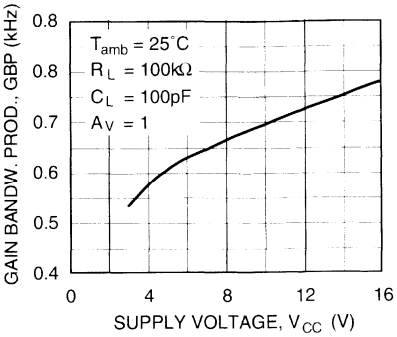
TYPICAL CHARACTERISTICS FOR I_{SET} = 25µA (continued)

Figure 15 : Open Loop Frequency Response and Phase Shift



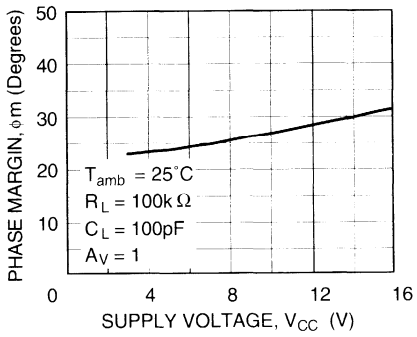
271-24.EPS

Figure 16 : Gain Bandwidth Product versus Supply voltage



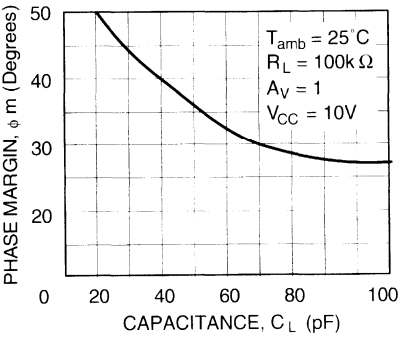
271-25.EPS

Figure 17 : Phase Margin versus Supply Voltage



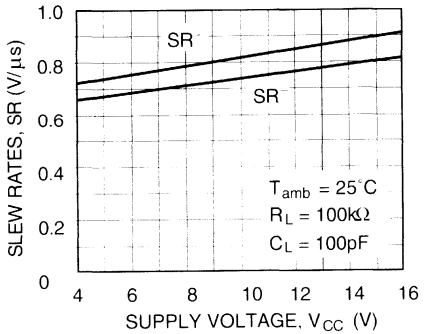
271-26.EPS

Figure 18 : Phase Margin versus Capacitive Load



271-27.EPS

Figure 19 : Slew Rates versus Supply Voltage



271-28.EPS

ELECTRICAL CHARACTERISTICS FOR I_{SET} = 130µA

V_{CC}^+ = +10V, V_{CC}^- = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	TS271C/AC/BC			TS271I/AI/BI TS271M/AM/BM			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage							mV
	V_O = 1.4V, V_{ic} = 0V TS271C/I/M		1.1	10		1.1	10	
	TS271AC/AI/AM		0.9	5		0.9	5	
	TS271BC/BI/BM		0.25	2		0.25	2	
	$T_{min.} \le T_{amb} \le T_{max.}$ TS271C/I/M			12			12	
	TS271AC/AI/AM			6.5			6.5	
	TS271BC/BI/BM			3			3.5	
DV_{io}	Input Offset Voltage Drift		2			2		µV/°C
I_{io}	Input Offset Current - (note 1)							pA
	V_{ic} = 5V, V_o = 5V		1			1		
	$T_{min.} \le T_{amb} \le T_{max.}$			100			200	
I_{ib}	Input Bias Current - (note 1)							pA
	V_{ic} = 5V, V_o = 5V		1			1		
	$T_{min.} \le T_{amb} \le T_{max.}$			150			300	
V_{OH}	High Level Output Voltage							V
	V_{id} = 100mV, R_L = 10kΩ	8.2	8.4		8.2	8.4		
	$T_{min.} \le T_{amb} \le T_{max.}$	8.1			8			
V_{OL}	Low Level Output Voltage (V_{id} = -100mV)			50			50	mV
A_{vd}	Large Signal Voltage Gain							V/mV
	V_o = 1V to 6V, R_L = 10kΩ, V_{ic} = 5V	10	15		10	15		
	$T_{min.} \le T_{amb} \le T_{max.}$	7			6			
GBP	Gain Bandwidth Product (A_v = 40dB,							MHz
	R_L = 10kΩ, C_L = 100pF, f_{in} = 200kHz)		2.3			2.3		
CMR	Common Mode Rejection Ratio							dB
	V_o = 1.4V, V_{ic} = 1V to 7.4V	60	80		60	80		
SVR	Supply Voltage Rejection Ratio							dB
	V_{CC}^+ = 5V to 10V ,V_o = 1.4V	60	70		60	70		
I_{CC}	Supply Current							µA
	A_v = 1, no load, V_o = 5V		800	1300		800	1300	
	$T_{min.} \le T_{amb} \le T_{max.}$			1400			1500	
I_o	Output Short Circuit Current							mA
	V_{id} = 100mV, V_o = 0V	45	60	85	45	60	85	
I_{sink}	Output Sink Current							mA
	V_{id} = -100mV, V_o = V_{CC}	35	45	65	35	45	65	
SR	Slew-Rate at Unity Gain							V/µs
	R_L = 10kΩ, C_L= 100pF, V_i = 3 to 7V		4.5			4.5		
Øm	Phase Margin at Unity Gain							degrees
	A_v = 40dB, R_L = 10kΩ							
	C_L= 10pF		65			65		
	C_L= 100pF		50			50		
K_{ov}	Overshoot Factor							%
	C_L = 10pF		30			30		
	C_L = 100pF		30			30		
e_n	Equivalent Input Noise Voltage							$\frac{nV}{\sqrt{Hz}}$
	f = 1kHz, R_S = 100Ω		30			30		

Note : 1. Maximum values including unavoidable inaccuracies of the industrial test.

271-06.TBL

TYPICAL CHARACTERISTICS FOR I_{SET} = 130µA

Figure 20 : Supply Current (each amplifier) versus Supply Voltage

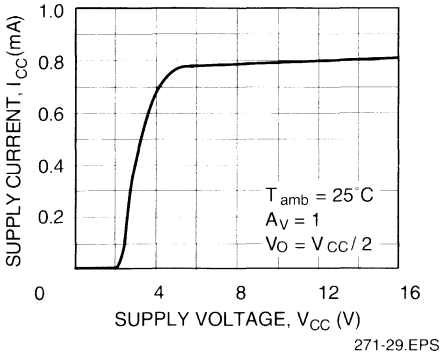


Figure 21 : Input Bias Current versus Free Air Temperature

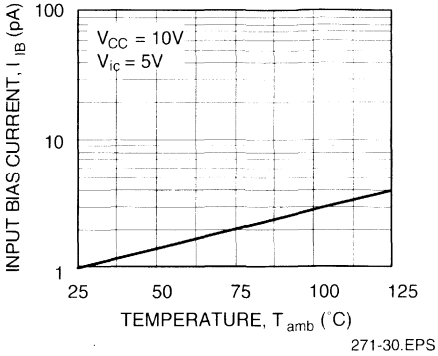


Figure 22a : High Level Output Voltage versus High Level Output Current

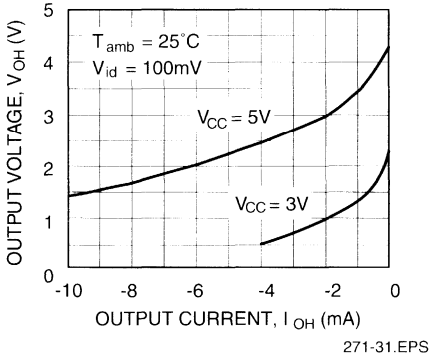


Figure 22b : High Level Output Voltage versus High Level Output Current

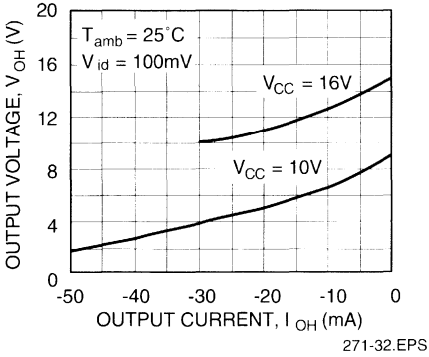


Figure 23a : Low Level Output Voltage versus Low Level Output Current

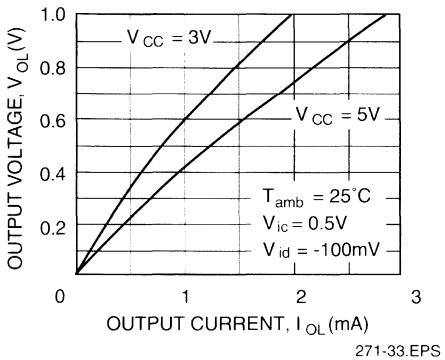
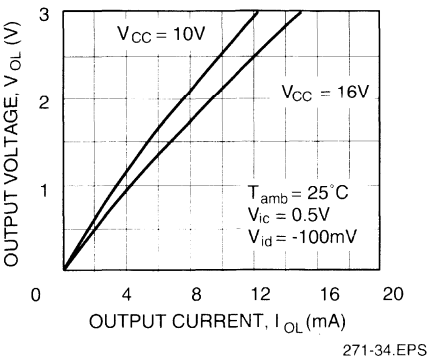


Figure 23b : Low Level Output Voltage versus Low Level Output Current



TYPICAL CHARACTERISTICS FOR I_{SET} = 130µA (continued)

Figure 24 : Open Loop Frequency Response and Phase Shift

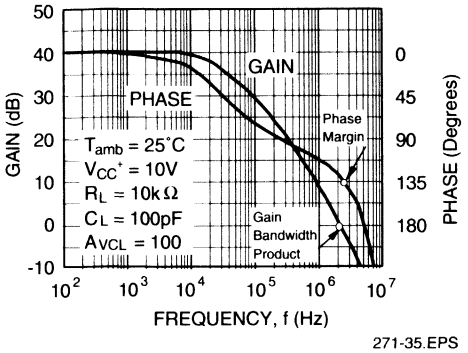


Figure 25 : Gain Bandwidth Product versus Supply voltage

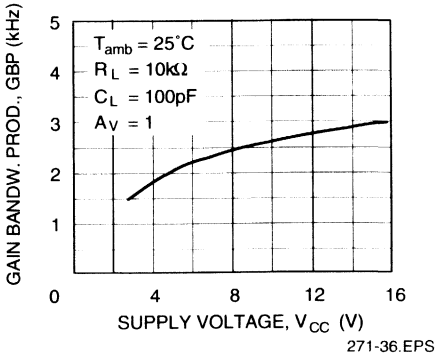


Figure 26 : Phase Margin versus Supply Voltage

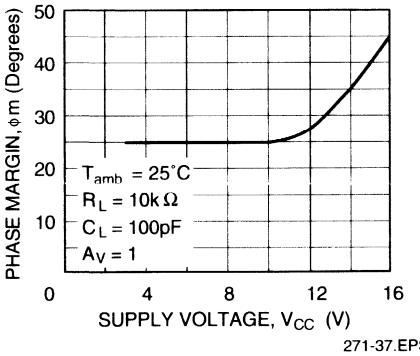


Figure 27 : Phase Margin versus Capacitive Load

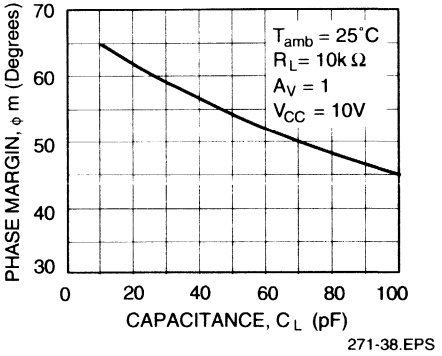
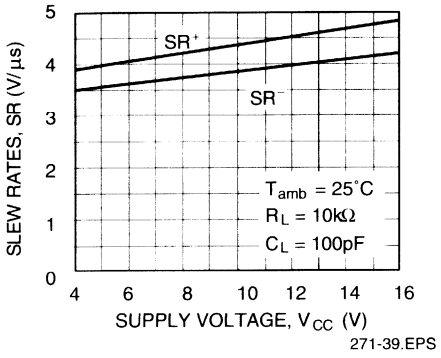


Figure 28 : Slew Rates versus Supply Voltage

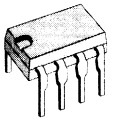


SGS-THOMSON MICROELECTRONICS

TS272C/I/M

HIGH SPEED DUAL CMOS OPERATIONAL AMPLIFIERS

- EXCELLENT PHASE MARGIN ON CAPACITIVE LOADS
- SYMETRICAL OUTPUT CURRENTS
- HIGH GAIN BANDWIDTH PRODUCT
- LOW OUTPUT DYNAMIC IMPEDANCE
- THE TRANSFER FUNCTION IS LINEAR
- PIN TO PIN COMPATIBLE WITH STANDARD DUAL OP-AMPs (TL082 -LM358)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS272C/AC/BC	0°C, +70°C	•	•
TS272I/AI/BI	-40°C, +105°C	•	•
TS272M/AM/BM	-55°C, +125°C	•	•
Example : TS272ACN			

272-01.TBL

DESCRIPTION

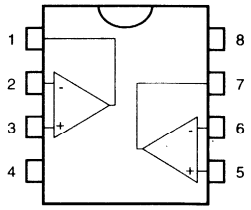
The TS272 series are low cost, low power dual operational amplifiers designed to operate with single or dual supplies. These operational amplifiers use the SGS-THOMSON silicon gate LIN MOS process giving them an excellent consumption-speed ratio. These series are ideally suited for low consumption applications.

Three power consumptions are available allowing to have always the best consumption-speed ratio :

- I_{CC}= 10µA/amp. : TS27L2 (very low power)
- I_{CC}= 150µA/amp. : TS27M2 (low power)
- I_{CC}= 1mA/amp. : TS272 (high speed)

These CMOS amplifiers offer very high input impedance and extremely low input currents. The major advantage versus JFET devices is the very low input currents drift with temperature (see figure 2).

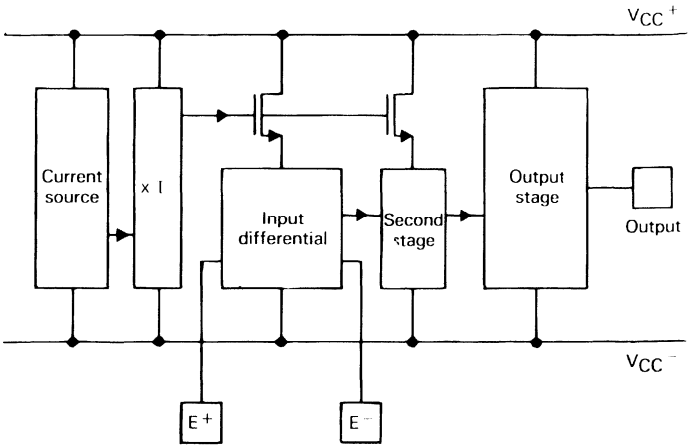
PIN CONNECTIONS (top view)



1 - Output 1
2 - Inverting Input 1
3 - Non-inverting Input 1
4 - V_{CC}^-
5 - Non-inverting Input 2
6 - Inverting Input 2
7 - Output 2
8 - V_{CC}^+

272-01.EPS

BLOCK DIAGRAM



272-02.EPS

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}^+	Supply Voltage - (note 1)		18	V
V_{id}	Differential Input Voltage - (note 2)		±18	V
V_i	Input Voltage - (note 3)		-0.3 to 18	V
I_O	Output Current for $V_{CC}^+ \geq 15V$		±30	mA
I_{in}	Input Current		±5	mA
T_{oper}	Operating Free-Air Temperature Range	TS272C/AC/BC TS272I/AI/BI TS272M/AM/BM	 0 to +70 -40 to +105 -55 to +125	°C
T_{stg}	Storage Temperature Range		-65 to +150	°C

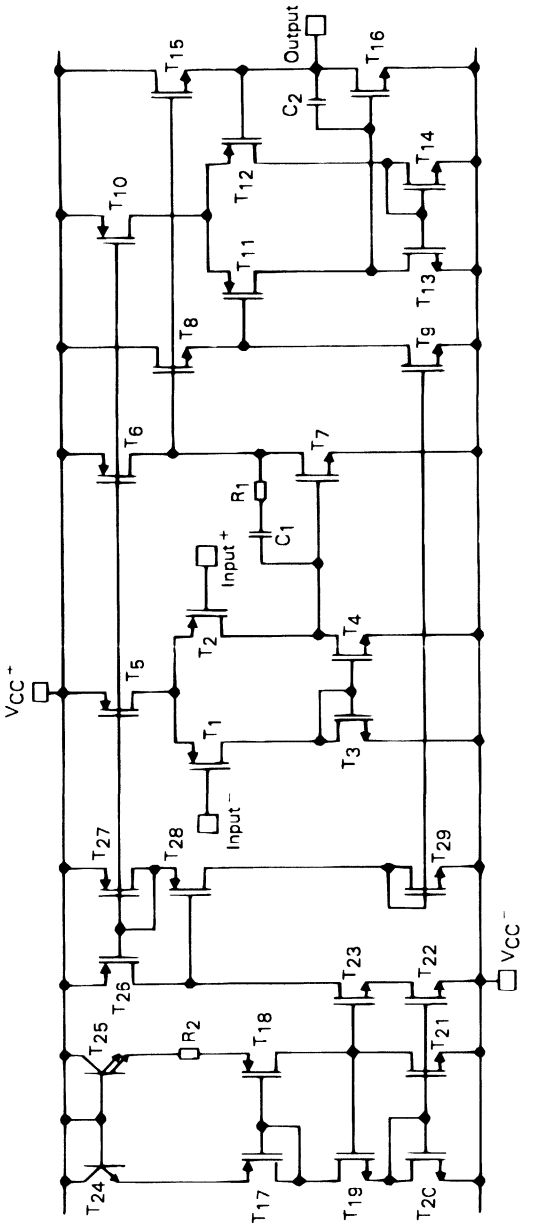
Notes : 1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input and the output voltages must never exceed the magnitude of the positive supply voltage.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage	3 * to 16	V
V_{icm}	Common Mode Input Voltage Range	0 to V_{CC}^+ - 1.5	V

* Selected devices only.

SCHEMATIC DIAGRAM (for 1/2 TS272)



272-03.EPS

ELECTRICAL CHARACTERISTICS

$V_{CC}^+ = +10V$, $V_{CC}^- = 0V$, $T_{amb} = 25^oC$ (unless otherwise specified)

Symbol	Parameter	TS272C/AC/BC			TS272I/AI/BI TS272M/AM/BM			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage							mV
	$V_O = 1.4V$, $V_{ic} = 0V$ TS272C/I/M		1.1	10		1.1	10	
	TS272AC/AI/AM		0.9	5		0.9	5	
	TS272BC/BI/BM		0.25	2		0.25	2	
	$T_{min.} \le T_{amb} \le T_{max.}$ TS272C/I/M			12			12	
	TS272AC/AI/AM			6.5			6.5	
	TS272BC/BI/BM			3			3.5	
DV_{io}	Input Offset Voltage Drift		2			2		µV/°C
I_{io}	Input Offset Current - (note 1)							pA
	$V_{ic} = 5V$, $V_o = 5V$		1			1		
	$T_{min.} \le T_{amb} \le T_{max.}$			100			200	
I_{ib}	Input Bias Current - (note 1)							pA
	$V_{ic} = 5V$, $V_o = 5V$		1			1		
	$T_{min.} \le T_{amb} \le T_{max.}$			150			300	
V_{OH}	High Level Output Voltage							V
	$V_{id} = 100mV$, $R_L = 10k\Omega$	8.2	8.4		8.2	8.4		
	$T_{min.} \le T_{amb} \le T_{max.}$	8.1			8			
V_{OL}	Low Level Output Voltage							mV
	$V_{id} = -100mV$			50			50	
A_{vd}	Large Signal Voltage Gain							V/mV
	$V_o = 1V$ to $6V$, $R_L = 10k\Omega$, $V_{ic} = 5V$	10	15		10	15		
	$T_{min.} \le T_{amb} \le T_{max.}$	7			6			
GBP	Gain Bandwidth Product							MHz
	$A_v = 40dB$, $R_L = 10k\Omega$, $C_L = 100pF$		3.5			3.5		
	$f_{in} = 200kHz$							
CMR	Common Mode Rejection Ratio							dB
	$V_o = 1.4V$, $V_{ic} = 1V$ to $7.4V$	65	80		65	80		
SVR	Supply Voltage Rejection Ratio							dB
	$V_{CC}^+ = 5V$ to $10V$,$V_o = 1.4V$	60	70		60	70		
I_{CC}	Supply Current (per amplifier)							µA
	$A_v = 1$, no load, $V_o = 5V$		1000	1500		1000	1500	
	$T_{min.} \le T_{amb} \le T_{max.}$			1600			1700	
I_o	Output Short Circuit Current							mA
	$V_{id} = 100mV$, $V_o = 0V$	45	60	85	45	60	85	
I_{sink}	Output Sink Current							mA
	$V_{id} = -100mV$, $V_o = V_{CC}$	35	45	65	35	45	65	
SR	Slew-Rate at Unity Gain							V/µs
	$R_L = 10k\Omega$, $C_L = 100pF$, $V_i = 3$ to $7V$		5.5			5.5		
Øm	Phase Margin at Unity Gain							Degrees
	$A_v = 40dB$, $R_L = 10k\Omega$, $C_L = 100pF$		40			40		
K_{ov}	Overshoot Factor		30			30		%
e_n	Equivalent Input Noise Voltage							$\frac{nV}{\sqrt{Hz}}$
	$f = 1kHz$, $R_S = 100\Omega$		30			30		
V_{O1}/V_{O2}	Channel Separation		120			120		dB

Note : 1. Maximum values including unavoidable inaccuracies of the industrial test.

272-04.TBL

TYPICAL CHARACTERISTICS

Figure 1 : Supply Current (each amplifier) versus Supply Voltage

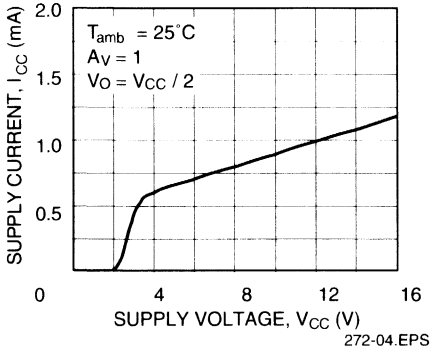


Figure 2 : Input Bias Current versus Free Air Temperature

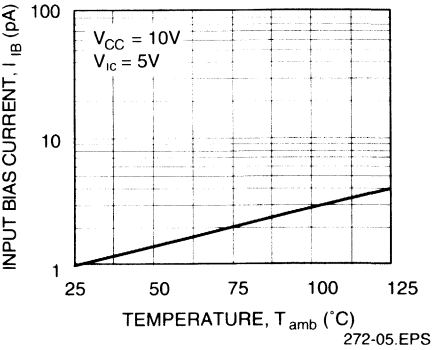


Figure 3a : High Level Output Voltage versus High Level Output Current

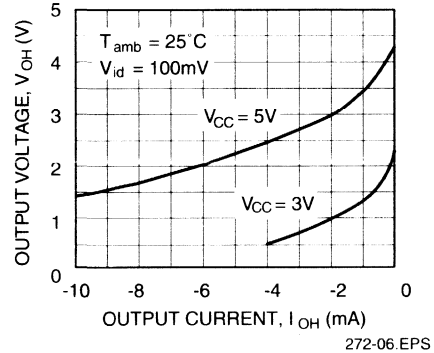


Figure 3b : IHigh Level Output Voltage versus High Level Output Current

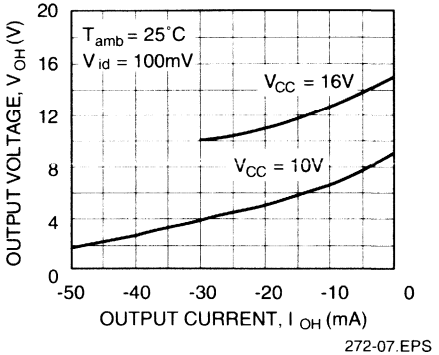


Figure 4a : Low Level Output Voltage versus Low Level Output Current

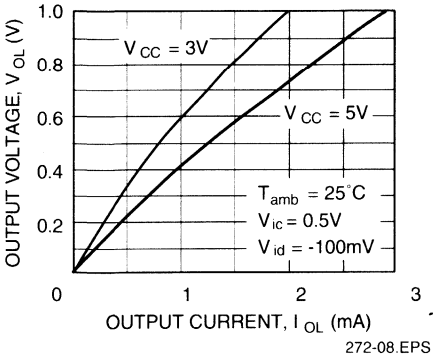
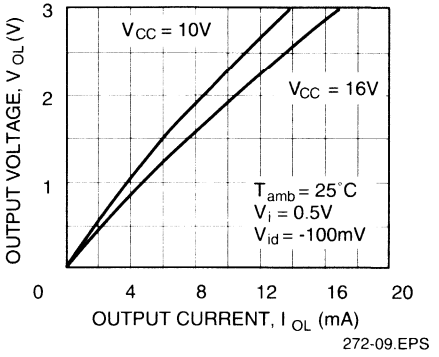


Figure 4b : ILow Level Output Voltage versus Low Level Output Current



TYPICAL CHARACTERISTICS (continued)

Figure 5 : Open Loop Frequency Response and Phase Shift

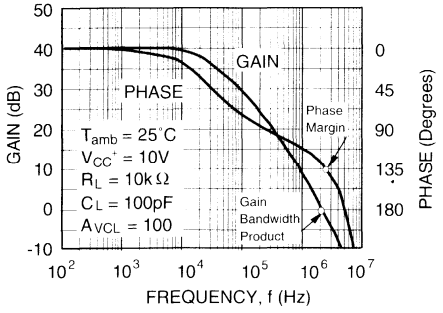


Figure 6 : Gain Bandwidth Product versus Supply Voltage

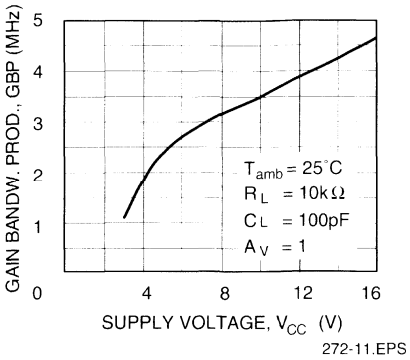


Figure 7 : Phase Margin versus Supply Voltage

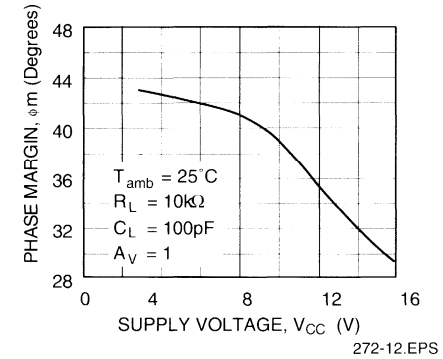


Figure 8 : Phase Margin versus Capacitive Load

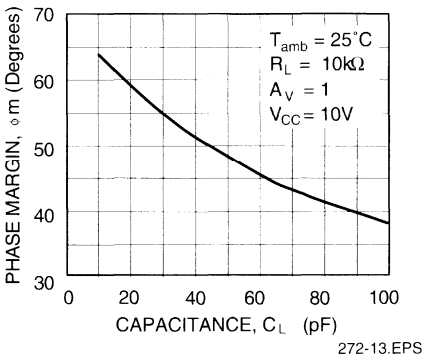


Figure 9 : Slew Rates versus Supply Voltage

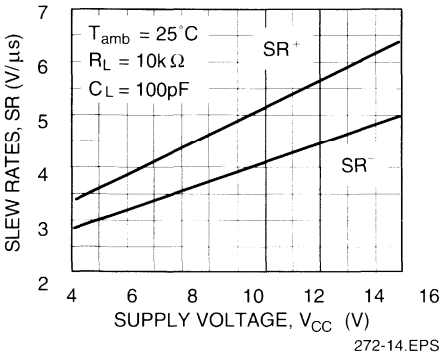
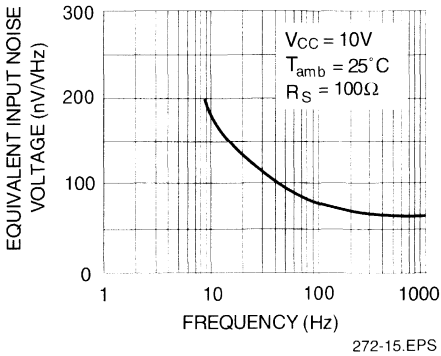


Figure 10 : Input Voltage Noise versus Frequency

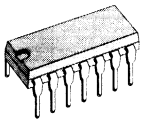


SGS-THOMSON MICROELECTRONICS

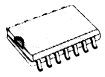
TS274C/I/M

HIGH SPEED QUAD CMOS OPERATIONAL AMPLIFIERS

- EXCELLENT PHASE MARGIN ON CAPACITIVE LOADS
- SYMETRICAL OUTPUT CURRENTS
- HIGH GAIN BANDWIDTH PRODUCT
- LOW OUTPUT DYNAMIC IMPEDANCE
- THE TRANSFER FUNCTION IS LINEAR
- PIN TO PIN COMPATIBLE WITH STANDARD QUAD OP-AMPs (TL084 -LM324)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS



N
DIP14
(Plastic Package)



D
SO14
(Plastic Micropackage)

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS274C/AC/BC	0°C, +70°C	•	•
TS274I/AI/BI	-40°C, +105°C	•	•
TS274M/AM/BM	-55°C, +125°C	•	•
Example : TS274ACN			

274-01.TBL

DESCRIPTION

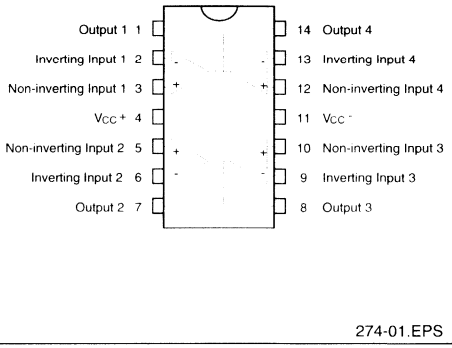
The TS274 series are low cost, low power quad operational amplifiers designed to operate with single or dual supplies. These operational amplifiers use the SGS-THOMSON silicon gate LIN MOS process giving them an excellent consumption-speed ratio. These series are ideally suited for low consumption applications.

Three power consumptions are available allowing to have always the best consumption-speed ratio :

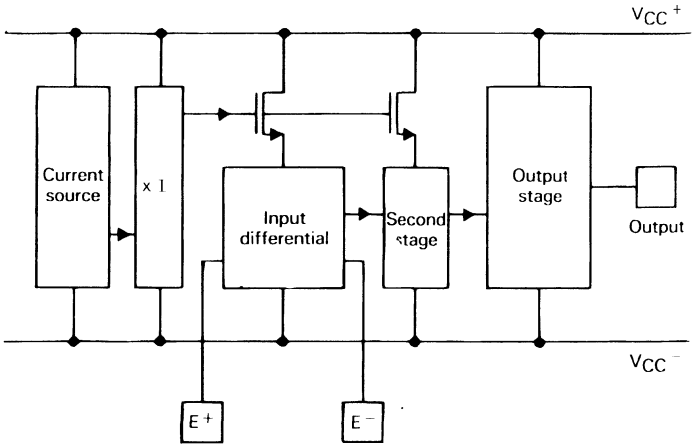
- I_{CC}= 10µA/amp. : TS27L4 (very low power)
- I_{CC}= 150µA/amp. : TS27M4 (low power)
- I_{CC}= 1mA/amp. : TS274 (high speed)

These CMOS amplifiers offer very high input impedance and extremely low input currents.
The major advantage versus JFET devices is the very low input currents drift with temperature (see figure 2).

PIN CONNECTIONS (top view)



BLOCK DIAGRAM



274-02.EPS

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage - (note 1)	18	V
V_{id}	Differential Input Voltage - (note 2)	±18	V
V_i	Input Voltage - (note 3)	-0.3 to 18	V
I_O	Output Current for $V_{CC}^+ \geq 15V$	±30	mA
I_{in}	Input Current	±5	mA
T_{oper}	Operating Free-Air Temperature Range TS274C/AC/BC TS274I/AI/BI TS274M/AM/BM	 0 to +70 -40 to +105 -55 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

274-09.TBL

Notes : 1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input and the output voltages must never exceed the magnitude of the positive supply voltage.

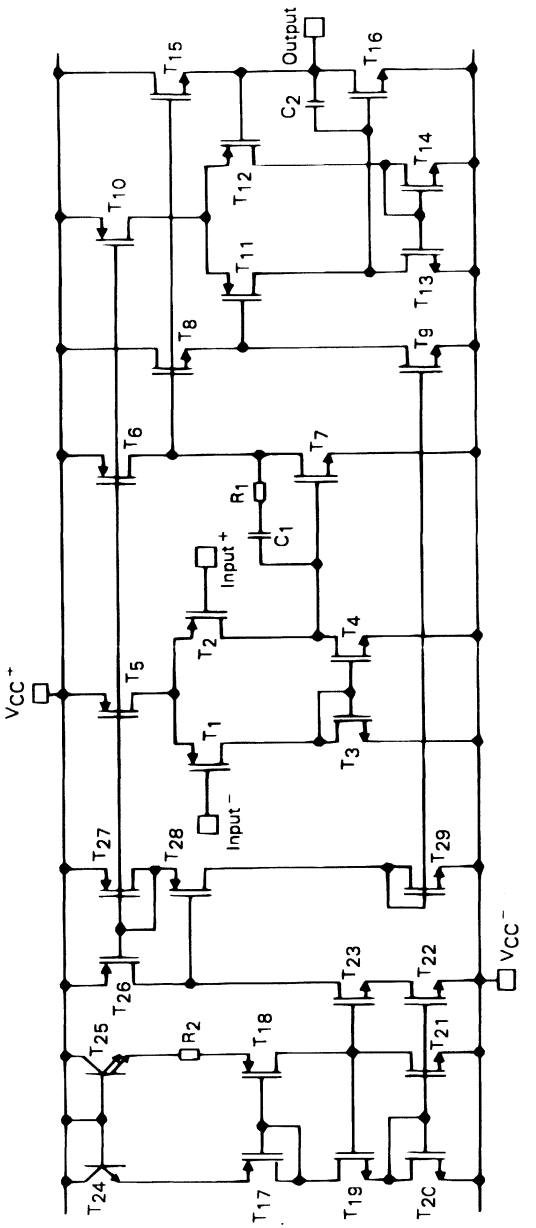
OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage	3 * to 16	V
V_{icm}	Common Mode Input Voltage Range	0 to V_{CC}^+ - 1.5	V

274-03.TBL

* Selected devices only.

SCHEMATIC DIAGRAM (for 1/4 TS274)



274-03.EPS

ELECTRICAL CHARACTERISTICS

$V_{CC}^+ = +10V$, $V_{CC}^- = 0V$, $T_{amb} = 25^oC$ (unless otherwise specified)

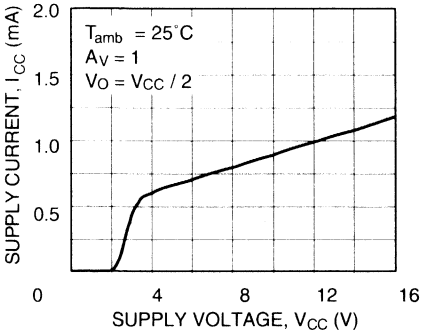
Symbol	Parameter	TS274C/AC/BC			TS274I/AI/BI TS274M/AM/BM			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage $V_O = 1.4V$, $V_{ic} = 0V$ TS274C/I/M TS274AC/AI/AM TS274BC/BI/BM $T_{min.} \leq T_{amb} \leq T_{max.}$ TS274C/I/M TS274AC/AI/AM TS274BC/BI/BM		1.1 0.9 0.25	10 5 2 12 6.5 3		1.1 0.9 0.25	10 5 2 12 6.5 3.5	mV
DV_{io}	Input Offset Voltage Drift		2			2		µV/°C
I_{io}	Input Offset Current - (note 1) $V_{ic} = 5V$, $V_o = 5V$ $T_{min.} \leq T_{amb} \leq T_{max.}$		1	 100		1	 200	pA
I_{ib}	Input Bias Current - (note 1) $V_{ic} = 5V$, $V_o = 5V$ $T_{min.} \leq T_{amb} \leq T_{max.}$		1	 150		1	 300	pA
V_{OH}	High Level Output Voltage $V_{id} = 100mV$, $R_L = 10k\Omega$ $T_{min.} \leq T_{amb} \leq T_{max.}$	8.2 8.1	8.4		8.2 8	8.4		V
V_{OL}	High Level Output Voltage $V_{id} = -100mV$			50			50	mV
A_{vd}	Large Signal Voltage Gain $V_o = 1V$ to $6V$, $R_L = 10k\Omega$, $V_{ic} = 5V$ $T_{min.} \leq T_{amb} \leq T_{max.}$	10 7	15		10 6	15		V/mV
GBP	Gain Bandwidth Product $A_v = 40dB$, $R_L = 10k\Omega$, $C_L = 100pF$ $f_{in} = 200kHz$		3.5			3.5		MHz
CMR	Common Mode Rejection Ratio $V_o = 1.4V$, $V_{ic} = 1V$ to $7.4V$	65	80		65	80		dB
SVR	Supply Voltage Rejection Ratio $V_{CC}^+ = 5V$ to $10V$, $V_o = 1.4V$	60	70		60	70		dB
I_{CC}	Supply Current (per amplifier) $A_v = 1$, no load, $V_o = 5V$ $T_{min.} \leq T_{amb} \leq T_{max.}$		1000	1500 1600		1000	1500 1700	µA
I_o	Output Short Circuit Current $V_{id} = 100mV$, $V_o = 0V$	45	60	85	45	60	85	mA
I_{sink}	Output Sink Current $V_{id} = -100mV$, $V_o = V_{CC}$	35	45	65	35	45	65	mA
SR	Slew-Rate at Unity Gain $R_L = 10k\Omega$, $C_L = 100pF$, $V_i = 3$ to $7V$		5.5			5.5		V/µs
$\varnothing m$	Phase Margin at Unity Gain $A_v = 40dB$, $R_L = 10k\Omega$, $C_L = 100pF$		40			40		Degrees
K_{ov}	Overshoot Factor		30			30		%
e_n	Equivalent Input Noise Voltage $f = 1kHz$, $R_S = 100\Omega$		30			30		$\frac{nV}{\sqrt{Hz}}$
V_{O1}/V_{O2}	Channel Separation		120			120		dB

Note : 1. Maximum values including unavoidable inaccuracies of the industrial test.

274-04.TBL

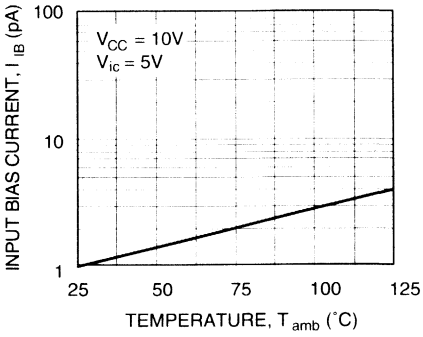
TYPICAL CHARACTERISTICS

Figure 1 : Supply Current (each amplifier) versus Supply Voltage



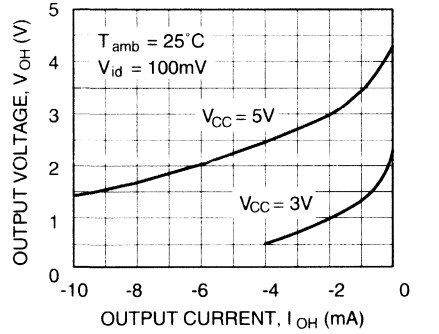
274-04.EPS

Figure 2 : Input Bias Current versus Free Air Temperature



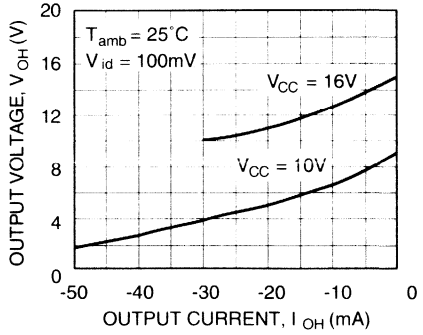
274-05.EPS

Figure 3a : High Level Output Voltage versus High Level Output Current



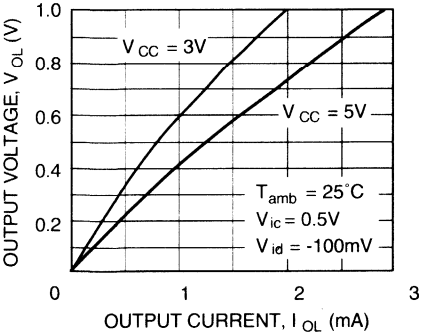
274-06.EPS

Figure 3b : High Level Output Voltage versus HIgh Level Output Current



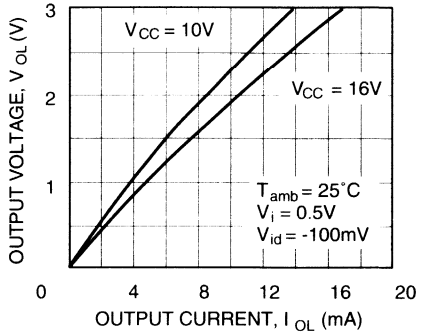
274-07.EPS

Figure 4a : High Level Output Voltage versus High Level Output Current



274-08.EPS

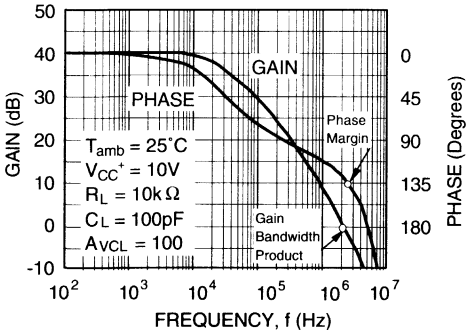
Figure 4b : High Level Output Voltage versus High Level Output Current



274-09.EPS

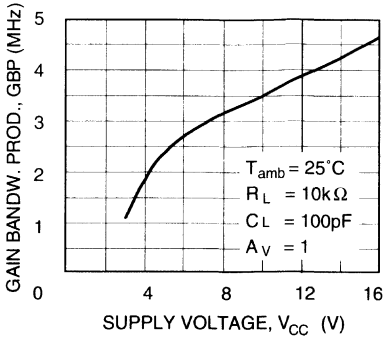
TYPICAL CHARACTERISTICS (continued)

Figure 5 : Open Loop Frequency Response and Phase Shift



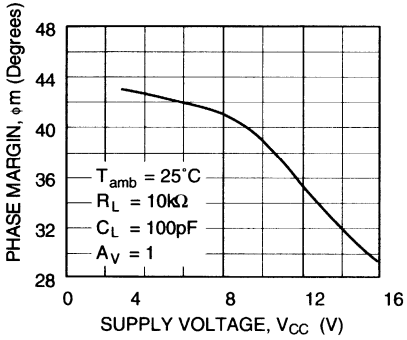
274-10.EPS

Figure 6 : Gain Bandwidth Product versus Supply Voltage



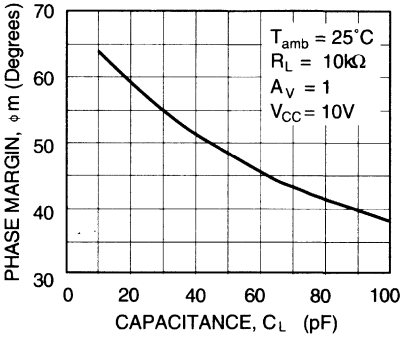
274-11.EPS

Figure 7 : Phase Margin versus Supply Voltage



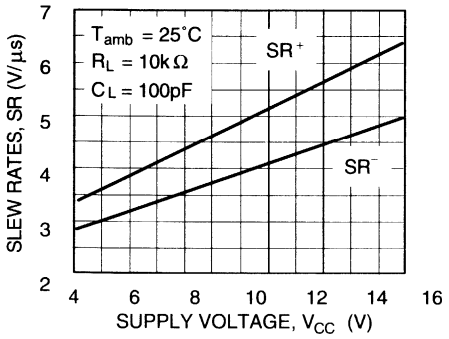
274-12.EPS

Figure 8 : Phase Margin versus Capacitive Load



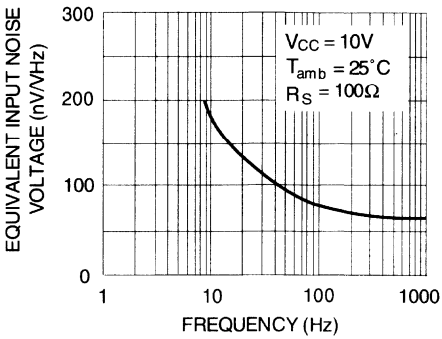
274-13.EPS

Figure 9 : Slew Rates versus Supply Voltage



274-14.EPS

Figure 10 : Input Voltage Noise versus Frequency



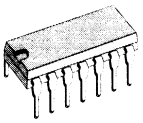
274-15.EPS

SGS-THOMSON MICROELECTRONICS

TS339C/I/M

MICROPOWER QUAD CMOS VOLTAGE COMPARATORS

- EXTREMELY LOW SUPPLY CURRENT : 9µA TYP / COMPARATOR
- WIDE SINGLE SUPPLY RANGE (3V TO 16V) OR DUAL SUPPLIES (±1.5V TO ±8V)
- EXTREMELY LOW INPUT BIAS CURRENT : 1pA TYP
- EXTREMELY LOW INPUT OFFSET CURRENT : 1pA TYP
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GND
- BUILT-IN ESD PROTECTION
- HIGH INPUT IMPEDANCE : $10^{12}\Omega$ TYP
- FAST RESPONSE TIME : 1.5µs TYP FOR 5mV OVERDRIVE
- PIN-TO-PIN AND FUNCTIONALLY COMPATIBLE WITH BIPOLAR LM339



N
DIP14
(Plastic Package)

D
SO14
(Plastic Micropackage)

DESCRIPTION

The TS339 is a micropower CMOS quad voltage comparator with extremely low consumption of 9µA typ / comparator (20 times less than bipolar LM339). Similar performances are offered by the quad micropower comparator TS3704 with a push-pull CMOS output.

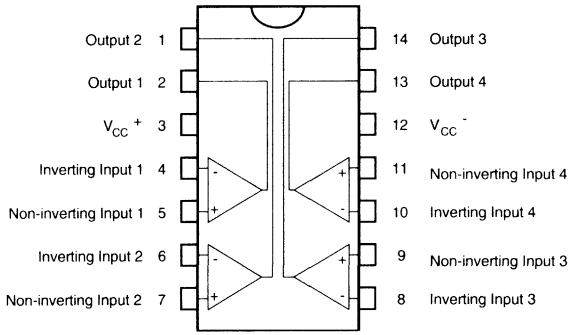
Thus response times remain similar to the LM339.

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS393C	0°C, +70°C	•	•
TS393I	-40°C, +105°C	•	•
TS393M	-55°C, +125°C	•	•
Example : TS393CN			

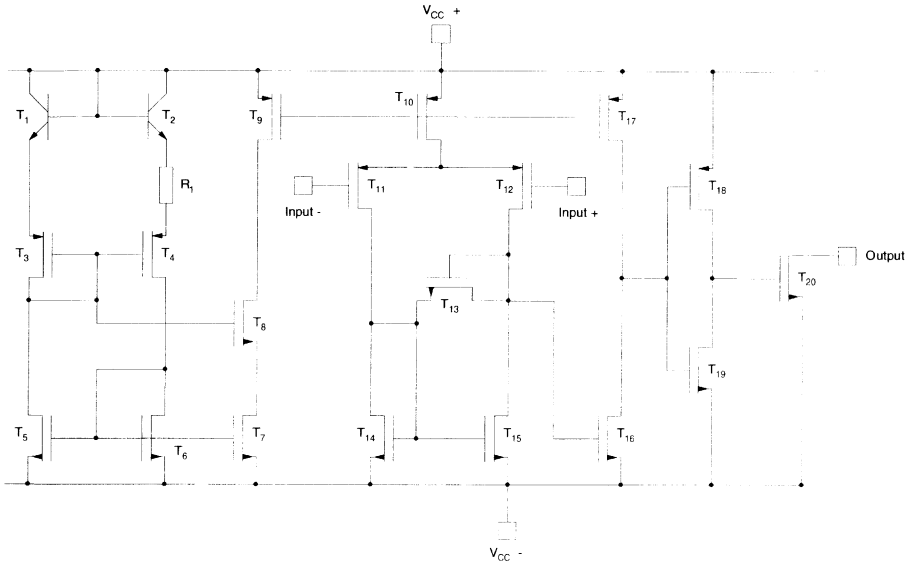
339-01.TBL

PIN CONNECTIONS (top view)



339-01.EPS

SCHEMATIC DIAGRAM (for 1/4 TS339)



MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}^+	Supply Voltage - (note 1)		18	V
V_{id}	Differential Input Voltage - (note 2)		±18	V
V_i	Input Voltage - (note 3)		18	V
V_O	Output Voltage		18	V
I_O	Output Current		20	mA
T_{oper}	Operating Free-Air Temperature Range	TS339C TS339I TS339M	0 to +70 -40 to +105 -55 to +125	°C
T_{stg}	Storage Temperature Range		-65 to +150	°C

339-03.TBL

Notes : 1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input and the output voltages must never exceed the magnitude of the positive supply voltage.
4. Short circuit from outputs to V_{CC}^+ can cause excessive heating and eventual destruction.

OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}^+	Supply Voltage	TS339C,I TS339M	3 to 16 4 to 16	V
V_{icm}	Common Mode Input Voltage Range		0 to V_{CC}^+ -1.5	V

339-04.TBL

ELECTRICAL CHARACTERISTICS

$V_{CC}^+ = 5V$, $V_{CC}^- = 0V$, $T_{amb} = 25°C$ (unless otherwise specified)

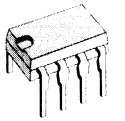
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage - (note 1) $V_{ic} = V_{icm\ min.}$, $V_{CC}^+ = 5V$ to $10V$ $T_{min.} \leq T_{amb} \leq T_{max.}$		1.4	5 6.5	mV
I_{io}	Input Offset Current - (note 2) $V_{ic} = 2.5\ V$ $T_{min.} \leq T_{amb} \leq T_{max.}$		1	 300	pA
I_{ib}	Input Bias Current - (note 2) $V_{ic} = 2.5\ V$ $T_{min.} \leq T_{amb} \leq T_{max.}$		1	 600	pA
V_{icm}	Input Common Mode Voltage Range $T_{min.} \leq T_{amb} \leq T_{max.}$	0 to V_{CC}^+ -1.2 0 to V_{CC}^+ -1.5			V
CMR	Common-mode Rejection Ratio $V_{ic} = V_{icm\ min.}$		75		dB
SVR	Supply Voltage Rejection Ratio $V_{CC}^+ = +5V$ to $+10V$		85		dB
I_{OH}	High Level Output Current $V_{id} = 1V$, $V_{OH} = +5V$ $T_{min.} \leq T_{amb} \leq T_{max.}$		2	40 1000	nA
V_{OL}	Low Level Output Voltage $V_{id} = -1V$, $I_{OL} = 6mA$ $T_{min.} \leq T_{amb} \leq T_{max.}$		350	400 650	mV
I_{CC}	Supply Current (4 comparators) No load - Outputs low $T_{min.} \leq T_{amb} \leq T_{max.}$		36	80 100	µA
t_{PLH}	Response Time Low to High $V_{ic} = 0V$, f = 10kHz, $R_L = 5.1k\Omega$, $C_L = 15pF$, Overdrive = 5mV Overdrive = 10mV Overdrive = 20mV Overdrive = 40mV TTL Input		1.5 1.2 1.1 0.9 0.8		µs
t_{PHL}	Response Time High to Low $V_{ic} = 0V$, f = 10kHz, $R_L = 5.1kW$, $C_L = 15pF$, Overdrive = 5mV Overdrive = 10mV Overdrive = 20mV Overdrive = 40mV TTL Input		2.5 1.9 1.2 0.8 0.08		µs
t_{THL}	Transition Time High to Low f = 10kHz, $C_L = 15pF$, $R_L = 5.1k\Omega$, Overdrive 50mV		25		ns

339-04.TBL

Note : 1. The specified offset voltage is the maximun value required to drive the output up to 4.5V or down to 0.3V.
2. Maximum values including unavoidable inaccuracies of the industrial test.

LOW POWER DUAL CMOS VOLTAGE COMPARATORS

- WIDE SINGLE SUPPLY RANGE OR DUAL SUPPLIES 3V TO 16V OR ±1.5V to ±8V
- VERY LOW SUPPLY CURRENT : 0.1mA/COMP INDEPENDENT OF SUPPLY VOLTAGE
- EXTREMELY LOW INPUT BIAS CURRENT : 1pA TYP
- EXTREMELY LOW INPUT OFFSET CURRENT : 1pA TYP
- LOW INPUT OFFSET VOLTAGE
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GND
- LOW OUTPUT SATURATION VOLTAGE 150mV TYP
- OUTPUT COMPATIBLE WITH TTL, MOS AND CMOS
- BUILT-IN ESD PROTECTION
- HIGH INPUT IMPEDANCE $10^{12}\Omega$ TYP
- FAST RESPONSE TIME : 200ns TYP FOR TTL LEVEL INPUT STEP



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

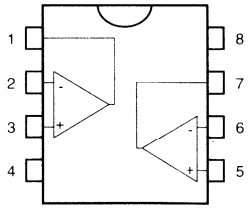
ORDER CODES

Part Number	Temperature Range	Package N	Package D
TS372C	0°C, +70°C	•	•
TS372I	-40°C, +105°C	•	•
TS372M	-55°C, +125°C	•	•

Example : TS372CN

372-01.TBL

PIN CONNECTIONS (top view)



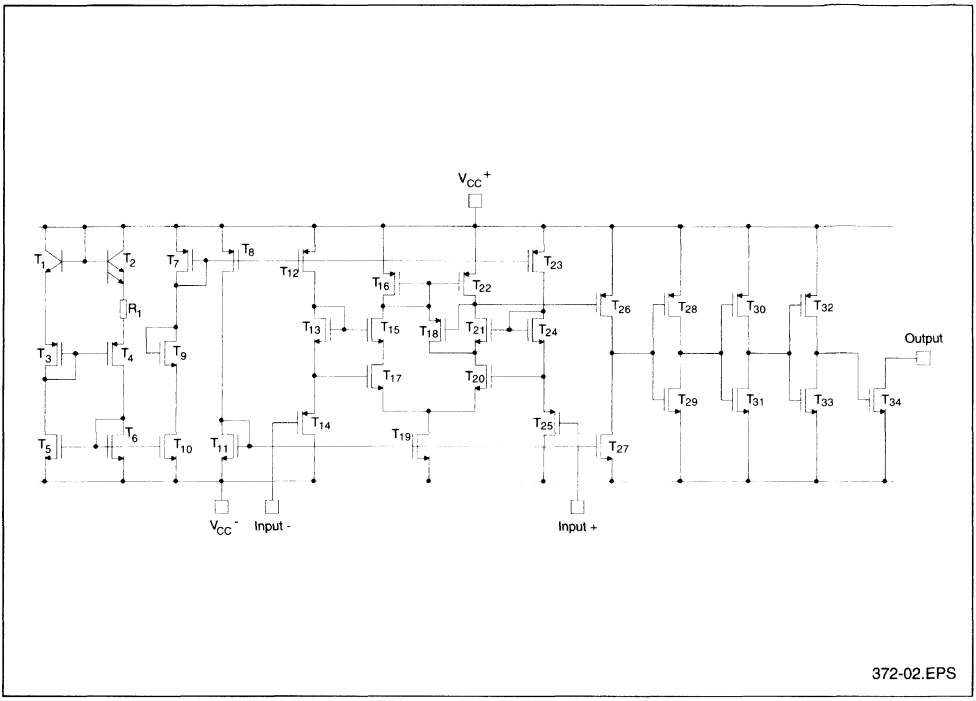
1 - Output 1
2 - Inverting Input 1
3 - Non-inverting Input 1
4 - V_{CC}^-
5 - Non-inverting Input 2
6 - Inverting Input 2
7 - Output 2
8 - V_{CC}^+

372-01.EPS

DESCRIPTION

These devices consist of two independent precision voltage comparators, designed to operate with single or dual supplies.
These differential comparators use the SGS-THOMSON silicon lin MOS process giving them an excellent consumption-speed ratio.
These devices are ideally suited for low consumption applications.

SCHEMATIC DIAGRAM (for 1/2 TS372)



MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage - (note 1)	18	V
V_{id}	Differential Input Voltage - (note 2)	±18	V
V_i	Input Voltage - (note 3)	18	V
V_O	Output Voltage	18	V
I_O	Output Current	20	mA
	Duration of Output Short-Circuit to GND - (note 4)	Infinite	
T_{oper}	Operating Free-Air Temperature Range TS372C TS372I TS372M	 0 to +70 -40 to +105 -55 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

Notes : 1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input and the output voltages must never exceed the magnitude of the positive supply voltage.
4. Short circuit from outputs to V_{CC}^+ can cause excessive heating and eventual destruction.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage	3* to 16	V
V_{icm}	Common Mode Input Voltage Range	0 to V_{CC}^+ -1.5	V

* Selected devices only

ELECTRICAL CHARACTERISTICS

V_{CC}^+ = 5V, V_{CC}^- = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage (V_{ic} = $V_{icm\ min.}$) - (note 1)					mV
	T_{amb} = 25°C			2	10	
	$T_{min.} \le T_{amb} \le T_{max.}$				12	
I_{io}	Input Offset Current - (note 2)					pA
	T_{amb} = 25°C			1		
	$T_{min.} \le T_{amb} \le T_{max.}$	TS372C			100	
		TS372I/TS372M			200	
I_{ib}	Input Bias Current - (note 2)					pA
	T_{amb} = 25°C			1		
	$T_{min.} \le T_{amb} \le T_{max.}$	TS372C			150	
		TS372I/TS372M			300	
V_{icm}	Input Common Mode Voltage Range					V
	T_{amb} = 25°C		0 to V_{CC}^+ -2			
	$T_{min.} \le T_{amb} \le T_{max.}$	TS372C	0 to V_{CC}^+ -2.25			
		TS372I/TS372M	0 to V_{CC}^+ -2.5			
I_{OH}	High Level Output Current (V_{id} = 1V)					
	T_{amb} = 25°C	V_{OH} = 5V		0.1		nA
	$T_{min.} \le T_{amb} \le T_{max.}$	V_{OH} = 15V			1	µA
V_{OL}	Low Level Output Voltage (V_{id} = -1V, I_{OL} = 4mA)					mV
	T_{amb} = 25°C			100	400	
	$T_{min.} \le T_{amb} \le T_{max.}$				700	
I_{OL}	Low Level Output Current (V_{id} = -1V, V_{OL} = 1.5V)		6	45		mA
I_{CC}	Supply Current (2 comparators) (V_{id} = +1V, no load)			0.3	0.75	mA

372-04.TBL

SWITCHING CHARACTERISTICS (V_{CC}^+ = 5V, T_{amb} = 25°C)

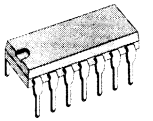
Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{re}	Response Time (R_L = 5.1kΩ connected to 5V, C_L = 15pF - note 3)				ns
	• 100mV input step with 5mV overdrive		600		
	• TTL level input step		200		

372-05.TBL

Notes : 1. The specified offset voltage is the maximum value required to drive the output down to 400mV or up to 4V with R_L = 100kΩ to V_{CC}^+.
2. Maximum values including unavoidable inaccuracies of the industrial test.
3. The response time which is specified is the internal between the input signal and the instant when the output signal crosses 1.4V.

LOW POWER QUAD CMOS VOLTAGE COMPARATORS

- WIDE SINGLE SUPPLY RANGE OR DUAL SUPPLIES 3V TO 16V OR ±1.5V to ±8V
- VERY LOW SUPPLY CURRENT : 0.1mA/COMP INDEPENDENT OF SUPPLY VOLTAGE
- EXTREMELY LOW INPUT BIAS CURRENT : 1pA TYP
- EXTREMELY LOW INPUT OFFSET CURRENT : 1pA TYP
- LOW INPUT OFFSET VOLTAGE
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GND
- LOW OUTPUT SATURATION VOLTAGE 150mV TYP
- OUTPUT COMPATIBLE WITH TTL, MOS AND CMOS
- BUILT-IN ESD PROTECTION
- HIGH INPUT IMPEDANCE $10^{12}\Omega$ TYP
- FAST RESPONSE TIME : 200ns TYP FOR TTL LEVEL INPUT STEP



N
DIP14
(Plastic Package)

D
SO14
(Plastic Micropackage)

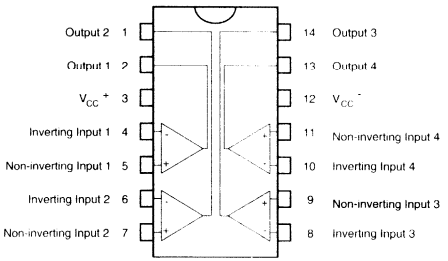
ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS374C	0°C, +70°C	•	•
TS374I	-40°C, +105°C	•	•
TS374M	-55°C, +125°C	•	•

Example : TS374CN

374-01.TBL

PIN CONNECTIONS (top view)



374-01.EPS

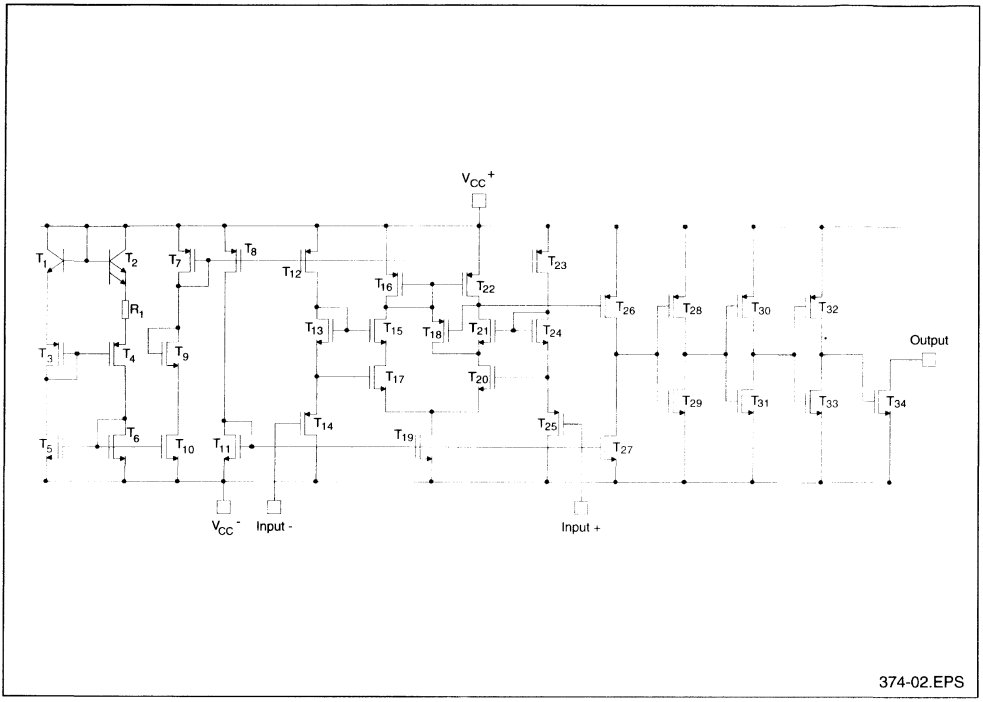
DESCRIPTION

These devices consist of four independent precision voltage comparators, designed to operate with single or dual supplies.

These differential comparators use the SGS-THOMSON silicon lin MOS process giving them an excellent consumption-speed ratio.

These devices are ideally suited for low consumption applications.

SCHEMATIC DIAGRAM (for 1/4 TS374)



MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage - (note 1)	18	V
V_{id}	Differential Input Voltage - (note 2)	±18	V
V_i	Input Voltage - (note 3)	18	V
V_O	Output Voltage	18	V
I_O	Output Current	20	mA
	Duration of Output Short-Circuit to GND - (note 4)	Infinite	
T_{oper}	Operating Free-Air Temperature Range TS374C TS374I TS374M	 0 to +70 -40 to +105 -55 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

374-02 TBL

Notes : 1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input and the output voltages must never exceed the magnitude of the positive supply voltage.
4. Short circuit from outputs to V_{CC}^+ can cause excessive heating and eventual destruction.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage	3 * to 16	V
V_{icm}	Common Mode Input Voltage Range	0 to V_{CC}^+ -1.5	V

374-03 TBL

* Selected devices only

ELECTRICAL CHARACTERISTICSED

$V_{CC}^+ = 5V$, $V_{CC}^- = 0V$, $T_{amb} = 25°C$ (unless otherwise specified)

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage ($V_{ic} = V_{icm\ min.}$) - (note 1)					mV
	$T_{amb} = 25°C$			2	10	
	$T_{min.} \le T_{amb} \le T_{max.}$				12	
I_{io}	Input Offset Current - (note 2)					pA
	$T_{amb} = 25°C$			1		
	$T_{min.} \le T_{amb} \le T_{max.}$	TS374C			100	
		TS374I/TS374M			200	
I_{ib}	Input Bias Current - (note 2)					pA
	$T_{amb} = 25°C$			1		
	$T_{min.} \le T_{amb} \le T_{max.}$	TS374C			150	
		TS374I/TS374M			300	
V_{icm}	Input Common Mode Voltage Range					V
	$T_{amb} = 25°C$		0 to V_{CC}^+ -2			
	$T_{min.} \le T_{amb} \le T_{max.}$	TS374C	0 to V_{CC}^+ -2.25			
		TS374I/TS374M	0 to V_{CC}^+ -2.5			
I_{OH}	High Level Output Current ($V_{id} = 1V$)					
	$T_{amb} = 25°C$	$V_{OH} = 5V$		0.1		nA
	$T_{min.} \le T_{amb} \le T_{max.}$	$V_{OH} = 15V$			1	µA
V_{OL}	Low Level Output Voltage ($V_{id} = -1V$, $I_{OL} = 4mA$)					mV
	$T_{amb} = 25°C$			100	400	
	$T_{min.} \le T_{amb} \le T_{max.}$				700	
I_{OL}	Low Level Output Current ($V_{id} = -1V$, $V_{OL} = 1.5V$)		6	45		mA
I_{CC}	Supply Current (4 comparators) ($V_{id} = +1V$, no load)			0.6	1	mA

374-04.TBL

SWITCHING CHARACTERISTICS ($V_{CC}^+ = 5V$, $T_{amb} = 25°C$)

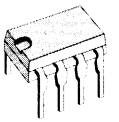
Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{re}	Response Time ($R_L = 5.1k\Omega$ connected to 5V, $C_L = 15pF$ - (note 3)				ns
	• 100mV input step with 5mV overdrive		600		
	• TTL level input step		200		

374-05.TBL

Notes : 1. The specified offset voltage is the maximum value required to drive the output down to 400mV or up to 4V with $R_L = 100k\Omega$ to V_{CC}^+.
2. Maximum values including unavoidable inaccuracies of the industrial test.
3. The response time which is specified is the internal between the input signal and the instant when the output signal crosses 1.4V.

MICROPOWER DUAL CMOS VOLTAGE COMPARATORS

- EXTREMELY LOW SUPPLY CURRENT : 9µA TYP/COMPARATOR
- WIDE SINGLE SUPPLY RANGE (3V to 16V) OR DUAL SUPPLIES (±1.5V to ±8V)
- EXTREMELY LOW INPUT BIAS CURRENT : 1pA TYP
- EXTREMELY LOW INPUT OFFSET CURRENT : 1pA TYP
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GND
- BUILT-IN ESD PROTECTION
- HIGH INPUT IMPEDANCE $10^{12}\Omega$ TYP
- FAST RESPONSE TIME : 2.5µs TYP FOR 5mV OVERDRIVE
- PIN-TO-PIN AND FUNCTIONALLY COMPATIBLE WITH BIPOLAR LM393



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

DESCRIPTION

The TS393 is a micropower CMOS dual voltage comparator with extremely low consumption of 9µA typ / comparator (20 times less than bipolar LM393). Similar performances are offered by the dual micropower comparator TS3702 with a push-pull CMOS output.

Thus response times remain similar to the LM393.

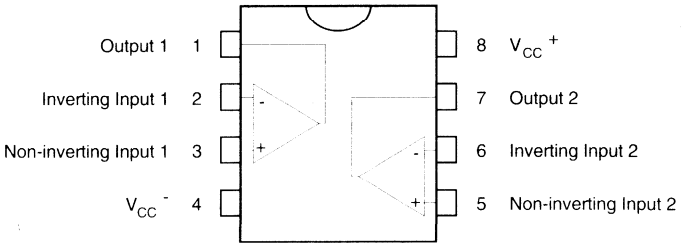
ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS393C	0°C, +70°C	•	•
TS393I	-40°C, +105°C	•	•
TS393M	-55°C, +125°C	•	•

Example : TS393CN

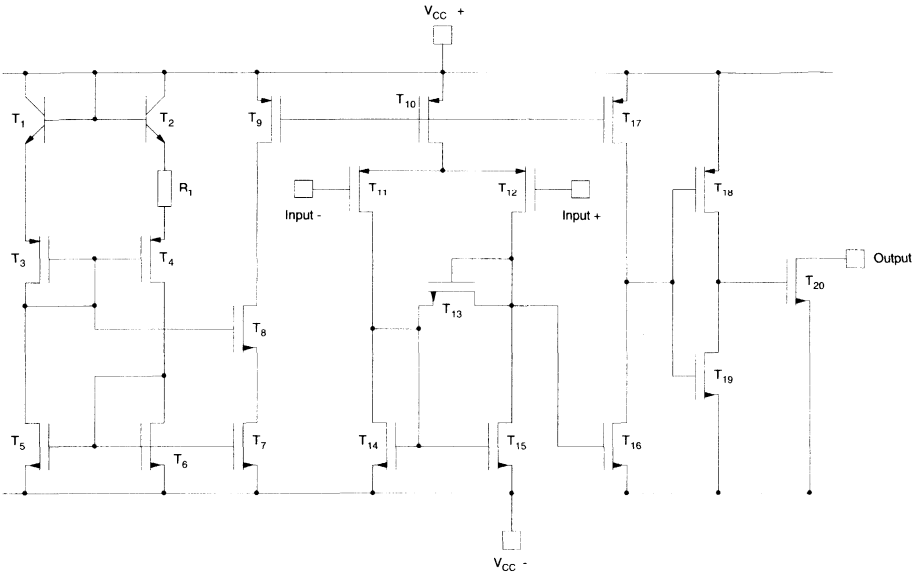
393-01.TBL

PIN CONNECTIONS (top view)



393-01.EPS

SCHEMATIC DIAGRAM (for 1/2 TS393)



393-02.EPS

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}^+	Supply Voltage - (note 1)		18	V
V_{id}	Differential Input Voltage - (note 2)		±18	V
V_i	Input Voltage - (note 3)		18	V
V_O	Output Voltage		18	V
I_O	Output Current		20	mA
T_{oper}	Operating Free-Air Temperature Range	TS393C TS393I TS393M	0 to +70 -40 to +105 -55 to +125	°C
T_{stg}	Storage Temperature Range		-65 to +150	°C

Notes : 1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input and the output voltages must never exceed the magnitude of the positive supply voltage.
4. Short circuit from outputs to V_{CC}^+ can cause excessive heating and eventual destruction.

OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}^+	Supply Voltage	TS393C,I TS393M	3 to 16 4 to 16	V
V_{icm}	Common Mode Input Voltage Range		0 to V_{CC}^+ -1.5	V

ELECTRICAL CHARACTERISTICS

V_{CC}^+ = 5V, V_{CC}^- = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage $V_{IC} = V_{Icm\ min.}$, V_{CC}^+ = 5V to 10V - (note 1) $T_{min.} \leq T_{amb} \leq T_{max.}$		1.4	5 6.5	mV
I_{io}	Input Offset Current - (note 2) V_{IC} = 2.5 V $T_{min.} \leq T_{amb} \leq T_{max.}$		1	 300	pA
I_{ib}	Input Bias Current - (note 2) V_{IC} = 2.5 V $T_{min.} \leq T_{amb} \leq T_{max.}$		1	 600	pA
V_{icm}	Input Common Mode Voltage Range $T_{min.} \leq T_{amb} \leq T_{max.}$	0 to V_{CC}^+-1.2 0 to V_{CC}^+ -1.5			V
CMR	Common-mode Rejection Ratio $V_{IC} = V_{icm\ min.}$		71		dB
SVR	Supply Voltage Rejection Ratio V_{CC}^+ = +5V to +10V		80		dB
I_{OH}	High Level Output Current V_{id} = 1V, V_{OH} = +5V $T_{min.} \leq T_{amb} \leq T_{max.}$		2	40 1000	nA
V_{OL}	Low Level Output Voltage V_{id} = -1V, I_{OL} = 6mA $T_{min.} \leq T_{amb} \leq T_{max.}$		260	400 650	mV
I_{CC}	Supply Current (2 comparators) No load - Outputs low $T_{min.} \leq T_{amb} \leq T_{max.}$		20	40 50	µA
t_{PLH}	Response Time Low to High V_{ic} = 0V, f = 10kHz, R_L = 5.1kΩ, C_L = 15pF, Overdrive = 5mV Overdrive = 10mV Overdrive = 20mV Overdrive = 40mV TTL Input		1.5 1.2 1.0 0.8 0.7		µs
t_{PHL}	Response Time High to Low V_{ic} = 0V, f = 10kHz, R_L = 5.1kW, C_L = 15pF, Overdrive = 5mV Overdrive = 10mV Overdrive = 20mV Overdrive = 40mV TTL Input		2.5 1.9 1.2 0.8 0.08		µs

393-04.TBL

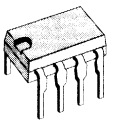
Note : 1. The specified offset voltage is the maximun value required to drive the output up to 4.5V or down to 0.3V.
2. Maximum values including unavoidable inaccuracies of the industrial test.

SGS-THOMSON MICROELECTRONICS

TS555C/I/M

LOW POWER SINGLE CMOS TIMERS

- VERY LOW POWER CONSUMPTION :
- 100µA typ at V_{CC} = 5V
- HIGH MAXIMUM ASTABLE FREQUENCY 2.7MHz
- PIN-TO-PIN AND FUNCTIONALLY COMPATIBLE WITH BIPOLAR NE555
- VOLTAGE RANGE : +2V to +18V
- HIGH OUTPUT CURRENT CAPABILITY
- SUPPLY CURRENT SPIKES REDUCED DURING OUTPUT TRANSITIONS
- HIGH INPUT IMPEDANCE : 10^{12} Ω
- OUTPUT COMPATIBLE WITH TTL,CMOS AND LOGIC MOS



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

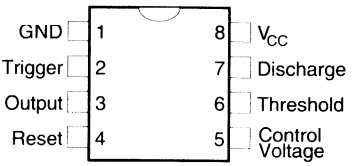
ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS555C	0°C. +70°C	●	●
TS555I	-40, +105°C	●	●
TS555M	-55, +125°C	●	●

Examples : TS555CD , TS555IN

TS555-01.TBL

PIN CONNECTIONS (top view)

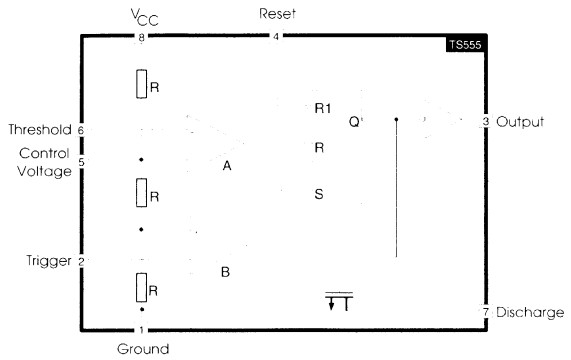


TS555-01.EPS

DESCRIPTION

The TS555 is a single CMOS timer which offers very low consumption ($I_{CC(TYP)}$ TS555 = 100µA $I_{CC(TYP)}$ NE555 = 3mA) and high frequency ($f_{(max.)}$ TS555 = 2.7MHz - $f_{(max.)}$ NE555 = 0.1 MHz) Thus, either in Monostable or Astable mode, timing remains very accurate.
The TS555 provides reduced supply current spikes during output transitions, which enables the use of lower decoupling capacitors compared to those required by bipolar NE555.
Timing capacitors can also be minimized due to high input impedance (10^{12} Ω).

BLOCK DIAGRAM



TS555-02.EPS

RESET	TRIGGER	THRESHOLD	OUTPUT
Low	x	x	Low
High	Low	x	High
High	High	High	Low
High	High	Low	Previous State

LOW ↔ Level Voltage ≤ Min voltage specified

HIGH ↔ Level Voltage ≥ Max voltage specified

X ↔ Irrelevant

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	+18	V
T_J	Junction Temperature	+150	°C

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
T_{OPER}	Operating Temperature Range		°C
	TS555C	0 to +70	
	TS555I	-40 to +105	
	TS555M	-55 to +125	
T_{STG}	Storage Temperature Range	-65 to +150	°C

SCHEMATIC DIAGRAM

TS555-03.EPS

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	+2 to +16	V

STATIC ELECTRICAL CHARACTERISTICS

V_{CC} = +2V, T_{amb} = +25°C, Reset to V_{CC} (unless otherwise specified)

Symbol	Parameter	TS555C-TS555I-TS555M			Unit
		Min.	Typ	Max.	
I_{CC}	Supply Current (no load, High and Low States) T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		65	200 200	µA
V_{CL}	Control Voltage T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	1.2 1.1	1.3	1.4 1.5	V
V_{dis}	Discharge Saturation Voltage (I_{dis} = 1mA) T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		0.05	0.2 0.25	V
V_{OL}	Low Level Output Voltage (I_{sink} = 1mA) T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		0.1	0.3 0.35	V
V_{OH}	High Level Output Voltage (I_{source} = -0.3mA) T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	1.5 1.5	1.9		V
V_{trig}	Trigger Voltage T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	0.4 0.3	0.67	0.95 1.05	V
I_{trig}	Trigger Current		10		pA
I_{TH}	Threshold Current		10		pA
V_{reset}	Reset Voltage T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	0.4 0.3	1.1	1.5 2.0	V
I_{reset}	Reset Current		10		pA
I_{dis}	Discharge Pin Leakage Current		1	100	nA

STATIC ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = +5V, T_{amb} = +25°C, Reset to V_{CC} (unless otherwise specified)

Symbol	Parameter	TS555C-TS555I-TS555M			Unit
		Min.	Typ	Max.	
I_{CC}	Supply Current (no load, High and Low States) T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		110	250 250	µA
V_{CL}	Control Voltage T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	2.9 2.8	3.3	3.8 3.9	V
V_{dis}	Discharge Saturation Voltage (I_{dis} = 10mA) T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		0.2	0.3 0.35	V
V_{OL}	Low Level Output Voltage (I_{sink} = 8mA) T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		0.3	0.6 0.8	V
V_{OH}	High Level Output Voltage (I_{source} = -2mA) T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	4.4 4.4	4.6		V
V_{trig}	Trigger Voltage T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	1.36 1.26	1.67	1.96 2.06	V
I_{trig}	Trigger Current		10		pA
I_{TH}	Threshold Current		10		pA
V_{reset}	Reset Voltage T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	0.4 0.3	1.1	1.5 2.0	V
I_{reset}	Reset Current		10		pA
I_{dis}	Discharge Pin Leakage Current		1	100	nA

TS555-07.TBL

STATIC ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = +12V, T_{amb} = +25°C, Reset to V_{CC} (unless otherwise specified)

Symbol	Parameter	TS555C-TS555I-TS555M			Unit
		Min.	Typ	Max.	
I_{CC}	Supply Current (no load, High and Low States) T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		170	400 400	µA
V_{CL}	Control Voltage T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	7.4 7.3	8	8.6 8.7	V
V_{dis}	Discharge Saturation Voltage (I_{dis} = 80mA) T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		0.09	1.6 2.0	V
V_{OL}	Low Level Output Voltage (I_{sink} = 50mA) T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		1.2	2 2.8	V
V_{OH}	High Level Output Voltage (I_{source} = -10mA) T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	10.5 10.5	11		V
V_{trig}	Trigger Voltage T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	3.2 3.1	4	4.8 4.9	V
I_{trig}	Trigger Current		10		pA
I_{TH}	Threshold Current		10		pA
V_{reset}	Reset Voltage T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	0.4 0.3	1.1	1.5 2.0	V
I_{reset}	Reset Current		10		pA
I_{dis}	Discharge Pin Leakage Current		1	100	nA

DYNAMIC ELECTRICAL CHARACTERISTICS

T_{amb} = +25°C, Reset to V_{CC} (unless otherwise specified)

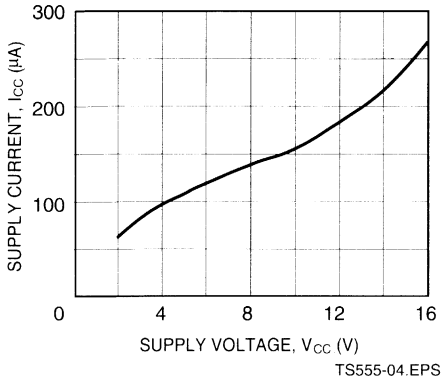
Symbol	Parameter	TS555C-TS555I-TS555M			Unit
		Min	Typ	Max	
	Timing Accuracy (Monostable) - (note 1) R = 10kΩ , C = 0.1µF				%
	V_{CC} = + 2V		1		
	V_{CC} = + 5V		2		
	V_{CC} = +12V		4		
	Timing Shift with supply voltage variations (Monostable) R = 10kΩ , C = 0.1µF, V_{CC} = + 5V +/-1V		0.38		%/V
	Timing Shift with temperature $T_{min.} \leq T_{amb} \leq T_{max.}$, V_{CC} = + 5V		75		ppm/°C
f_{max}	Maximum astable frequency R_A = 470Ω , R_B = 200Ω, C = 200pF , V_{CC} = + 5V			2.7	MHz
	Astable frequency accuracy - (note 2) R_A = R_B = 1kΩ to 100kΩ, C = 0.1µF				%
	V_{CC} = + 5V		3		
	V_{CC} = + 12V		3		
	Timing Shift with supply voltage variations (Astable mode) R_A = R_B = 1kΩ to 100kΩ, C = 0.1µF, V_{CC} = 5 to+ 12V		0.1		%/V
t_r	Output Rise Time (V_{CC} = + 5V , C_{load} = 10pF)		25		ns
t_f	Output Fall Time (V_{CC} = + 5V , C_{load} = 10pF)		20	-	ns
t_{pd}	Trigger Propagation Delay (V_{CC} = + 5V)		100		ns
t_{rpw}	Minimum Reset Pulse Width (V_{trg} = + 5V)		350		ns

Notes : 1. See Figure 2
2. See Figure 4

TS555-09.TBL

TYPICAL CHARACTERISTICS

Figure 1 : Supply Current (each timer) versus Supply Voltage

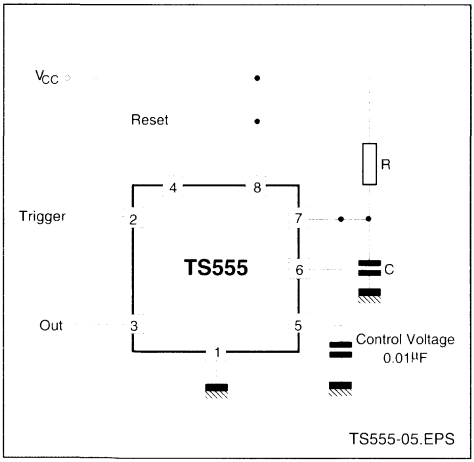


APPLICATION INFORMATION

MONOSTABLE OPERATION

In the monostable mode,the timer functions as a one-shot. Referring to figure 2 the external capacitor is initially held discharged by a transistor inside the timer.

Figure 2



The circuit triggers on a negative-going input signal when the level reaches 1/3 V_{CC}. Once triggered,the circuit remains in this state until the set time has elapsed,even if it is triggered again during this interval. The duration of the output HIGH state is given by t = 1.1 R x C.

Notice that since the charge rate and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the Reset terminal (pin 4) and the Trigger terminal (pin 2) during the timing cycle discharges the external capacitor and causes the cycle to start over. The timing cycle now starts on the positive edge of the reset pulse. During the time the reset pulse is applied, the output is driven to its LOW state.

When a negative trigger pulse is applied to pin 2, the flip-flop is set, releasing the short circuit across the external capacitor and driving the output HIGH.

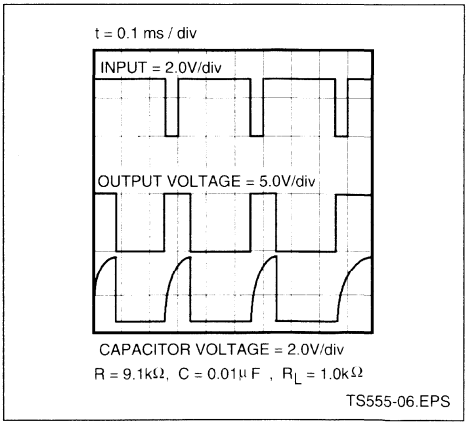
The voltage across the capacitor increases exponentially with the time constant τ = R x C.

When the voltage across the capacitor equals 2/3 V_{CC}, the comparator resets the flip-flop which then discharges the capacitor rapidly and drives the output to its LOW state.

Figure 3 shows the actual waveforms generated in this mode of operation.

When Reset is not used, it should be tied high to avoid any possible or false triggering.

Figure 3



ASTABLE OPERATION

When the circuit is connected as shown in figure 4 (pin 2 and 6 connected) it triggers itself and free runs as a multivibrator. The external capacitor charges through R_A and R_B and discharges through R_B only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

In the astable mode of operation, C charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times and therefore frequency, are independent of the supply voltage.

Figure 5 shows actual waveforms generated in this mode of operation.

The charge time (output HIGH) is given by :

$t1 = 0.693 (R_A + R_B) C$

and the discharge time (output LOW) by :

$t2 = 0.693 (R_B) C$

Thus the total period T is given by :

$T = t1 + t2 = 0.693 (R_A + 2R_B) C$

The frequency of oscillation is then :

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)C}$$

The duty cycle is given by : $D = \frac{R_B}{R_A + 2R_B}$

Figure 4

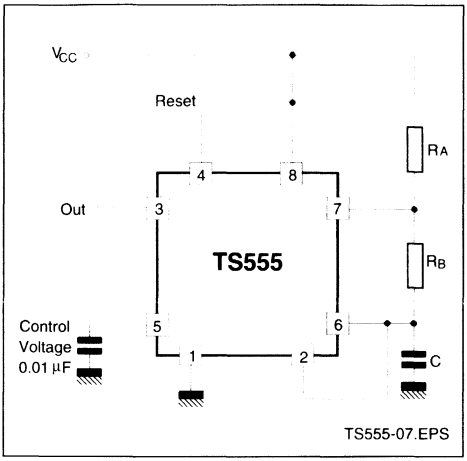
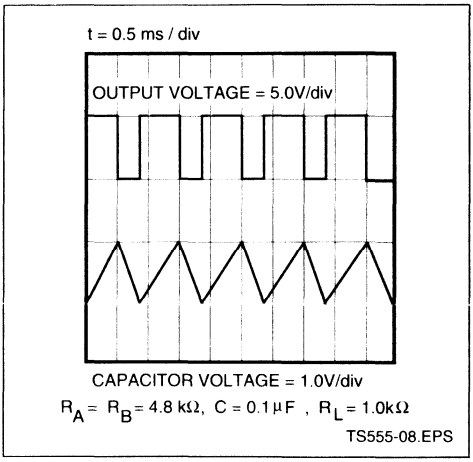
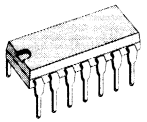


Figure 5

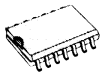


LOW POWER DUAL CMOS TIMERS

- VERY LOW POWER CONSUMPTION :
- 100µA typ at V_{CC} = 5V
- HIGH MAXIMUM ASTABLE FREQUENCY 2.7MHz
- PIN-TO-PIN AND FUNCTIONALLY COMPATIBLE WITH BIPOLAR NE555
- VOLTAGE RANGE : +2V to +18V
- HIGH OUTPUT CURRENT CAPABILITY
- SUPPLY CURRENT SPIKES REDUCED DURING OUTPUT TRANSITIONS
- HIGH INPUT IMPEDANCE : $10^{12}\ \Omega$
- OUTPUT COMPATIBLE WITH TTL,CMOS AND LOGIC MOS



N
DIP14
(Plastic Package)



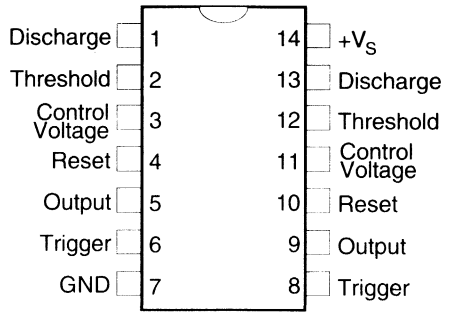
D
SO14
(Plastic Micropackage)

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS556C	0°C, +70°C	●	●
TS556I	-40, +105°C	●	●
TS556M	-55, +125°C	●	●
Examples : TS556CD , TS556IN			

TS556-01.TBL

PIN CONNECTIONS (top view)



TS556-01.EPS

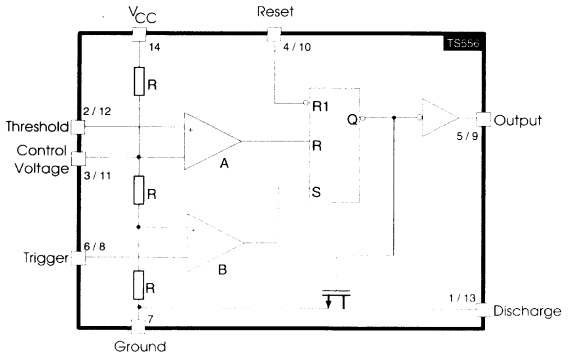
DESCRIPTION

The TS556 is a dual CMOS timer which offers very low consumption ($I_{CC(TYP)}$ TS556 = 200µA $I_{CC(TYP)}$ NE556 = 6mA) and high frequency ($f_{(max.)}$ TS556 = 2.7MHz - $f_{(max.)}$ NE556 = 0.1 MHz) Thus, either in Monostable or Astable mode, timing remains very accurate.

The TS556 provides reduced supply current spikes during output transitions, which enables the use of lower decoupling capacitors compared to those required by bipolar NE556.

Timing capacitors can also be minimized due to high input impedance ($10^{12}\ \Omega$).

BLOCK DIAGRAM



TS556-02.EPS

RESET	TRIGGER	THRESHOLD	OUTPUT
Low	x	x	Low
High	Low	x	High
High	High	High	Low
High	High	Low	Previous State

LOW ↔ Level Voltage ≤ Min voltage specified

HIGH ↔ Level Voltage ≥ Max voltage specified

X ↔ Irrelevant

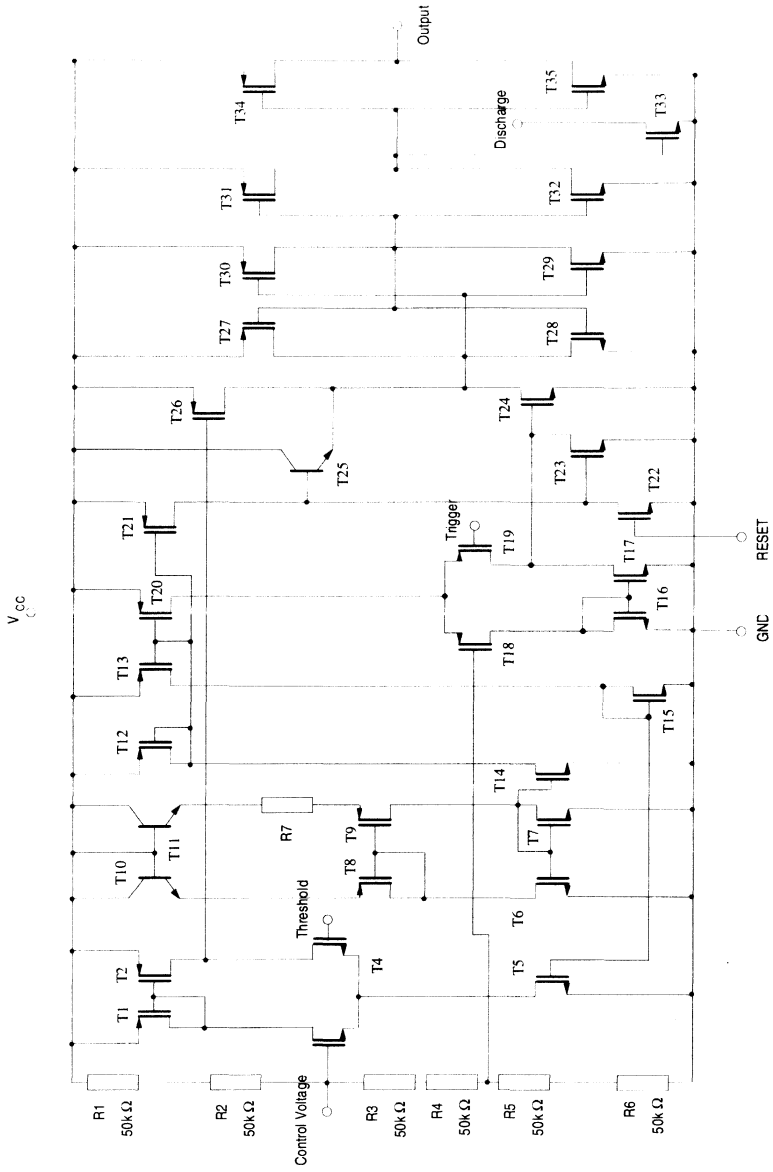
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	+18	V
T_J	Junction Temperature	+150	°C

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
T_{OPER}	Operating Temperature Range TS556C TS556I TS556M	 0 to +70 -40 to +105 -55 to +125	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C

SCHEMATIC DIAGRAM (1/2 TS556)



TS556-03.EPS

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	+2 to +16	V

STATIC ELECTRICAL CHARACTERISTICS

V_{CC} = +2V, T_{amb} = +25°C, Reset to V_{CC} (unless otherwise specified)

Symbol	Parameter	TS556C-TS556I-TS556M			Unit
		Min.	Typ	Max.	
I_{CC}	Supply Current (no load, High and Low States) T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		130	400 400	µA
V_{CL}	Control Voltage T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	1.2 1.1	1.3	1.4 1.5	V
V_{dis}	Discharge Saturation Voltage (I_{dis} = 1mA) T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		0.05	0.2 0.25	V
V_{OL}	Low Level Output Voltage (I_{sink} = 1mA) T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		0.1	0.3 0.35	V
V_{OH}	High Level Output Voltage (I_{source} = -0.3mA) T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	1.5 1.5	1.9		V
V_{trig}	Trigger Voltage T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	0.4 0.3	0.67	0.95 1.05	V
I_{trig}	Trigger Current		10		pA
I_{TH}	Threshold Current		10		pA
V_{reset}	Reset Voltage T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	0.4 0.3	1.1	1.5 2.0	V
I_{reset}	Reset Current		10		pA
i_{dis}	Discharge Pin Leakage Current		1	100	nA

STATIC ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = +5V, T_{amb} = +25°C, Reset to V_{CC} (unless otherwise specified)

Symbol	Parameter	TS556C-TS556I-TS556M			Unit
		Min.	Typ	Max.	
I_{CC}	Supply Current (no load, High and Low States) T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		220	500 500	µA
V_{CL}	Control Voltage T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	2.9 2.8	3.3	3.8 3.9	V
V_{dis}	Discharge Saturation Voltage (I_{dis} = 10mA) T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		0.2	0.3 0.35	V
V_{OL}	Low Level Output Voltage (I_{sink} = 8mA) T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		0.3	0.6 0.8	V
V_{OH}	High Level Output Voltage (I_{source} = -2mA) T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	4.4 4.4	4.6		V
V_{trig}	Trigger Voltage T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	1.36 1.26	1.67	1.96 2.06	V
I_{trig}	Trigger Current		10		pA
I_{TH}	Threshold Current		10		pA
V_{reset}	Reset Voltage T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	0.4 0.3	1.1	1.5 2.0	V
I_{reset}	Reset Current		10		pA
I_{dis}	Discharge Pin Leakage Current		1	100	nA

TS556-07.TBL

STATIC ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = +12V, T_{amb} = +25°C, Reset to V_{CC} (unless otherwise specified)

Symbol	Parameter	TS556C-TS556I-TS556M			Unit
		Min.	Typ	Max.	
I_{CC}	Supply Current (no load, High and Low States) T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		340	800 800	µA
V_{CL}	Control Voltage T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	7.4 7.3	8	8.6 8.7	V
V_{dis}	Discharge Saturation Voltage (I_{dis} = 80mA) T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		0.09	1.6 2.0	V
V_{OL}	Low Level Output Voltage (I_{sink} = 50mA) T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		1.2	2 2.8	V
V_{OH}	High Level Output Voltage (I_{source} = -10mA) T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	10.5 10.5	11		V
V_{trig}	Trigger Voltage T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	3.2 3.1	4	4.8 4.9	V
I_{trig}	Trigger Current		10		pA
I_{TH}	Threshold Current		10		pA
V_{reset}	Reset Voltage T_{amb} = + 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	0.4 0.3	1.1	1.5 2.0	V
I_{reset}	Reset Current		10		pA
I_{dis}	Discharge Pin Leakage Current		1	100	nA

TS556-08.TBL

DYNAMIC ELECTRICAL CHARACTERISTICS

T_{amb} = +25°C, Reset to V_{CC} (unless otherwise specified)

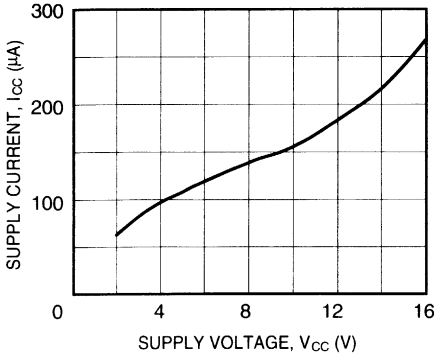
Symbol	Parameter	TS556C-TS556I-TS556M			Unit
		Min	Typ	Max	
	Timing Accuracy (Monostable) - (note 1) R = 10kΩ , C = 0.1µF				%
	V_{CC} = + 2V		1		
	V_{CC} = + 5V		2		
	V_{CC} = +12V		4		
	Timing Shift with supply voltage variations (Monostable) R = 10kΩ , C = 0.1µF, V_{CC} = + 5V +/-1V		0.38		%/V
	Timing Shift with temperature $T_{min.} \leq T_{amb} \leq T_{max.}$, V_{CC} = + 5V		75		ppm/°C
f_{max}	Maximum astable frequency R_A = 470Ω , R_B = 200Ω, C = 200pF , V_{CC} = + 5V		2.7		MHz
	Astable frequency accuracy - (note 2) $R_A = R_B$ = 1kΩ to 100kΩ, C = 0.1µF				%
	V_{CC} = + 5V		3		
	V_{CC} = + 12V		3		
	Timing Shift with supply voltage variations (Astable mode) $R_A = R_B$ = 1kΩ to 100kΩ, C = 0.1µF, V_{CC} = 5 to+ 12V		0.1		%/V
t_r	Output Rise Time (V_{CC} = + 5V , C_{load} = 10pF)		25		ns
t_f	Output Fall Time (V_{CC} = + 5V , C_{load} = 10pF)		20	-	ns
t_{pd}	Trigger Propagation Delay (V_{CC} = + 5V)		100		ns
t_{rpw}	Minimum Reset Pulse Width (V_{trg} = + 5V)		350		ns

TS556-09.TBL

Notes : 1. See Figure 2
2. See Figure 4

TYPICAL CHARACTERISTICS

Figure 1 : Supply Current (each timer) versus Supply Voltage



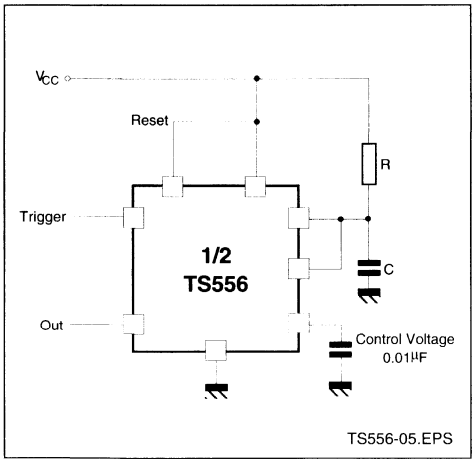
TS556-04.EPS

APPLICATION INFORMATION

MONOSTABLE OPERATION

In the monostable mode,the timer functions as a one-shot. Referring to figure 2 the external capacitor is initially held discharged by a transistor inside the timer.

Figure 2



TS556-05.EPS

The circuit triggers on a negative-going input signal when the level reaches 1/3 V_{CC}. Once triggered,the circuit remains in this state until the set time has elapsed,even if it is triggered again during this interval. The duration of the output HIGH state is given by t = 1.1 R x C.

Notice that since the charge rate and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the Reset terminal (pin 4 or 10) and the Trigger terminal (pin 2 or 8) during the timing cycle discharges the external capacitor and causes the cycle to start over. The timing cycle now starts on the positive edge of the reset pulse. During the time the reset pulse is applied, the output is driven to its LOW state.

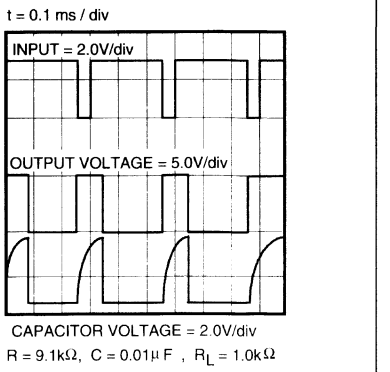
When a negative trigger pulse is applied to the trigger terminal, the flip-flop is set, releasing the short circuit across the external capacitor and driving the output HIGH. The voltage across the capacitor increases exponentially with the time constant τ = R x C.

When the voltage across the capacitor equals 2/3 V_{CC}, the comparator resets the flip-flop which then discharges the capacitor rapidly and drives the output to its LOW state.

Figure 3 shows the actual waveforms generated in this mode of operation.

When Reset is not used, it should be tied high to avoid any possible or false triggering.

Figure 3



TS556-06.EPS

ASTABLE OPERATION

When the circuit is connected as shown in figure 4 it triggers itself and free runs as a multivibrator. The external capacitor charges through R_A and R_B and discharges through R_B only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

In the astable mode of operation, C charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times and therefore frequency, are independent of the supply voltage.

Figure 5 shows actual waveforms generated in this mode of operation.

The charge time (output HIGH) is given by :

$t1 = 0.693 (R_A + R_B) C$

and the discharge time (output LOW) by :

$t2 = 0.693 (R_B) C$

Thus the total period T is given by :

$T = t1 + t2 = 0.693 (R_A + 2R_B) C$

The frequency of oscillation is then :

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)C}$$

The duty cycle is given by : $D = \frac{R_B}{R_A + 2R_B}$

Figure 4

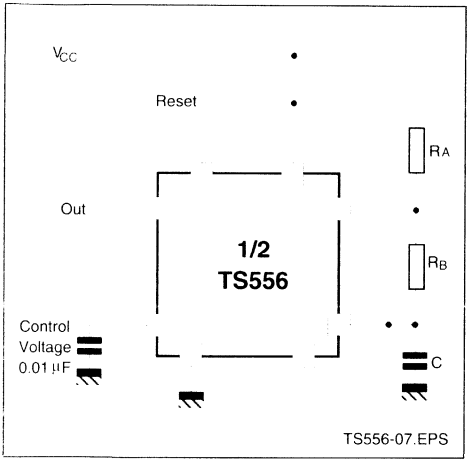
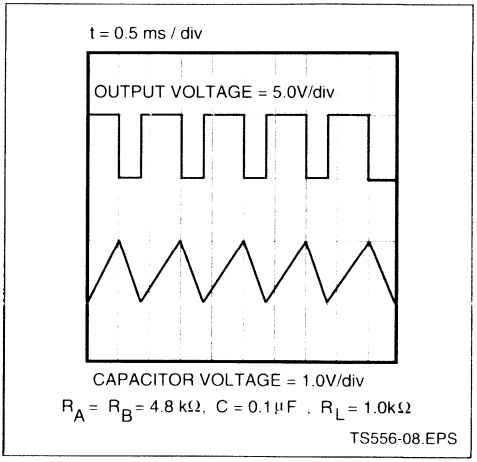


Figure 5



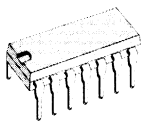
SGS-THOMSON MICROELECTRONICS

TS902

INPUT/OUTPUT **RAIL-TO-RAIL** DUAL CMOS OPERATIONAL AMPLIFIERS (WITH STANDBY POSITION)

TENTATIVE DATA

- RAIL TO RAIL INPUT AND OUTPUT VOLTAGE RANGE
- SINGLE POWER SUPPLY OPERATION FROM 2.7V TO 16V
- GAIN BANDWIDTH PRODUCT OF 1MHz
- LOW SUPPLY CURRENT : 350µA/Ampli
- EXTREMELY LOW INPUT BIAS CURRENT 1pA TYP
- LOW IMPEDANCE 100Ω DRIVING CAPABILITY
- SLEW RATE : 1V/µs
- LOW NOISE : $40nV/\sqrt{Hz}$
- ESD INTERNAL PROTECTION DIODES
- LOW INPUT OFFSET VOLTAGE : 1.5mV max.
- STANDBY POSITION : REDUCED CONSUMPTION (800nA/amp) AND TRISTATE OUTPUTS



N
DIP14
(Plastic Package)

D
SO
(Plastic Micropackage)

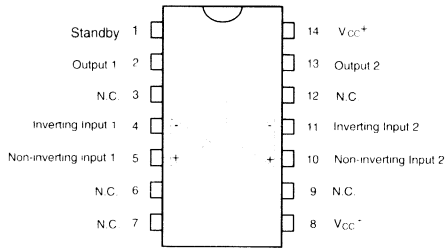
ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS902C/AC/BC	0, +70°C	•	•
TS902I/AI/BI	-40, +105°C	•	•
TS902M/AM/BM	-55, +125°C	•	•

902-01.TBL

PIN CONNECTIONS (top view)

DIP14

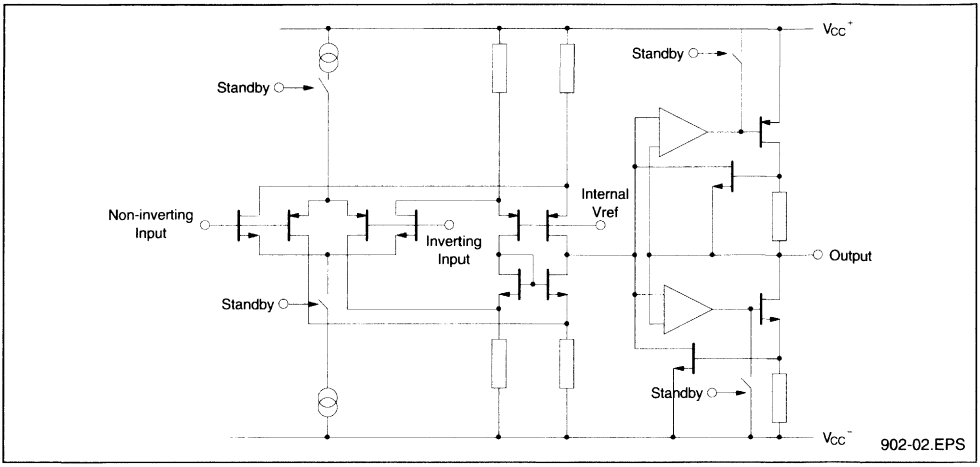


902-01.EPS

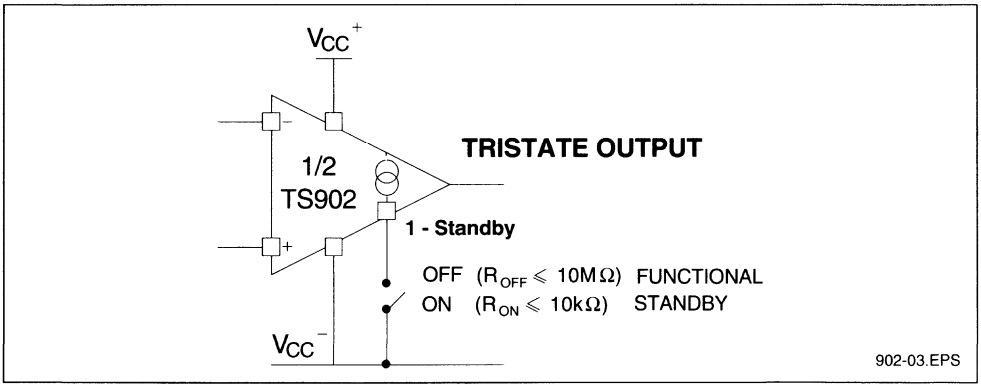
DESCRIPTION

The TS902 is a Rail-to-Rail dual CMOS operational amplifier designed to operate with single or dual supply voltage.
The input voltage range V_{icm} includes the two supply rails V_{CC}^+ and V_{CC}^-.
The output reaches (V_{CC}^- +50mV ; V_{CC}^+ -50mV) with R_L = 10kΩ and (V_{CC}^- +650mV ; V_{CC}^+ -650mV) with R_L = 600Ω.
This product offers a broad supply voltage operating range from 2.7V to 16V and a supply current of only 350µA/amp. (V_{CC} = 10V).
Source and sink output capability is typically 80mA (at V_{CC} = ±5V), fixed by an internal limitation circuit.
The TS902 can be put in STANDBY position by connecting the pin 1 to V_{CC}^- (only 800nA/amp and tristate outputs).

SCHEMATIC DIAGRAM (1/2 TS902)



STANDBY POSITION



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage - (note 1)	18	V
V_{id}	Differential Input Voltage - (note 2)	±18	V
V_i	Input Voltage - (note 3)	-0.3 to 18	V
I_{in}	Current on Inputs	±50	mA
I_o	Current on Outputs	±130	mA
T_{oper}	Operating Ambient Temperature Range TS902C/AC/BC TS902I/AI/BI TS902M/AM/BM	 0 to +70 -40 to +105 -55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Notes :
1. All voltage values, except differential voltage are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of input and output voltages must never exceed V_{CC}^+ +0.3V.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage	2.7 to 16	V
V_{icm}	Common Mode Input Voltage Range	V_{CC}^- -0.2 to V_{CC}^+ +0.2	V

ELECTRICAL CHARACTERISTICS

V_{CC}^+ = 10V, V_{CC}^- = 0V, pin 1 not connected, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage	TS902 TS902A TS902B			12 5 1.5	mV
I_{io}	Input Offset Current - (note 1)			1	100	pA
I_{ib}	Input Bias Current - (note 1)			1	150	pA
I_{CC}	Supply Current (per amplifier) A_V = 1, no load			350	450	µA
V_{icm}	Input Common Mode Voltage Range			-0.2 to +10.2		V
CMR	Common Mode Rejection Ratio V_{ic} = 3 to 7V, V_o = 5V V_{ic} = 0 to 10V, V_o = 5V			100 85		dB
SVR	Supply Voltage Rejection Ratio V_{CC}^+ = 6 to 10V, V_O = 5V			70		dB
A_{vd}	Large Signal Voltage Gain R_L = 10kΩ		10	20		V/mV
V_{OH}	High Level Output Voltage V_{id} = 100mV	R_L = 100kΩ R_L = 10kΩ R_L = 600Ω R_L = 100Ω	9.95 9.85 9.2	 9.95 9.35 8		V
V_{OL}	Low Level Output Voltage V_{id} = -100mV	R_L = 100kΩ R_L = 10kΩ R_L = 600Ω R_L = 100Ω		 50 650 2100	 50 150 800	mV
I_o	Output Short Circuit Current V_{id} = ±100mV	Source (V_o = 0V) Sink (V_o = V_{CC}^+)		90 80		mA
GBP	Gain Bandwidth Product A_{VCL} = 100, R_L = 10kΩ, C_L = 100pF, f = 100kHz			1		MHz
SR	Slew Rate A_{VCL} = 1, R_L = 10kΩ, C_L = 100pF, V_{in} = 2.5V to 7.5V			1		V/µs
Øm	Phase Margin			30		Degrees
e_n	Equivalent Input Noise Voltage (R_s = 100Ω, f = 1kHz)			40		$\frac{nV}{\sqrt{Hz}}$
THD	Total Harmonic Distortion A_{VCL} = 1, R_L = 10kΩ, C_L = 100pF, V_i = 4.75V to 5.25V			0.024		%
C_{in}	Input Capacitance			1.5		pF
V_{O1}/V_{O2}	Channel Separation (f = 1kHz)			120		dB
$I_{CC\ STB}$	Supply Current (per amplifier) in standby position (pin 1 connected to V_{CC}^-)			800		nA

Note 1 : Maximum values including unavoidable inaccuracies of the industrial test.

ELECTRICAL CHARACTERISTICS

$V_{CC}^+ = 3V$, $V_{CC}^- = 0V$, pin 1 not connected, $T_{amb} = 25°C$ (unless otherwise specified)

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage	TS912 TS912A TS912B			12 5 1.5	mV
I_{io}	Input Offset Current - (note 1)			1	100	pA
I_{ib}	Input Bias Current - (note 1)			1	150	pA
I_{CC}	Supply Current (per amplifier) $A_V = 1$, no load			170	230	µA
V_{icm}	Input Common Mode Voltage Range			-0.2 to +3.2		V
CMR	Common Mode Rejection Ratio $V_{ic} = 0$ to 3V, $V_o = 1.5V$			60		dB
SVR	Supply Voltage Rejection Ratio $V_{CC}^+ = 2.7$ to 3.3V, $V_O = 1.5V$			60		dB
A_{vd}	Large Signal Voltage Gain $R_L = 10k\Omega$		3	5		V/mV
V_{OH}	High Level Output Voltage $V_{id} = 100mV$	$R_L = 100k\Omega$ $R_L = 10k\Omega$ $R_L = 600\Omega$ $R_L = 100\Omega$	2.95 2.9 2.2	 2.96 2.6 2		V
V_{OL}	Low Level Output Voltage $V_{id} = -100mV$	$R_L = 100k\Omega$ $R_L = 10k\Omega$ $R_L = 600\Omega$ $R_L = 100\Omega$		 50 350 900	50 100 600	mV
I_o	Output Short Circuit Current $V_{id} = \pm 100mV$	Source ($V_o = 0V$) Sink ($V_o = V_{CC}^+$)		30 30		mA
GBP	Gain Bandwidth Product $A_{VCL} = 100$, $R_L = 10k\Omega$, $C_L = 100pF$, f = 100kHz			0.6		MHz
SR	Slew Rate $A_{VCL} = 1$, $R_L = 10k\Omega$, $C_L = 100pF$, $V_{in} = 2.5V$ to 7.5V			0.4		V/µs
Øm	Phase Margin			12		Degrees
$I_{CC\ STB}$	Supply Current (per amplifier) in standby position (pin 1 connected to V_{CC}^-)			700		nA

902-05.TBL

Note 1 : Maximum values including unavoidable inaccuracies of the industrial test.

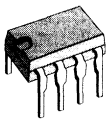
SGS-THOMSON MICROELECTRONICS

TS912

INPUT/OUTPUT **RAIL-TO-RAIL** DUAL CMOS OPERATIONAL AMPLIFIERS

TENTATIVE DATA

- RAIL TO RAIL INPUT AND OUTPUT VOLTAGE RANGE
- SINGLE POWER SUPPLY OPERATION FROM 2.7V TO 16V
- GAIN BANDWIDTH PRODUCT OF 1MHz
- LOW SUPPLY CURRENT : 350µA/Ampli
- EXTREMELY LOW INPUT BIAS CURRENT 1pA TYP
- LOW IMPEDANCE 100Ω DRIVING CAPABILITY
- SLEW RATE : 1V/µs
- LOW NOISE : 40nV/$\sqrt{Hz}$
- ESD INTERNAL PROTECTION DIODES
- LOW INPUT OFFSET VOLTAGE : 1.5mV max.



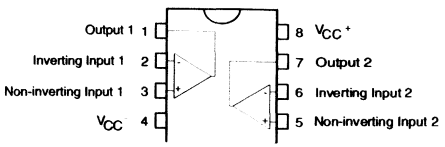
N
DIP8
(Plastic Package)

ORDER CODES

Part Number	Temperature Range	Package
		N
TS912C/AC/BC	0, +70°C	•
TS912I/AI/BI	-40, +105°C	•
TS912M/AM/BM	-55, +125°C	•

912-01.TBL

PIN CONNECTIONS (top view)

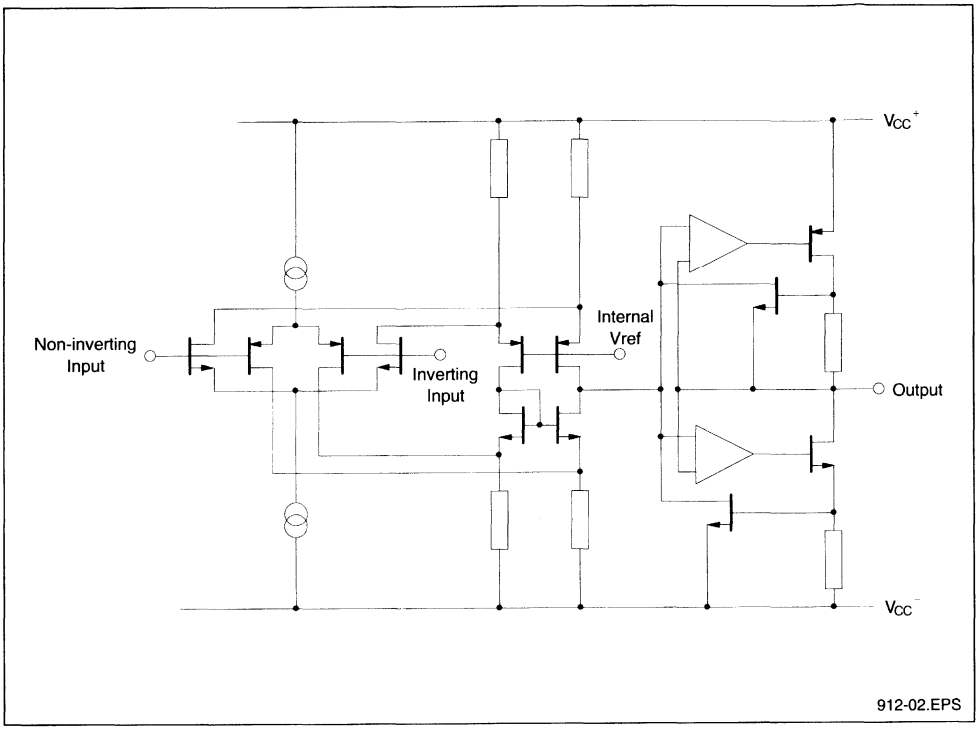


912-01.EPS

DESCRIPTION

The TS912 is a Rail-to-Rail dual CMOS operational amplifier designed to operate with single or dual supply voltage.
The input voltage range V_{icm} includes the two supply rails V_{CC}^+ and V_{CC}^-.
The output reaches (V_{CC}^- +50mV ; V_{CC}^+ -50mV) with R_L = 10kΩ and (V_{CC}^- +650mV ; V_{CC}^+ -650mV) with R_L = 600Ω.
This product offers a broad supply voltage operating range from 2.7V to 16V and a supply current of only 350µA/amp. (V_{CC} = 10V).
Source and sink output capability is typically 80mA (at V_{CC} = ±5V), fixed by an internal limitation circuit.

SCHEMATIC DIAGRAM (1/2 TS912)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage - (note 1)	18	V
V_{id}	Differential Input Voltage - (note 2)	±18	V
V_i	Input Voltage - (note 3)	-0.3 to 18	V
I_{in}	Current on Inputs	±50	mA
I_o	Current on Outputs	±130	mA
T_{oper}	Operating Free Air Temperature Range TS912C/AC/BC TS912I/AI/BI TS912M/AM/BM	 0 to +70 -40 to +105 -55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

912-02.TBL

Notes : 1. All voltage values, except differential voltage are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of input and output voltages must never exceed V_{CC}^+ +0.3V.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage	2.7 to 16	V
V_{icm}	Common Mode Input Voltage Range	V_{CC}^- -0.2 to V_{CC}^++0.2	V

912-03.TBL

ELECTRICAL CHARACTERISTICS

$V_{CC}^+ = 10V$, $V_{CC}^- = 0V$, $T_{amb} = 25^oC$ (unless otherwise specified)

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage					mV
		TS912			12	
		TS912A			5	
		TS912B			1.5	
I_{io}	Input Offset Current - (note 1)			1	100	pA
I_{ib}	Input Bias Current - (note 1)			1	150	pA
I_{CC}	Supply Current (per amplifier)					µA
	A_V = 1, no load			350	450	
V_{icm}	Input Common Mode Voltage Range			-0.2 to +10.2		V
CMR	Common Mode Rejection Ratio					dB
	V_{ic} = 3 to 7V, V_o = 5V			100		
	V_{ic} = 0 to 10V, V_o = 5V			85		
SVR	Supply Voltage Rejection Ratio					dB
	V_{CC}^+ = 6 to 10V, V_O = 5V			70		
A_{vd}	Large Signal Voltage Gain					V/mV
	R_L = 10kΩ		10	40		
V_{OH}	High Level Output Voltage					V
	V_{id} = 100mV	R_L = 100kΩ	9.95			
		R_L = 10kΩ	9.85	9.95		
		R_L = 600Ω	9.2	9.35		
		R_L = 100Ω		8		
V_{OL}	Low Level Output Voltage					mV
	V_{id} = -100mV	R_L = 100kΩ			50	
		R_L = 10kΩ		50	150	
		R_L = 600Ω		650	800	
		R_L = 100Ω		2100		
I_o	Output Short Circuit Current					mA
	V_{id} = ±100mV	Source (V_o = 0V)		90		
		Sink ($V_o = V_{CC}^+$)		80		
GBP	Gain Bandwidth Product					MHz
	A_{VCL} = 100, R_L = 10kΩ, C_L = 100pF, f = 100kHz			1		
SR	Slew Rate					V/µs
	A_{VCL} = 1, R_L = 10kΩ, C_L = 100pF, V_{in} = 2.5V to 7.5V			1		
∅m	Phase Margin			30		Degrees
e_n	Equivalent Input Noise Voltage					nV
	(R_s = 100Ω, f = 1kHz)			40		√Hz
THD	Total Harmonic Distortion					%
	A_{VCL} = 1, R_L = 10kΩ, C_L = 100pF, V_i = 4.75V to 5.25V			0.024		
C_{in}	Input Capacitance			1.5		pF
V_{O1}/V_{O2}	Channel Separation (f = 1kHz)			120		dB

912-04.TBL

Note 1 : Maximum values including unavoidable inaccuracies of the industrial test.

ELECTRICAL CHARACTERISTICS

$V_{CC}^+ = 3V$, $V_{CC}^- = 0V$, $T_{amb} = 25°C$ (unless otherwise specified)

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage	TS912 TS912A TS912B			12 5 1.5	mV
I_{io}	Input Offset Current - (note 1)			1	100	pA
I_{ib}	Input Bias Current - (note 1)			1	150	pA
I_{CC}	Supply Current (per amplifier) $A_V = 1$, no load			170	230	µA
V_{icm}	Input Common Mode Voltage Range			-0.2 to +3.2		V
CMR	Common Mode Rejection Ratio $V_{ic} = 0$ to 3V, $V_o = 1.5V$			60		dB
SVR	Supply Voltage Rejection Ratio $V_{CC}^+ = 2.7$ to 3.3V, $V_O = 1.5V$			60		dB
A_{vd}	Large Signal Voltage Gain $R_L = 10k\Omega$		3	5		V/mV
V_{OH}	High Level Output Voltage $V_{id} = 100mV$	$R_L = 100k\Omega$ $R_L = 10k\Omega$ $R_L = 600\Omega$ $R_L = 100\Omega$	2.95 2.9 2.2	 2.96 2.6 2		V
V_{OL}	Low Level Output Voltage $V_{id} = -100mV$	$R_L = 100k\Omega$ $R_L = 10k\Omega$ $R_L = 600\Omega$ $R_L = 100\Omega$		 50 350 900	50 100 600	mV
I_o	Output Short Circuit Current $V_{id} = \pm 100mV$	Source ($V_o = 0V$) Sink ($V_o = V_{CC}^+$)		30 30		mA
GBP	Gain Bandwidth Product $A_{VCL} = 100$, $R_L = 10k\Omega$, $C_L = 100pF$, f = 100kHz			0.6		MHz
SR	Slew Rate $A_{VCL} = 1$, $R_L = 10k\Omega$, $C_L = 100pF$, $V_{in} = 2.5V$ to 7.5V			0.4		V/µs
Øm	Phase Margin			12		Degrees

912-05.TBL

Note 1 : Maximum values including unavoidable inaccuracies of the industial test.

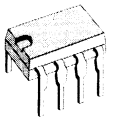
SGS-THOMSON MICROELECTRONICS

TSH150

WIDE BANDWIDTH AND BIPOLAR INPUTS SINGLE OPERATIONAL AMPLIFIERS

PRELIMINARY DATA

- LOW DISTORTION
- GAIN BANDWIDTH PRODUCT : 150MHz
- UNITY GAIN STABLE
- SLEW RATE : 190V/µs
- VERY FAST SETTLING TIME : 20ns (0.1%)



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

DESCRIPTION:

The TSH150 is a wideband monolithic operational amplifier, internally compensated for unity-gain stability.

Low noise and low distortion, wide bandwidth and high linearity make this amplifier suitable for RF and video applications. Short circuit protection is provided by an internal current-limiting circuit.

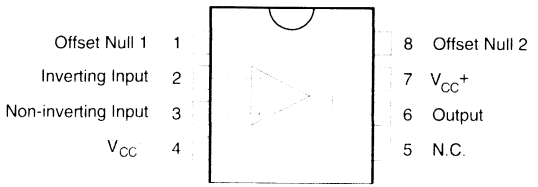
The THS150 has internal electrostatic discharge (ESD) protection circuits and fulfills MILSTD833C-Class2.

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TSH150C	0°C, 70°C	•	•
TSH150I	-40°C, 105°C	•	•
TSH150M	-55°C, 125°C	•	•

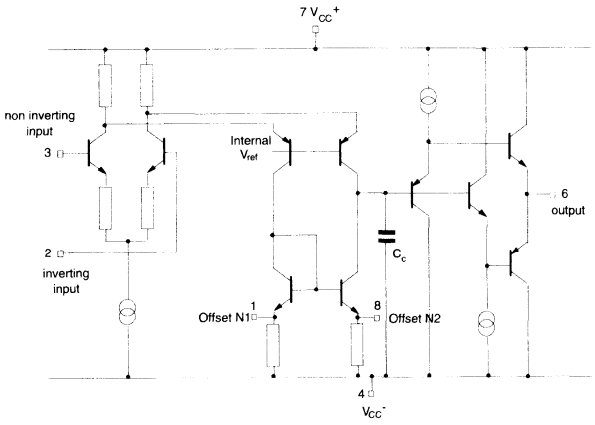
150-01.TBL

PIN CONNECTIONS (top view)



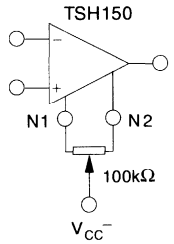
150-01.EPS

SCHEMATIC DIAGRAM



150-02.EPS

INPUT OFFSET VOLTAGE NULL CIRCUIT



150-03.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		±7	V
V_{id}	Differential Input Voltage		±5	V
V_i	Input Voltage Range		±5	V
I_{in}	Current On Inputs Current On Offset Null Pins		±50 ±20	mA
T_{oper}	Operating Free-Air Temperature Range	TSH150C TSH150I TSH150M	0 to +70 -40 to +105 -55 to +125	°C
T_{stg}	Storage Temperature Range		-65 to 150	°C

150-02.TBL

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	±3 to ±6	V
V_{ic}	Common Mode Input Voltage Range	V_{CC}^- +2 to V_{CC}^+ -1	V

150-03.TBL

ELECTRICAL CHARACTERISTICS

$V_{CC} = \pm 5V$, $T_{amb} = 25°C$ (unless otherwise specified)

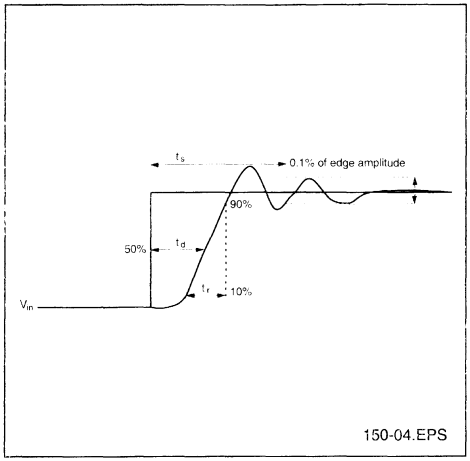
Symbol	Parameter		TSH150C, I, M			Unit
			Min.	Typ.	Max.	
V_{io}	Input Offset Voltage			0.15	5	mV
DV_{io}	Input Offset Voltage Drift $T_{min} \le T_{amb} \le T_{max}$			10		µV/°C
I_{ib}	Input Bias Current			5	30	µA
I_{io}	Input Offset Current			0.1	2	µA
I_{CC}	Supply Current, no load					mA
		$V_{CC} = \pm 5V$		23	30	
		$V_{CC} = \pm 3V$		21	28	
		$V_{CC} = \pm 6V$		25	40	
A_{vd}	Large Signal Voltage Gain $V_o = \pm 2.5V$					V/V
		$R_L = \infty$	800	1300		
		$R_L = 100\Omega$	300	850		
		$R_L = 50\Omega$	200	650		
V_{icm}	Input Common Mode Voltage Range		-3 to +4	-3.5 to +4.5		V
CMR	Common Mode Rejection Ratio	$V_{ic} = V_{icm\ min.}$	60	100		dB
SVR	Supply Voltage Rejection Ratio $V_{CC} = \pm 5V$ to $\pm 3V$		50	70		dB
V_o	Output Voltage	$R_L = 100\Omega$	± 3	+3.5 -3.7		V
		$R_L = 50\Omega$	± 2.8	+3.3 -3.5		
I_o	Output Short Circuit Current $V_{id} = \pm 1V$, $V_o = 0V$		±50	±100		mA
GBP	Gain Bandwidth Product $A_V = 100$, $R_L = 100\Omega$, $C_L = 15pF$, f = 7.5MHz			150		MHz
SR	Slew Rate $V_{in} = \pm 2V$, $A_v = 1$, $R_L = 100\Omega$, $C_L = 15pF$		100	190		V/µs
e_n	Equivalent Input Voltage Noise $R_S = 10\Omega$					$\frac{nV}{\sqrt{Hz}}$
		f = 1kHz		6.5		
		f = 10kHz		6.3		
		f = 100kHz		6.2		
		f = 1MHz		6.1		
	$R_S = 50\Omega$					
		fo = 1kHz		7		
		fo = 10kHz		6.5		
		fo = 100kHz		6.2		
		fo = 1MHz		5.5		
K_{ov}	Overshoot $V_{in} = \pm 2V$, $A_v = 1$, $R_L = 100\Omega$, $C_L = 15pF$			10		%
t_s	Settling Time 0.1% - (note 1) $V_{in} = \pm 1V$, $A_v = -1$			20		ns
t_r, t_f	Rise and Fall Time - (note 1) $V_{in} = \pm 100mV$, $A_V = 2$			3.5		ns
t_d	Delay Time - (note 1) $V_{in} = \pm 100mV$, $A_V = 2$			2.5		ns
Øm	Phase Margin $A_v = 2$, $R_L = 100\Omega$, $C_L = 15pF$			42		Degrees
THD	Total Harmonic Distortion $A_v = 10$, f = 1KHz, $V_o = \pm 2.5V$, no load			0.02		%
FPB	Full Power Bandwidth - (note 2) $V_o = 5Vpp$, $R_L = 100\Omega$			12		MHz
	$V_o = 2Vpp$, $R_L = 100\Omega$			30		

150-03.TBL

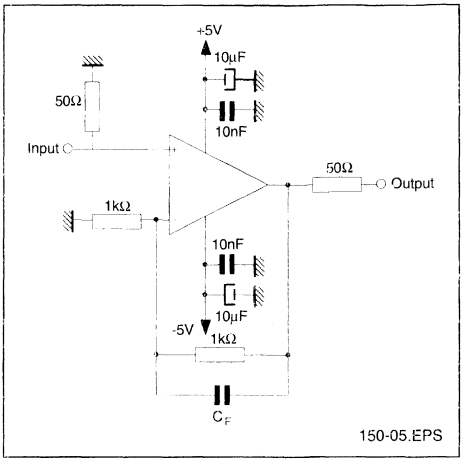
Note 1 : See test waveform figure

Note 2 : Full power bandwidth = $\frac{SR}{\Pi V_{opp}}$

TEST WAVEFORM



EVALUATION CIRCUIT



PRINTED CIRCUIT LAYOUT

As for any high frequency device, a few rules must be observed when designing the PCB to get the best performance from your high speed op amp.

From the most to the least important points :

- Each power supply lead has to be bypassed to ground with a 1nF ceramic capacitor very close to the device and a 10uF tantalum capacitor.
- To provide low inductance and low resistance common return, use a ground plane or common point return for power and signal.
- All leads must be wide and as short as possible especially for op amp inputs. This is in order to decrease parasitic capacitor and inductance.
- Use small resistor values to decrease time constant with parasitic capacitor. Be avare on TSH150 device of the I_{io} error and input noise currents with high feedback resistor values.
- Choose component sizes as small as possible (SMD).
- On output, decrease capacitor load so as to avoid circuit stability being degraded which may cause oscillation. You can also add a serial resistor in order to minimise its influence.
- One can add in parallel with feedback resistor a few pF ceramic capacitor C_F adjusted to optimize the settling time.

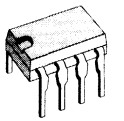
SGS-THOMSON MICROELECTRONICS

TSH151

WIDE BANDWIDTH AND MOS INPUTS SINGLE OPERATIONAL AMPLIFIERS

PRELIMINARY DATA

- LOW DISTORTION
- GAIN BANDWIDTH PRODUCT : 150MHz
- UNITY GAIN STABLE
- SLEW RATE : 200V/µs
- VERY FAST SETTLING TIME : 70ns (0.1%)
- VERY HIGH INPUT IMPEDANCE



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

DESCRIPTION:

The TSH151 is a wideband monolithic operational amplifier, internally compensated for unity-gain stability.

The TSH151 features extremely high input impedance (typically greater than $10^{12}\Omega$) allowing direct interfacing with high impedance sources.

Low distortion, wide bandwidth and high linearity make this amplifier suitable for RF and video applications. Short circuit protection is provided by an internal current-limiting circuit.

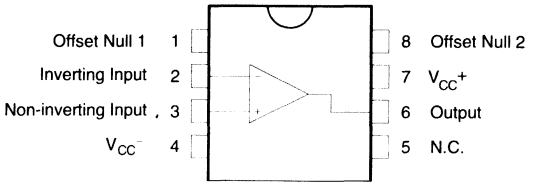
The THS151 has internal electrostatic discharge (ESD) protection circuits and fulfills MILSTD833C-Class2.

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TSH151C	0°C, 70°C	•	•
TSH151I	-40°C, 105°C	•	•
TSH151M	-55°C, 125°C	•	•

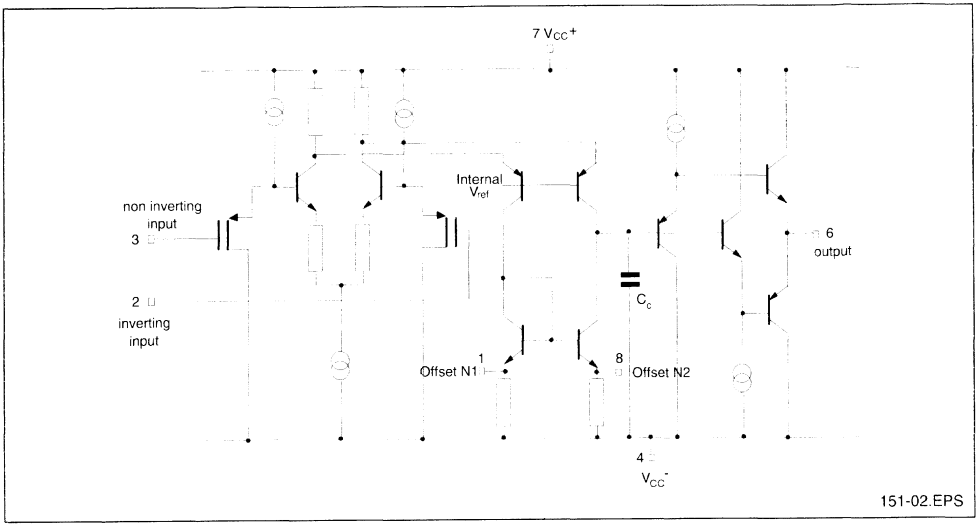
151-01.TBL

PIN CONNECTIONS (top view)

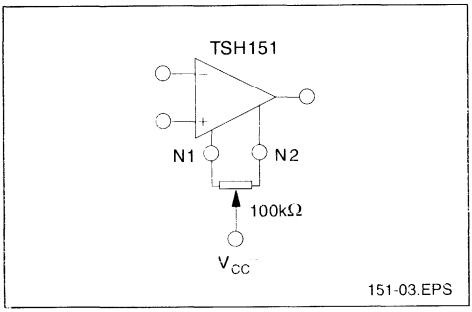


151-01.EPS

SCHEMATIC DIAGRAM



INPUT OFFSET VOLTAGE NULL CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		±7	V
V_{id}	Differential Input Voltage		±5	V
V_i	Input Voltage Range		±5	V
i_{in}	Current On Offset Null Pins		±20	mA
T_{oper}	Operating Free-Air Temperature Range	TSH151C TSH151I TSH151M	0°C, 70°C -40°C, 105°C -55°C, 125°C	°C

151-09.TBL

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	±3 to ±6	V
V_{ic}	Common Mode Input Voltage Range	V_{CC}^- to V_{CC}^+ -3	V

151-03.TBL

ELECTRICAL CHARACTERISTICS

$V_{CC} = \pm 5V$, $T_{amb} = 25^{o}C$ (unless otherwise specified)

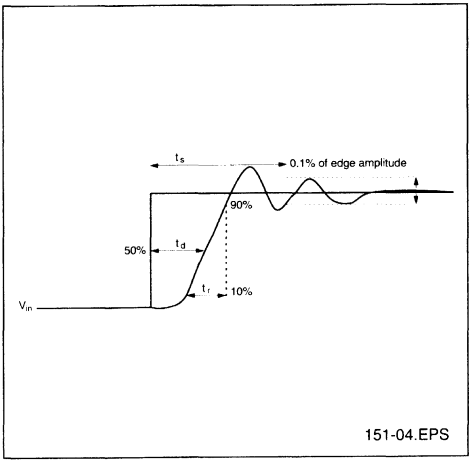
Symbol	Parameter		TSH151C, I, M			Unit
			Min.	Typ.	Max.	
V_{io}	Input Offset Voltage			0.15	10	mV
DV_{io}	Input Offset Voltage Drift $T_{min} \le T_{amb} \le T_{max}$			10		µV/°C
I_{ib}	Input Bias Current			25	300	pA
I_{io}	Input Offset Current			5	40	pA
I_{CC}	Supply Current, no load					mA
		$V_{CC} = \pm 5V$		23	30	
		$V_{CC} = \pm 3V$		21	28	
		$V_{CC} = \pm 6V$		25	40	
A_{vd}	Large Signal Voltage Gain $V_o = \pm 2.5V$					V/V
		$R_L = \infty$	800	1300		
		$R_L = 100\Omega$	300	850		
		$R_L = 50\Omega$	200	650		
V_{icm}	Input Common Mode Voltage Range		-5 to +2	-5.5 to +2.5		V
CMR	Common Mode Rejection Ratio	$V_{ic} = V_{icm\ min.}$	60	100		dB
SVR	Supply Voltage Rejection Ratio $V_{CC} = \pm 5V$ to $\pm 3V$		50	70		dB
V_o	Output Voltage	$R_L = 100\Omega$	± 3	+3.5 -3.7		V
		$R_L = 50\Omega$	± 2.8	+3.3 -3.5		
I_o	Output Short Circuit Current $V_{id} = \pm 1V$, $V_o = 0V$		±50	±100		mA
GBP	Gain Bandwidth Product $A_V = 100$, $R_L = 100\Omega$, $C_L = 15pF$, f = 7.5MHz			150		MHz
SR	Slew Rate $V_{in} = \pm 2V$, $A_v = 1$, $R_L = 100\Omega$, $C_L = 15pF$		100	200		V/µs
e_n	Equivalent Input Voltage Noise $R_S = 10\Omega$					$\frac{nV}{\sqrt{Hz}}$
		f = 1kHz		19.5		
		f = 10kHz		18		
		f = 100kHz		18		
		f = 1MHz		18		
	$R_S = 50\Omega$					
		fo = 1kHz		20		
		fo = 10kHz		18.2		
		fo = 100kHz		18.1		
		fo = 1MHz		18.2		
K_{ov}	Overshoot $V_{in} = \pm 2V$, $A_v = 1$, $R_L = 100\Omega$, $C_L = 15pF$			10		%
t_s	Settling Time 0.1% - (note 1) $V_{in} = \pm 1V$, $A_v = -1$			70		ns
t_r, t_f	Rise and Fall Time - (note 1) $V_{in} = \pm 100mV$, $A_V = 2$			5		ns
t_d	Delay Time - (note 1) $V_{in} = \pm 100mV$, $A_V = 2$			4		ns
∅m	Phase Margin $A_v = 2$, $R_L = 100\Omega$, $C_L = 15pF$			42		Degrees
THD	Total Harmonic Distortion $A_v = 10$, f = 1KHz, $V_o = \pm 2.5V$, no load			0.02		%
FPB	Full Power Bandwidth - (note 2) $V_o = 5Vpp$, $R_L = 100\Omega$ $V_o = 2Vpp$, $R_L = 100\Omega$			13 32		MHz

151-04.TBL

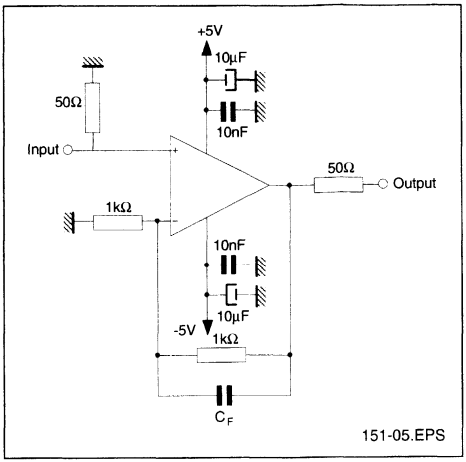
Note 1 : See test waveform figure

Note 2 : Full power bandwidth = $\frac{SR}{\Pi\ V_{opp}}$

TEST WAVEFORM



EVALUATION CIRCUIT



PRINTED CIRCUIT LAYOUT

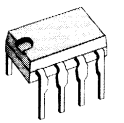
As for any high frequency device, a few rules must be observed when designing the PCB to get the best performance from your high speed op amp.

From the most to the least important points :

- Each power supply lead has to be bypassed to ground with a 1nF ceramic capacitor very close to the device and a 10uF tantalum capacitor.
- To provide low inductance and low resistance common return, use a ground plane or common point return for power and signal.
- All leads must be wide and as short as possible especially for op amp inputs. This is in order to decrease parasitic capacitor and inductance.
- Use small resistor values to decrease time constant with parasitic capacitor.
- Choose component sizes as small as possible (SMD).
- On output, decrease capacitor load so as to avoid circuit stability being degraded which may cause oscillation. One can also add a serial resistor in order to minimise its influence.
- One can add in parallel with feedback resistor a few pF ceramic capacitor C_F adjusted to optimize the settling time.

MICROPOWER DUAL CMOS VOLTAGE COMPARATORS

- PUSH-PULL CMOS OUTPUT (NO EXTERNAL PULL-UP RESISTOR REQUIRED)
- EXTREMELY LOW SUPPLY CURRENT : 9µA TYP / COMPARATOR
- WIDE SINGLE SUPPLY RANGE (3V TO 16V) OR DUAL SUPPLIES (± 1.5V TO ± 8V)
- EXTREMELY LOW INPUT BIAS CURRENT : 1pA TYP
- EXTREMELY LOW INPUT OFFSET CURRENT : 1pA TYP
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GND
- BUILT-IN ESD PROTECTION
- HIGH INPUT IMPEDANCE : $10^{12}\Omega$ TYP
- FAST RESPONSE TIME : 2µs TYP FOR 5mV OVERDRIVE
- PIN-TO-PIN AND FUNCTIONALLY COMPATIBLE WITH BIPOLAR LM393



N
DIP8
(Plastic Package)

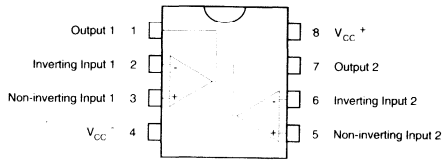
D
SO8
(Plastic Micropackage)

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS3702C	0°C, +70°C	•	•
TS3702I	-40°C, +105°C	•	•
TS3702M	-55°C, +125°C	•	•
Example : TS3702CN			

3702-01.TBL

PIN CONNECTIONS (top view)



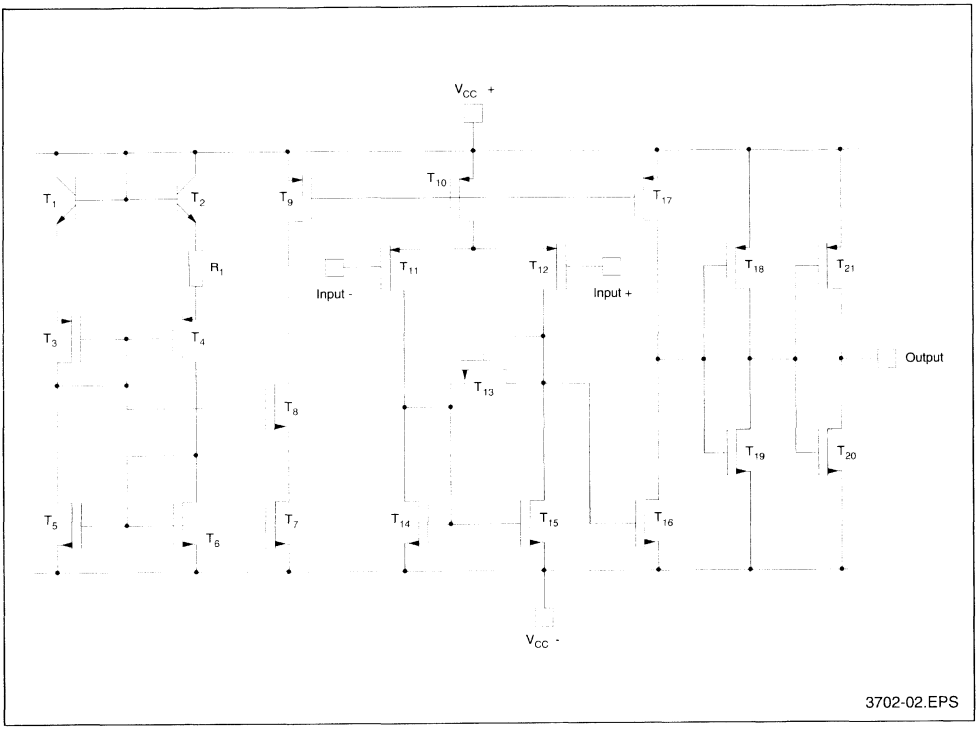
3702-01.EPS

DESCRIPTION

The TS3702 is a micropower CMOS dual voltage comparator with extremely low consumption of 9µA typ / comparator (20 times less than bipolar LM393). The push-pull CMOS output stage allows power and space saving by eliminating the external pull-up resistor required by usual open-collector output comparators.

Thus response times remain similar to the LM393.

SCHEMATIC DIAGRAM (for 1/2 TS3702)



3702-02.EPS

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}^+	Supply Voltage - (note 1)		18	V
V_{id}	Differential Input Voltage - (note 2)		±18	V
V_i	Input Voltage - (note 3)		18	V
V_O	Output Voltage		18	V
I_O	Output Current		20	mA
T_{oper}	Operating Free-Air Temperature Range	TS3702C TS3702I TS3702M	 0 to +70 -40 to +105 -55 to +125	°C
T_{stg}	Storage Temperature Range		-65 to +150	°C

3702-01.TBL

Notes : 1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input and the output voltages must never exceed the magnitude of the positive supply voltage.
4. Short circuit from outputs to V_{CC}^+ can cause excessive heating and eventual destruction.

OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}^+	Supply Voltage	TS3702C,I TS3702M	3 to 16 4 to 16	V
V_{icm}	Common Mode Input Voltage Range		0 to V_{CC}^+ -1.5	V

3702-03.TBL

ELECTRICAL CHARACTERISTICS

V_{CC}^+ = 5V, V_{CC}^- = 0V, T_{amb} = 25°C (unless otherwise specified)

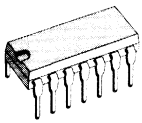
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage $V_{ic} = V_{icm\ min.}$, V_{CC}^+ = 5V to 10V - (note 1) $T_{min.} \leq T_{amb} \leq T_{max.}$		1.2	5 6.5	mV
I_{io}	Input Offset Current - (note 2) V_{ic} = 2.5 V $T_{min.} \leq T_{amb} \leq T_{max.}$		1	 300	pA
I_{ib}	Input Bias Current - (note 2) V_{ic} = 2.5 V $T_{min.} \leq T_{amb} \leq T_{max.}$		1	 600	pA
V_{icm}	Input Common Mode Voltage Range $T_{min.} \leq T_{amb} \leq T_{max.}$	0 to V_{CC}^+-1.2 0 to V_{CC}^+ -1.5			V
CMR	Common-mode Rejection Ratio $V_{ic} = V_{icm\ min.}$		82		dB
SVR	Supply Voltage Rejection Ratio V_{CC}^+ = +5V to +10V		90		dB
V_{OH}	High Level Output Current V_{id} = 1V, I_{OH} = -4mA $T_{min.} \leq T_{amb} \leq T_{max.}$	 4.5 4.3	4.7		V
V_{OL}	Low Level Output Voltage V_{id} = -1V, I_{OL} = 4mA $T_{min.} \leq T_{amb} \leq T_{max.}$		220	300 375	mV
I_{CC}	Supply Current (4 comparators) No load - Outputs low $T_{min.} \leq T_{amb} \leq T_{max.}$		18	40 50	µA
t_{PLH}	Response Time Low to High V_{ic} = 0V, f = 10kHz, C_L = 50pF, Overdrive = 5mV Overdrive = 10mV Overdrive = 20mV Overdrive = 40mV TTL Input		 1.5 1.1 0.9 0.7 0.6		µs
t_{PHL}	Response Time High to Low V_{ic} = 0V, f = 10kHz, C_L = 50pF, Overdrive = 5mV Overdrive = 10mV Overdrive = 20mV Overdrive = 40mV TTL Input		 2.2 1.6 1.1 0.75 0.17		µs
t_f	Fall time f = 10kHz, C_L = 50pF, Overdrive 50mV		30		ns

Note : 1. The specified offset voltage is the maximun value required to drive the output up to 4.5V or down to 0.3V.
2. Maximum values including unavoidable inaccuracies of the industrial test.

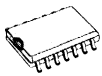
3702-04.TBL

MICROPOWER QUAD CMOS VOLTAGE COMPARATORS

- PUSH-PULL CMOS OUTPUT (NO EXTERNAL PULL-UP RESISTOR REQUIRED)
- EXTREMELY LOW SUPPLY CURRENT : 9µA TYP / COMPARATOR
- WIDE SINGLE SUPPLY RANGE (3V TO 16V) OR DUAL SUPPLIES (± 1.5V TO ± 8V)
- EXTREMELY LOW INPUT BIAS CURRENT : 1pA TYP
- EXTREMELY LOW INPUT OFFSET CURRENT : 1pA TYP
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GND
- BUILT-IN ESD PROTECTION
- HIGH INPUT IMPEDANCE : $10^{12}\Omega$ TYP
- FAST RESPONSE TIME : 2µs TYP FOR 5mV OVERDRIVE
- PIN-TO-PIN AND FUNCTIONALLY COMPATIBLE WITH BIPOLAR LM339



N
DIP14
(Plastic Package)



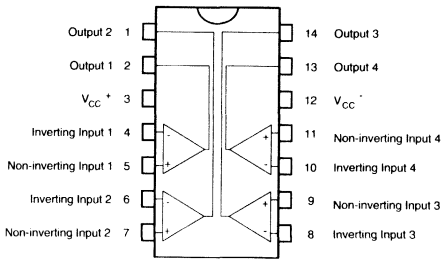
D
SO14
(Plastic Micropackage)

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS3704C	0°C, +70°C	•	•
TS3704I	-40°C, +105°C	•	•
TS3704M	-55°C, +125°C	•	•
Example : TS3704CN			

374-01.TBL

PIN CONNECTIONS (top view)



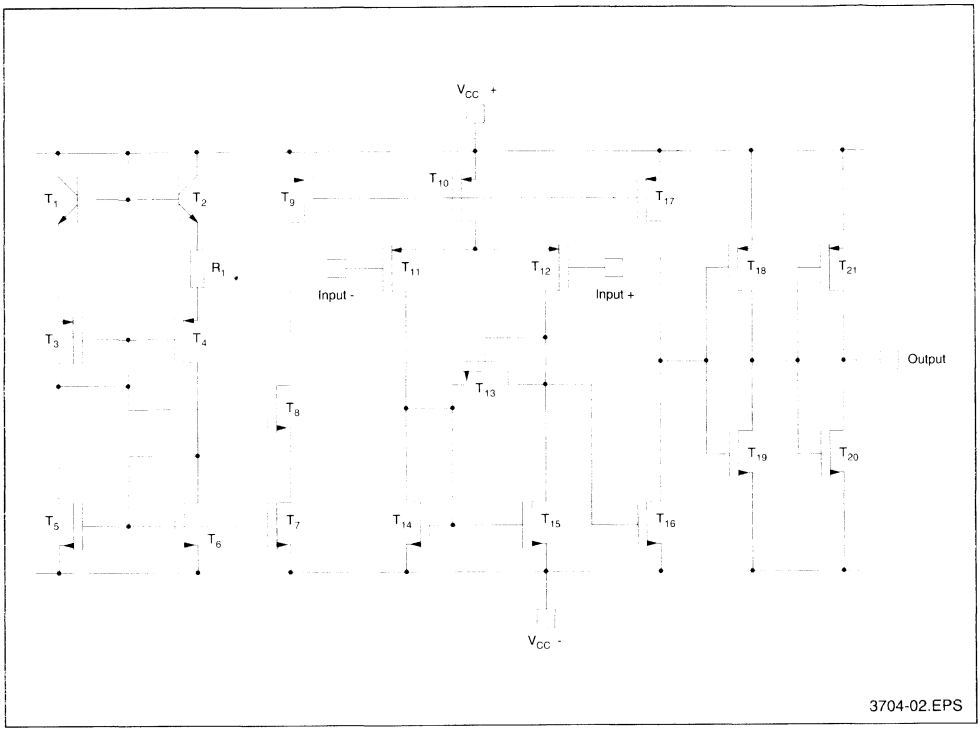
3704-01.EPS

DESCRIPTION

The TS3704 is a micropower CMOS quad voltage comparator with extremely low consumption of 9µA typ / comparator (20 times less than bipolar LM339). The push-pull CMOS output stage allows power and space saving by eliminating the external pull-up resistor required by usual open-collector output comparators.

Thus response times remain similar to the LM339.

SCHEMATIC DIAGRAM (for 1/4 TS3704)



MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}^+	Supply Voltage - (note 1)		18	V
V_{id}	Differential Input Voltage - (note 2)		±18	V
V_i	Input Voltage - (note 3)		18	V
V_O	Output Voltage		18	V
I_O	Output Current		20	mA
T_{oper}	Operating Free-Air Temperature Range	TS3704C TS3704I TS3704M	0 to +70 -40 to +105 -55 to +125	°C
T_{stg}	Storage Temperature Range		-65 to +150	°C

3704-02.TBL

Notes : 1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input and the output voltages must never exceed the magnitude of the positive supply voltage.
4. Short circuit from outputs to V_{CC}^+ can cause excessive heating and eventual destruction.

OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}^+	Supply Voltage	TS3704C,I TS3704M	3 to 16 4 to 16	V
V_{icm}	Common Mode Input Voltage Range		0 to V_{CC}^+ -1.5	V

3704-03.TBL

ELECTRICAL CHARACTERISTICS

$V_{CC}^+ = 5V$, $V_{CC}^- = 0V$, $T_{amb} = 25°C$ (unless otherwise specified)

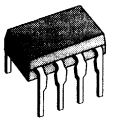
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage $V_{ic} = V_{icm\ min.}$, $V_{CC}^+ = 5V$ to 10V - (note 1) $T_{min.} \leq T_{amb} \leq T_{max.}$		1.2	5 6.5	mV
I_{io}	Input Offset Current - (note 2) $V_{ic} = 2.5\ V$ $T_{min.} \leq T_{amb} \leq T_{max.}$		1	 300	pA
I_{ib}	Input Bias Current - (note 2) $V_{ic} = 2.5\ V$ $T_{min.} \leq T_{amb} \leq T_{max.}$		1	 600	pA
V_{icm}	Input Common Mode Voltage Range $T_{min.} \leq T_{amb} \leq T_{max.}$	0 to V_{CC}^+ -1.2 0 to V_{CC}^+ -1.5			V
CMR	Common-mode Rejection Ratio $V_{ic} = V_{icm\ min.}$		78		dB
SVR	Supply Voltage Rejection Ratio $V_{CC}^+ = +5V$ to +10V		92		dB
V_{OH}	High Level Output Current $V_{id} = 1V$, $I_{OH} = -4mA$ $T_{min.} \leq T_{amb} \leq T_{max.}$	 4.5 4.3	 4.7		V
V_{OL}	Low Level Output Voltage $V_{id} = -1V$, $I_{OL} = 4mA$ $T_{min.} \leq T_{amb} \leq T_{max.}$		234	300 375	mV
I_{CC}	Supply Current (4 comparators) No load - Outputs low $T_{min.} \leq T_{amb} \leq T_{max.}$		36	80 100	µA
t_{PLH}	Response Time Low to High $V_{ic} = 0V$, f = 10kHz, $C_L = 50pF$, Overdrive = 5mV Overdrive = 10mV Overdrive = 20mV Overdrive = 40mV TTL Input		 1.2 1 0.9 0.8 0.7		µs
t_{PHL}	Response Time High to Low $V_{ic} = 0V$, f = 10kHz, $C_L = 50pF$, Overdrive = 5mV Overdrive = 10mV Overdrive = 20mV Overdrive = 40mV TTL Input		 2 1.5 0.9 0.7 0.15		µs
t_f	Fall time f = 10kHz, $C_L = 50pF$, Overdrive 50mV		30		ns

374-04.TBL

Note : 1. The specified offset voltage is the maximun value required to drive the output up to 4.5V or down to 0.3V.
2. Maximum values including unavoidable inaccuracies of the industrial test.

GENERAL PURPOSE SINGLE OPERATIONAL AMPLIFIERS

- LARGE INPUT VOLTAGE RANGE
- NO LATCH-UP
- HIGH GAIN
- SHORT-CIRCUIT PROTECTION
- NO FREQUENCY COMPENSATION REQUIRED
- SAME PIN CONFIGURATION AS THE UA709



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

J
CERDIP8
(Cerdip Package)

H
TO99
(Metal Can)

DESCRIPTION

The UA741 is a high performance monolithic operational amplifier constructed on a single silicon chip. It is intented for a wide range of analog applications.

- Summing amplifier
- Voltage follower
- Integrator
- Active filter
- Function generator

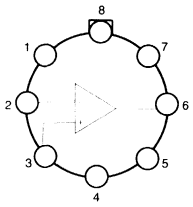
The high gain and wide range of operating voltages provide superior performances in integrator, summing amplifier and general feedback applications. The internal compensation network (6dB / octave) insures stability in closed loop circuits.

Part Number	Temperature Range	Package			
		H	N	J	D
UA741C/E	0°C, +70°C	•	•	•	•
UA741I	-40°C, +105°C	•	•	•	•
UA741M/A	-55°C, +125°C	•	•	•	•
Examples : UA741CN, UA741IH					

741-01.TBL

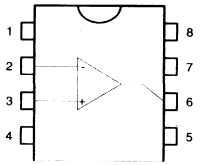
PIN CONNECTIONS (top views)

TO99



741-01.EPS

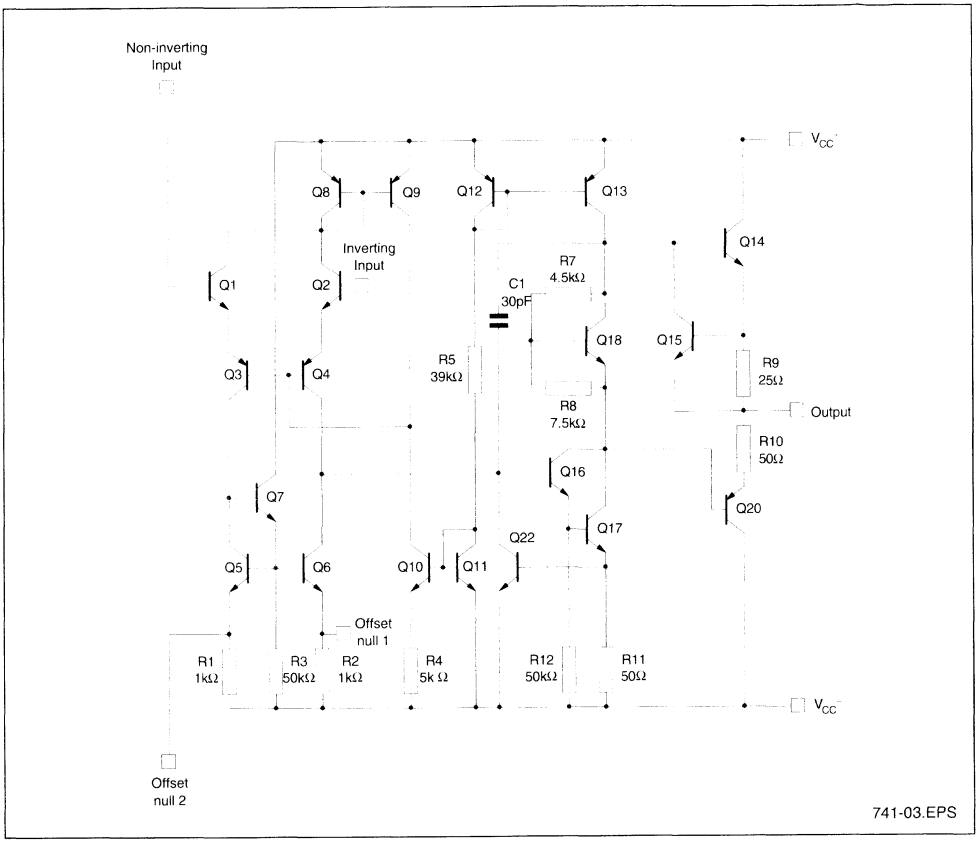
DIP8/CERDIP8
SO8



741-02.EPS

1 - Offset null 1
2 - Inverting input
3 - Non-inverting input
4 - V_{CC}^-
5 - Offset null 2
6 - Output
7 - V_{CC}^+
8 - N.C.

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	UA741M-A	UA741I	UA741C-E	Unit
V_{CC}	Supply Voltage	±22	±22	±22	V
V_i	Input Voltage	±15	±15	±15	V
V_{id}	Differential Input Voltage	±30	±30	±30	V
P_{tot}	Power Dissipation	500	500	500	mW
	Output Short-circuit Duration	Infinite			
T_{oper}	Operating Free Air Temperature Range	-55 to +125	-40 to +105	0 to +70	°C
T_{stg}	Storage Temperature Range	-65 to +150	-65 to +150	-65 to +150	°C

741-02.TBL

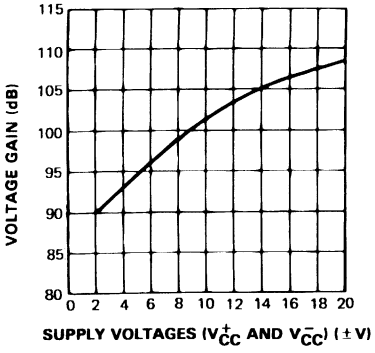
ELECTRICAL CHARACTERISTICS

V_{CC} = ±15V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage ($R_s \leq 10k\Omega$) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$ UA741E,A T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		 1 1	 5 6 2 4	mV
I_{io}	Input Offset Current T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		 2	 30 70	nA
I_{ib}	Input Bias Current T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		 10	 100 200	nA
A_{vd}	Large Signal Voltage Gain (V_o = ±10V, R_L = 2kΩ) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	 50 25	 200		V/mV
SVR	Supply Voltage Rejection Ratio ($R_s \leq 10k\Omega$) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	 77 77	 90		dB
I_{CC}	Supply Current, no load T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		 1.7	 2.8 3.3	mA
V_{icm}	Input Common Mode Voltage Range T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	 ±12 ±12			V
CMR	Common Mode Rejection Ratio ($R_s \leq 10k\Omega$) T_{amb} = 25°C $T_{min} \leq T_{amb} \leq T_{max}$	 70 70	 90		dB
I_{os}	Output Short-circuit Current	10	25	40	mA
$\pm V_{OPP}$	Output Voltage Swing T_{amb} = 25°C R_L = 10kΩ R_L = 2kΩ $T_{min.} \leq T_{amb} \leq T_{max}$ R_L = 10kΩ R_L = 2kΩ	 12 10 12 10	 14 13		V
SR	Slew Rate (V_i = ±10V, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)	0.25	0.5		V/µs
t_r	Rise Time (V_i = ±20mV, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)		0.3		µs
K_{OV}	Overshoot (V_i = ±20mV, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)		5		%
R_i	Input Resistance	0.3	2		MΩ
GBP	Gain Bandwidth Product (V_i = 10mV, R_L = 2kΩ, C_L = 100pF, f = 100kHz)	0.7	1		MHz
THD	Total Harmonic Distortion (f = 1kHz, A_V = 20dB, R_L = 2kΩ, V_o = $2V_{PP}$, C_L = 100pF, T_{amb} = 25°C)		0.06		%
e_n	Equivalent Input Noise Voltage (f = 1kHz, R_s = 100Ω)		23		$\frac{nV}{\sqrt{Hz}}$
Øm	Phase Margin		50		Degrees

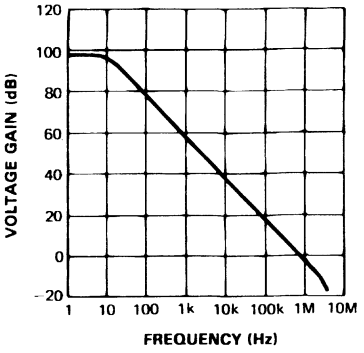
741-03.TBL

OPEN LOOP VOLTAGE GAIN (Typ.)



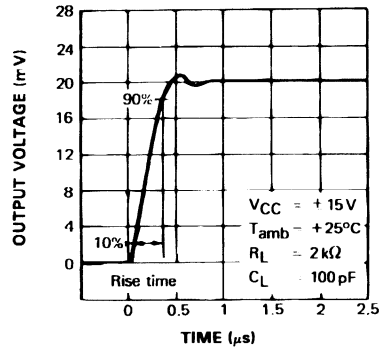
741-04.EPS

OPEN LOOP FREQUENCY RESPONSE (Typ.)



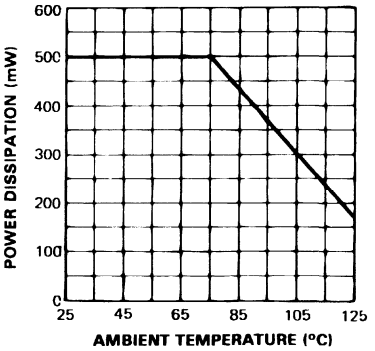
741-05.EPS

TRANSIENT RESPONSE (Typ.)



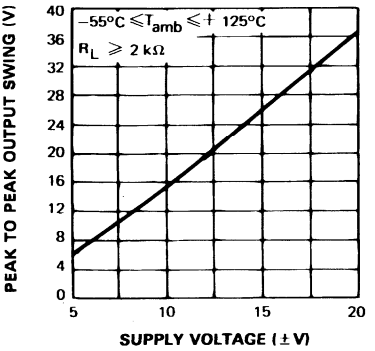
741-06.EPS

ABSOLUTE MAXIMUM POWER DISSIPATION



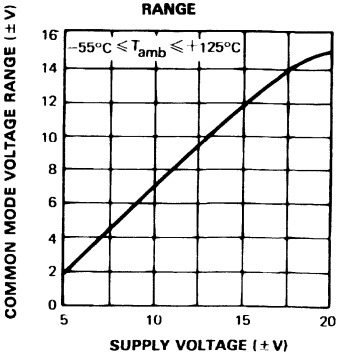
741-07.EPS

OUTPUT VOLTAGE SWING



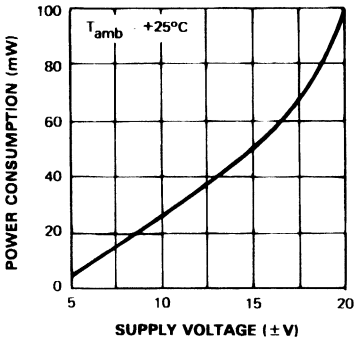
741-08.EPS

INPUT COMMON MODE VOLTAGE RANGE



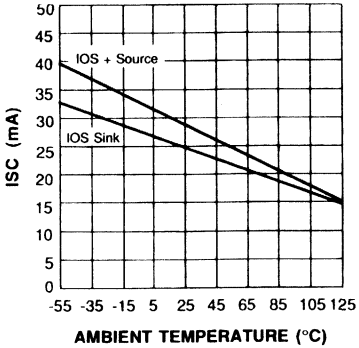
741-09.EPS

POWER CONSUMPTION



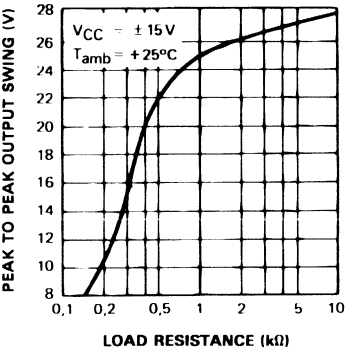
741-10.EPS

OUTPUT CURRENT vs AMBIENT TEMPERATURE



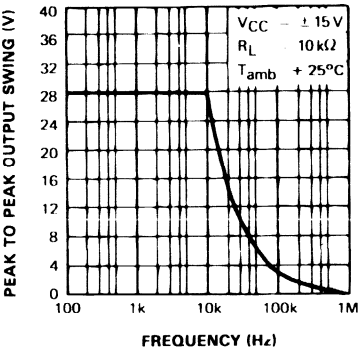
741-11.EPS

OUTPUT VOLTAGE SWING



741-12.EPS

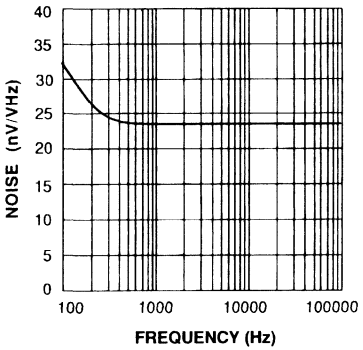
OUTPUT VOLTAGE SWING



741-13.EPS

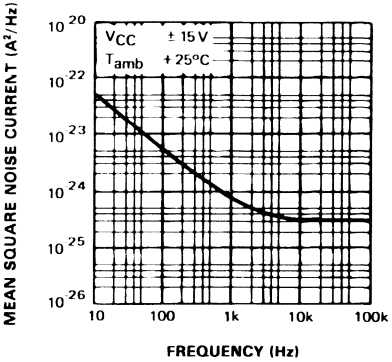
EQUIVALENT INPUT NOISE vs FREQUENCY

Rg = 100 Ω



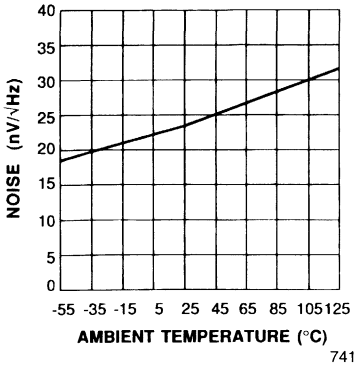
741-14.EPS

INPUT NOISE CURRENT



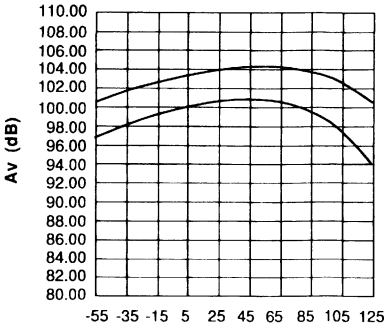
741-15.EPS

EQUIVALENT INPUT NOISE vs AMBIENT TEMPERATURE



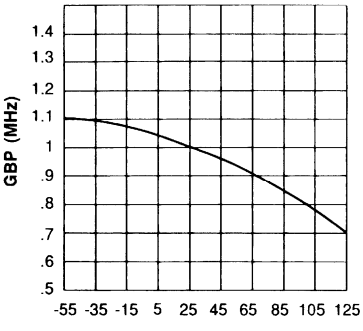
741-16.EPS

LARGE SIGNAL VOLTAGE GAIN vs AMBIENT TEMPERATURE



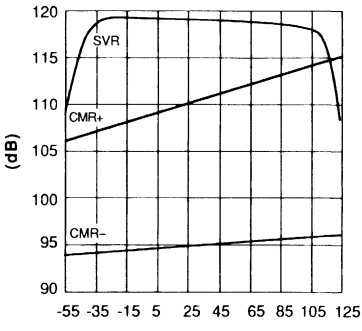
741-17.EPS

GAIN BANDWIDTH PRODUCT vs AMBIENT TEMPERATURE



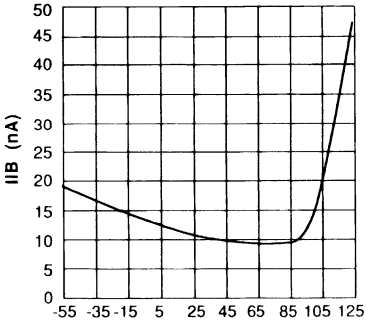
741-18.EPS

POWER SUPPLY & COMMON MODE REJECTION RATIO vs AMBIENT TEMPERATURE



741-19.EPS

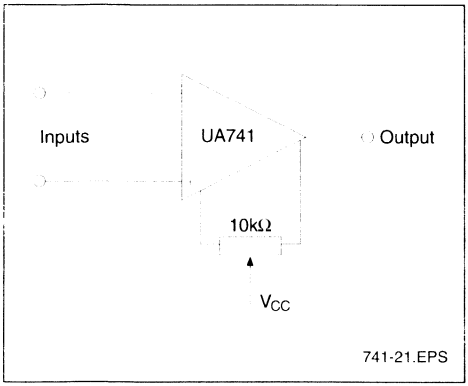
INPUT BIAS CURRENT vs AMBIENT TEMPERATURE



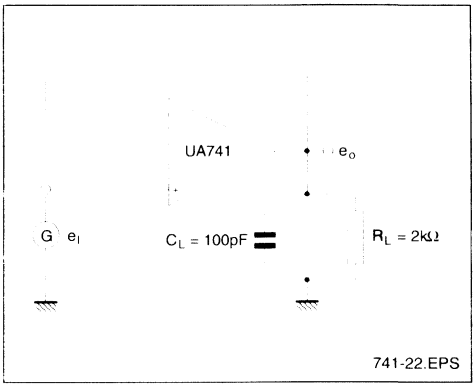
741-20.EPS

MEASUREMENT DIAGRAMS

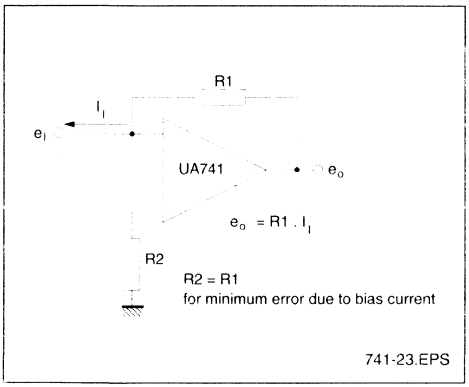
OFFSET VOLTAGE NULL CIRCUIT



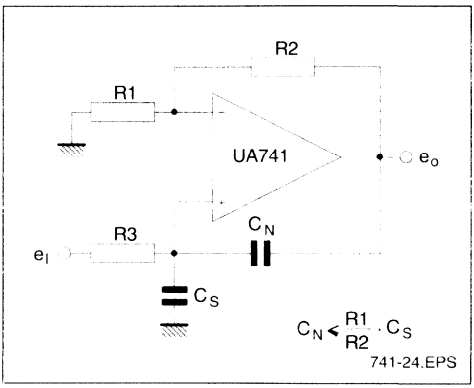
TRANSIENT RESPONSE TEST CIRCUIT



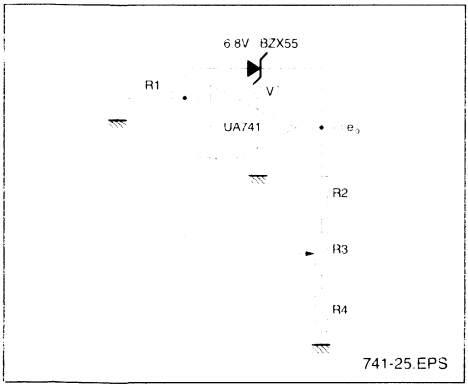
CURRENT TO VOLTAGE CONVERTER



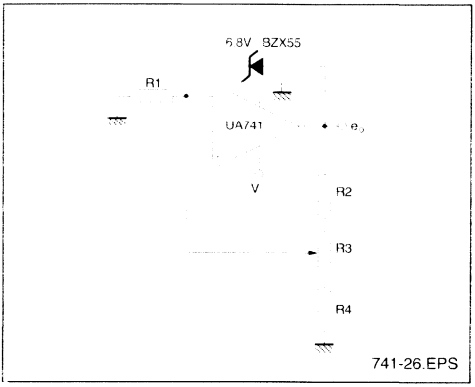
NEUTRALIZING INPUT CAPACITANCE TO OPTIMIZE RESPONSE TIME



POSITIVE VOLTAGE REFERENCE

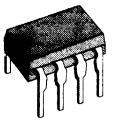


NEGATIVE VOLTAGE REFERENCE



PRECISION SINGLE OPERATIONAL AMPLIFIERS

- FREQUENCY COMPENSATION WITH A SINGLE 30pF CAPACITOR
- OPERATION FROM ±5V TO ±15V
- LOW POWER CONSUMPTION : 50mW AT ±15V
- CONTINUOUS SHORT-CIRCUIT PROTECTION
- OPERATION AS A COMPARATOR WITH DIFFERENTIAL INPUTS AS HIGH AS ±30V
- NO LATCH-UP WHEN COMMON-MODE RANGE IS EXCEEDED
- SAME PIN CONFIGURATION AS THE LM101A



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

J
CERDIP8
(Cerdip Package)

H
TO99
(Metal Can)

Part Number	Temperature Range	Package			
		H	N	J	D
UA748C	0°C, +70°C	•	•	•	•
UA748I	-40°C, +105°C	•	•	•	•
UA748M	-55°C, +125°C	•	•	•	•
Example : UA748CH					

748-01.TBL

DESCRIPTION

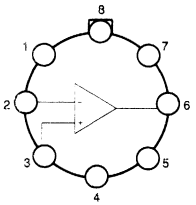
The UA748 is a general-purpose operational amplifier built on a single silicon chip. The resulting close match and tight thermal coupling gives low offsets and temperature drift as well as fast recovery from thermal transients.

- Short-circuit protection
- Offset voltage null capability
- Large common-mode and differential voltage ranges
- Low power consumption
- No latch-up

The unity-gain compensation specified makes the circuit stable for all feedback configurations, even with capacitive loads. However, it is possible to optimize compensation for best high frequency performance at any gain. The low power dissipation permits high voltage operation and simplifies packaging in full-temperature range systems.

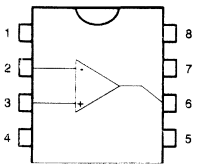
PIN CONNECTIONS (top views)

TO99



748-01.EPS

DIP8/CERDIP8
SO8

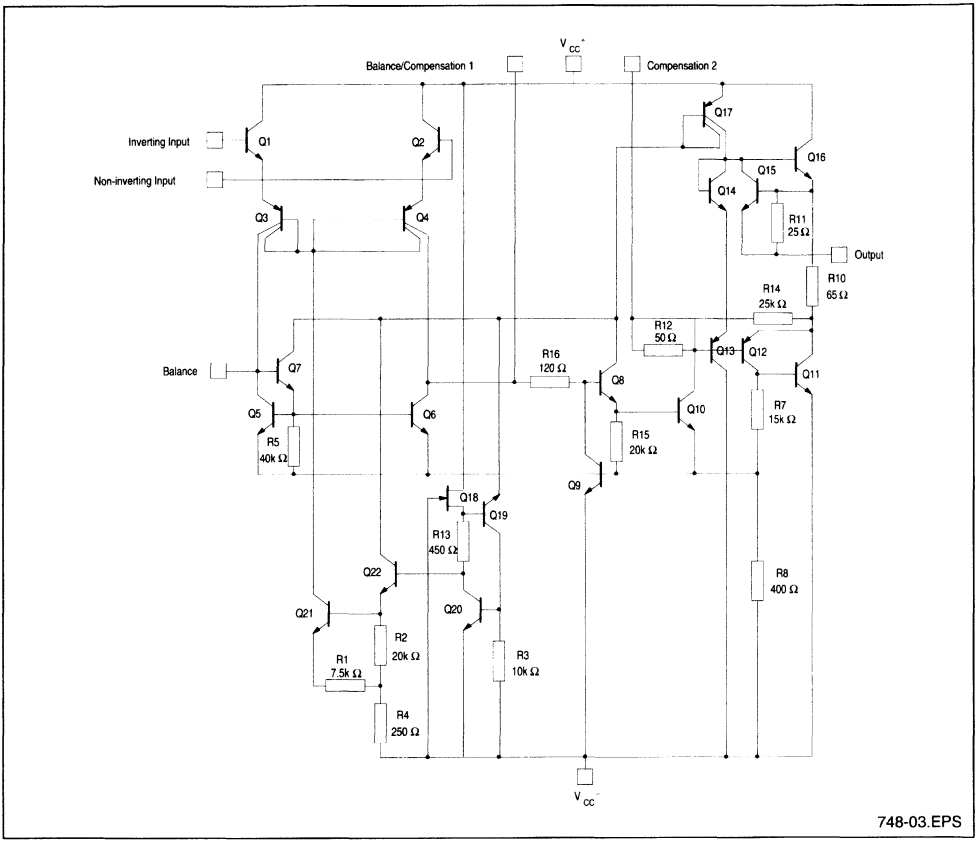


748-02.EPS

1 - Offset null 1/frequency compensation
2 - Inverting input
3 - Non-inverting input
4 - V_{CC}^-
5 - Offset null 2
6 - Output
7 - V_{CC}^+
8 - Frequency compensation

December 1992

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value			Unit
		UA748M	UA748I	UA748C	
V_{CC}	Supply Voltage	±22	±22	±22	V
V_i	Input Voltage	±15	±15	±15	V
V_{id}	Differential Input Voltage	±30	±30	±30	V
P_{tot}	Power Dissipation	500	500	500	mW
	Output Short-circuit Duration	Infinite			
T_{oper}	Operating Free Air Temperature Range	-55 to +125	-40 to +105	0 to +70	°C
T_{stg}	Storage Temperature Range	-65 to +150	-65 to +150	-65 to +150	°C

748-03 TRI

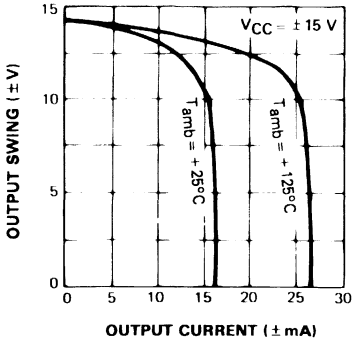
ELECTRICAL CHARACTERISTICS

$\pm 5V \leq V_{CC} \leq \pm 20V$, $C_1 = 30pF$, $T_{amb} = 25°C$ (unless otherwise specified)

Symbol	Parameter	UA748-M-I			UA748C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage ($R_s \leq 10k\Omega$)							mV
	$T_{amb} = 25°C$		0.2	2		2	7.5	
	$T_{min} \leq T_{amb} \leq T_{max}$			3			10	
I_{ib}	Input Bias Current							nA
	$T_{amb} = 25°C$		1.5	10		2	50	
	$T_{min} \leq T_{amb} \leq T_{max}$			20			70	
I_{io}	Input Offset Current							nA
	$T_{amb} = 25°C$		25	75		70	250	
	$T_{min} \leq T_{amb} \leq T_{max}$			10			300	
A_{v1}	Large Signal Voltage Gain							V/mV
	($V_{CC} = \pm 15V$, $V_o = \pm 10V$, $R_L = 2k\Omega$)							
	$T_{amb} = 25°C$	50	100		25	10		
	$T_{min} \leq T_{amb} \leq T_{max}$	25			15			
SVR	Supply Voltage Rejection Ratio ($R_s \leq 10k\Omega$)							dB
	$T_{amb} = 25°C$	80	96		70	96		
	$T_{min} \leq T_{amb} \leq T_{max}$	80			70			
I_{CC}	Supply Current, no load							mA
	$T_{amb} = 25°C$		1.8	3		1.8	3	
	$T_{min} \leq T_{amb} \leq T_{max}$			3			3	
V_{icm}	Input Common Mode Voltage Range ($V_{CC} = \pm 20V$)							V
	$T_{amb} = 25°C$	±15			±15			
	$T_{min} \leq T_{amb} \leq T_{max}$	±15			±15			
CMR	Common Mode Rejection Ratio ($R_s \leq 10k\Omega$)							dB
	$T_{amb} = 25°C$	80	96		70	96		
	$T_{min} \leq T_{amb} \leq T_{max}$	80			70			
I_{os}	Output Short-circuit Current ($V_{CC} = \pm 15V$)	10	30	50	10	30	50	mA
$\pm V_{OPP}$	Output Voltage Swing ($V_{CC} = \pm 15V$)							V
	$T_{amb} = 25°C$ $R_L = 10k\Omega$	12	14		12	14		
	$R_L = 2k\Omega$	10	13		10	13		
	$T_{min} \leq T_{amb} \leq T_{max}$ $R_L = 10k\Omega$	12			12			
	$R_L = 2k\Omega$	10			10			
SR	Slew Rate ($V_{CC} = \pm 15V$, $V_i = \pm 10V$, $R_L = 2k\Omega$, $C_L = 100pF$, $T_{amb} = 25°C$, unity gain)	0.25	0.5		0.25	0.5		V/µs
t_r	Rise Time ($V_{CC} = \pm 15V$, $V_i = 20mV$, $R_L = 2k\Omega$, $C_L = 100pF$, $T_{amb} = 25°C$, unity gain)		0.3			0.3		µs
K_{OV}	Overshoot ($V_{CC} = \pm 15V$, $V_i = 20mV$, $R_L = 2k\Omega$, $C_L = 100pF$, $T_{amb} = 25°C$, unity gain)		5			5		%
Z_i	Input Impedance ($V_{CC} = \pm 15V$)	1.5	4		1.5	4		MΩ
R_o	Output Resistance ($V_{CC} = \pm 15V$)		75			75		Ω
GBP	Gain Bandwidth Product ($V_{CC} = \pm 15V$, $V_i = 10mV$, $R_L = 2k\Omega$, $C_L = 100pF$, f = 100kHz)	0.5	1		0.5	1		MHz
THD	Total Harmonic Distortion ($V_{CC} = \pm 15V$, f = 1kHz, $A_V = 20dB$, $R_L = 2k\Omega$, $V_o = 2V_{PP}$, $C_L = 100pF$)		0.015			0.015		%
e_n	Equivalent Input Noise Voltage ($V_{CC} = \pm 15V$, f = 1kHz, $R_S = 100\Omega$)		25			25		$\frac{nV}{\sqrt{Hz}}$
DV_{io}	Input Offset Current Drift							pA/°C
	$25°C \leq T_{amb} \leq T_{max}$		10	100		10	300	
	$T_{min} \leq T_{amb} \leq 25°C$		20	200		20	600	
DI_{io}	Input Offset Voltage Drift							µV/°C
	$T_{min} \leq T_{amb} \leq T_{max}$		3	15		6	30	

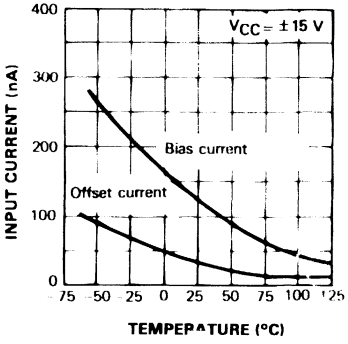
748-03.TBL

CURRENT LIMITING



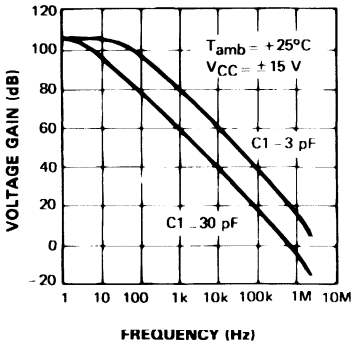
748-04.EPS

INPUT CURRENT



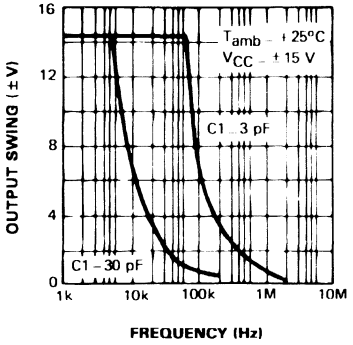
748-05.EPS

OPEN LOOP FREQUENCY RESPONSE



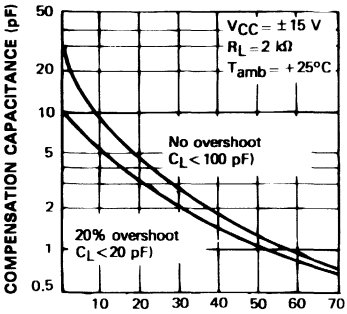
748-06.EPS

LARGE SIGNAL FREQUENCY RESPONSE



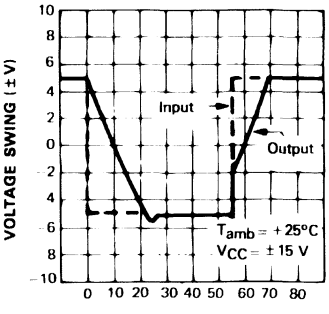
748-07.EPS

FREQUENCY COMPENSATION



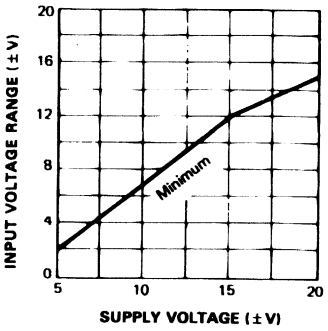
748-08.EPS

VOLTAGE FOLLOWER PULSE RESPONSE



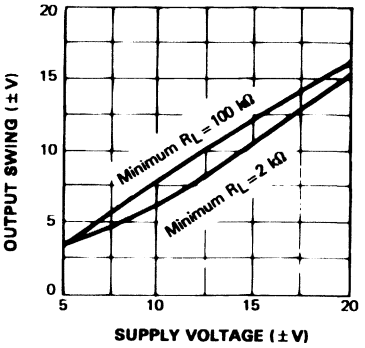
748-09.EPS

INPUT VOLTAGE RANGE



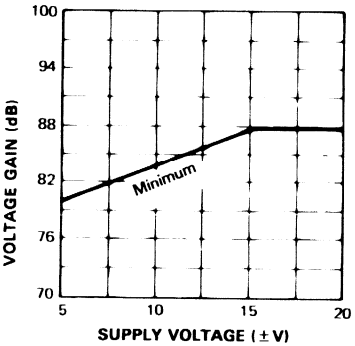
748-10.EPS

OUTPUT SWING



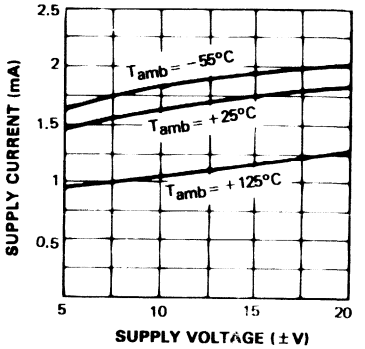
748-11.EPS

VOLTAGE GAIN



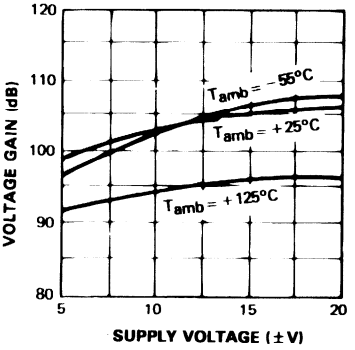
748-12.EPS

SUPPLY CURRENT



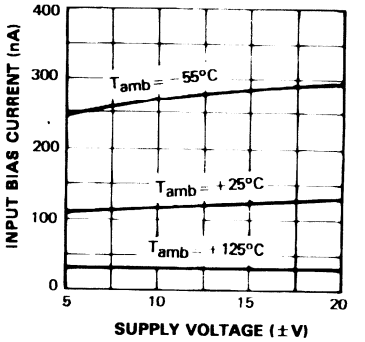
748-13.EPS

VOLTAGE GAIN



748-14.EPS

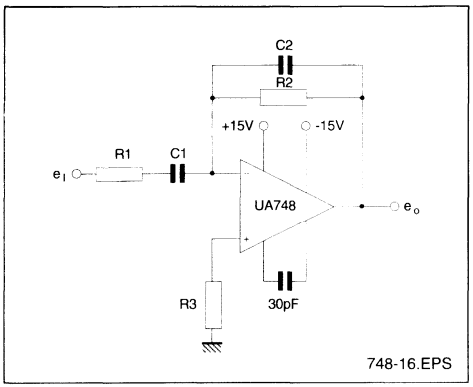
INPUT BIAS CURRENT



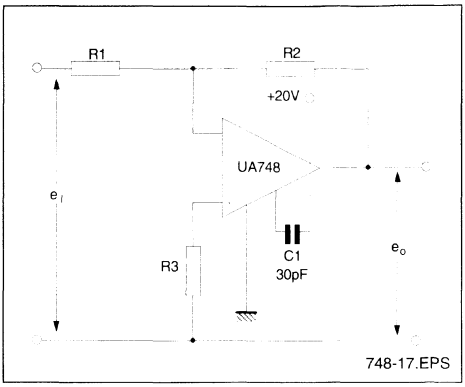
748-15.EPS

TYPICAL APPLICATIONS

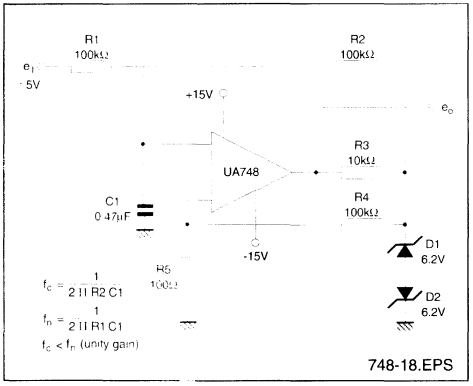
PRACTICAL DIFFERENTIATOR



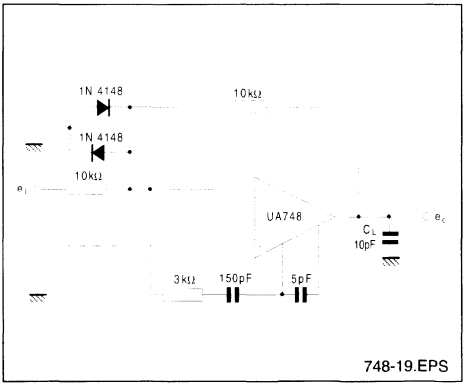
SINGLE SUPPLY OPERATION



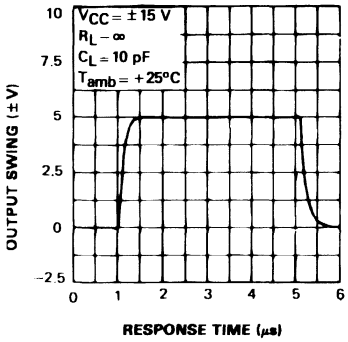
PULSE WIDTH MODULATOR



FEED-FORWARD COMPENSATION



LARGE SIGNAL FEED-FORWARD TRANSIENT RESPONSE



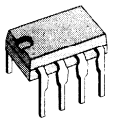
748-20.EPS

SGS-THOMSON MICROELECTRONICS

UA776

PROGRAMMABLE LOW POWER SINGLE OPERATIONAL AMPLIFIERS

- MICROPOWER OPERATION
- NO FREQUENCY COMPENSATION REQUIRED
- WIDE PROGRAMMING RANGE
- HIGH SLEW RATE
- SHORT-CIRCUIT PROTECTION
- PROGRAMMABLE SINGLE OP-AMPs



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

H
TO99
(Metal Can)

Part Number	Temperature Range	Package		
		H	N	D
UA776C	0°C, +70°C	•	•	•
UA776I	-40°C, +105°C	•	•	•
UA776M	-55°C, +125°C	•	•	•

Examples : UA776CH, UA776CN, UA776CD

776-01.TBL

DESCRIPTION

The UA776 programmable operational amplifier is characterized by, low supply current and low input noise over a wide range of operating supply voltages.

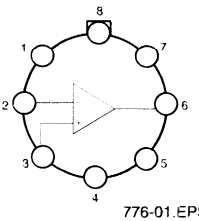
Coupled with programmable electrical characteristics, it is an extremely versatile amplifier for use in high accuracy, low power consumption analog applications.

Input noise voltage and current, power consumption, and input current can be optimized by a single resistor or current source that sets the chip quiescent current for nano-watt power consumption or for characteristics similar to the UA741.

Internal frequency compensation, absence of latch up, high slew rate and short-circuit protection assure ease of use in long time integrators, active filters, and sample and hold circuits.

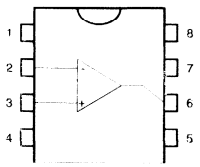
PIN CONNECTIONS (top views)

TO99



776-01.EPS

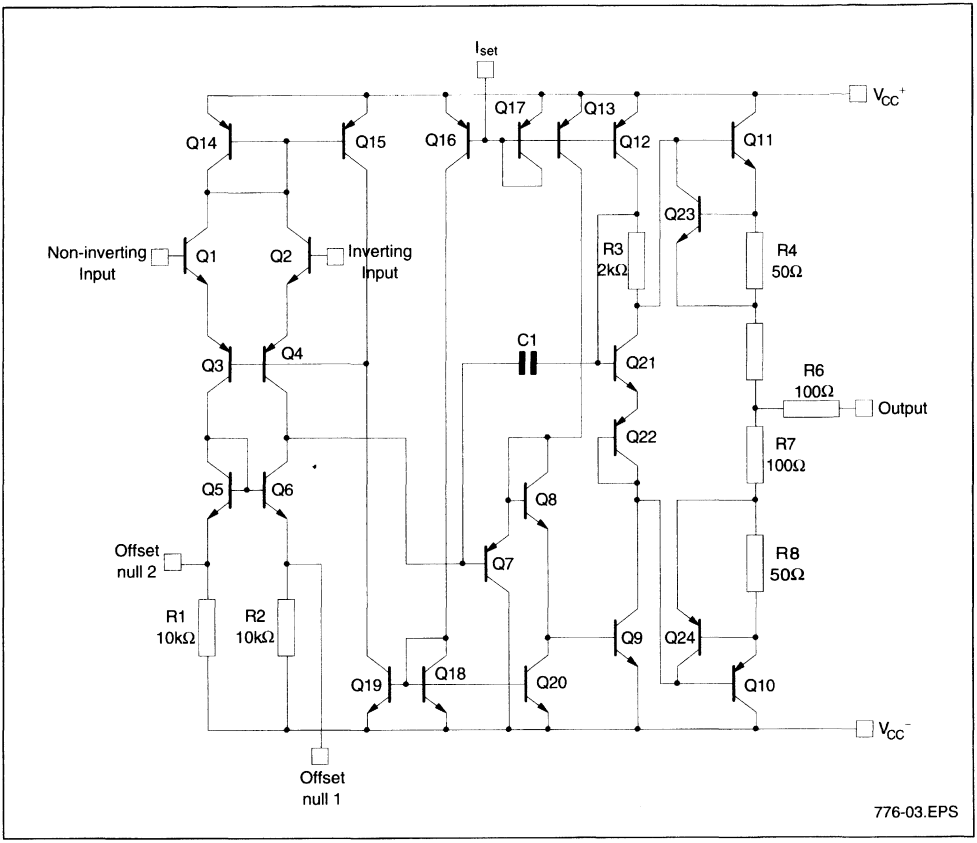
DIP8/SO8



776-02.EPS

1 - Offset null 1
2 - Inverting input
3 - Non-inverting input
4 - V_{CC}^-
5 - Offset null 2
6 - Output
7 - V_{CC}^+
8 - I_{set}

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	UA776M	UA776I	UA776C	Unit
V_{CC}	Supply Voltage	±18	±18	±18	V
V_i	Input Voltage - (note 1)	±15	±15	±15	V
V_{id}	Differential Input Voltage	±30	±30	±30	V
P_{tot}	Power Dissipation UA776CH	500	310	310 500	mW
	Output Short-circuit Duration	Infinite			
T_{oper}	Operating Free Air Temperature Range	-55 to +125	-40 to +105	0 to +70	°C
T_{stg}	Storage Temperature Range	-65 to +150	-65 to +150	-65 to +150	°C

776-02.TBL

Note : 1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS

V_{CC} = ±15V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter		I_{set} = 1.5µA			I_{set} = 15µA			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage								mV
	T_{amb} = 25°C			2	5		2	5	
	$T_{min.} \le T_{amb} \le T_{max.}$				6			6	
I_{io}	Input Offset Current								nA
	T_{amb} = 25°C			0.7	3		2	15	
	$T_{min.} \le T_{amb} \le T_{max.}$				10			40	
I_{ib}	input Bias Current								nA
	T_{amb} = 25°C	UA776M		2	7.5		15	50	
		UA776I,C		2	10		15	50	
	$T_{min.} \le T_{amb} \le T_{max.}$				20			100	
A_{vd}	Large Signal Voltage Gain (V_o = ±10V)								V/mV
	T_{amb} = 25°C	R_L = 5kΩ				100	400		
		R_L = 75kΩ	200	400					
	$T_{min.} \le T_{amb} \le T_{max.}$	R_L = 75kΩ	100						
		R_L = 5kΩ				75			
SVR	Supply Voltage Rejection Ratio ($R_s \le$ 10kΩ)								dB
	T_{amb} = 25°C		77	92		77	92		
	$T_{min.} \le T_{amb} \le T_{max.}$		77			77			
I_{CC}	Supply Current - (no load)								µA
	T_{amb} = 25°C			20	25		160	180	
	$T_{min.} \le T_{amb} \le T_{max.}$				30			200	
V_{icm}	Input Common Mode Voltage Range		±10			±10			V
CMR	Common Mode Rejection Ratio ($R_s \le$ 10kΩ)								dB
	T_{amb} = 25°C		70	90		70	90		
	$T_{min.} \le T_{amb} \le T_{max.}$		70			70			
I_{os}	Output Short-circuit Current		0.5	3	15	6	12	30	mA
$\pm V_{OPP}$	Output Voltage Swing								V
	T_{amb} = 25°C	R_L = 5kΩ				10	13		
		R_L = 75kΩ	12	14					
	$T_{min.} \le T_{amb} \le T_{max}$	R_L = 75kΩ	10			10			
V_{ior}	Offset Voltage Adjustment Range			9			18		mV
SR	Slew Rate (V_i = ±10V, C_L = 100pF, unity gain)								V/µs
		R_L = 5kΩ				0.2	0.8		
		R_L = 75kΩ	0.01	0.1					
t_r	Rise Time (V_i = ±20mV, C_L = 100pF, unity gain)								µs
		R_L = 5kΩ					0.35		
		R_L = 75kΩ		1.6					
K_{OV}	Overshoot (V_i = ±20mV, C_L =100pF, unity gain)								%
		R_L = 5kΩ					10		
		R_L = 75kΩ		0					
R_i	Input Resistance			50			5		MΩ
C_{id}	Differential Input Capacitance			2			2		pF
R_o	Output Resistance			5			1		kΩ
GBP	Gain Bandwidth Product (T_{amb} = 25°C, C_L = 100pF)								MHz
	f = 100kHz	R_L = 5kΩ				0.4	0.7		
	f = 10kHz	R_L = 75kΩ	0.03	0.1					
THD	Total Harmonic Distortion (f = 1kHz, A_V = 20dB, V_o = 2V_{PP}, C_L = 100pF, T_{amb} = 25°C)								%
		R_L = 5kΩ					0.025		
		R_L = 75kΩ		0.8					
e_n	Equivalent Input Noise Voltage (f = 1kHz, R_s = 100Ω)			20			20		$\frac{nV}{\sqrt{Hz}}$

776-03.TBL

ELECTRICAL CHARACTERISTICS

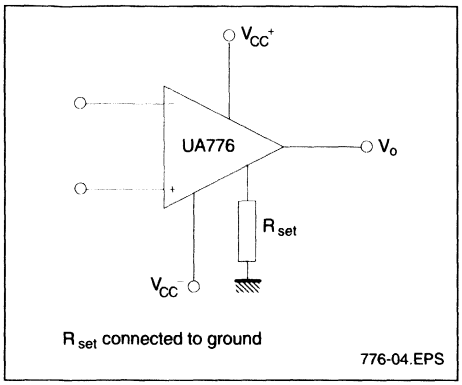
V_{CC} = ±3V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	I_{set} = 1.5µA			I_{set} = 15µA			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$		2	5 6		2	5 6	mV
I_{io}	Input Offset Current T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$		0.7	3 10		2	15 40	nA
I_{ib}	Input Bias Current T_{amb} = 25°C UA776M UA776I,C $T_{min.} \le T_{amb} \le T_{max.}$		2 2	7 10 20		15 15	50 50 100	nA
A_{vd}	Large Signal Voltage Gain (V_o = ±1V) T_{amb} = 25°C R_L = 5kΩ R_L = 75kΩ $T_{min.} \le T_{amb} \le T_{max.}$ R_L = 5kΩ R_L = 75kΩ	 50 25	 200		 50 25	 200		V/mV
SVR	Supply Voltage Rejection Ratio ($R_s \le$ 10kΩ) T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$	 77 77	 92		 77 77	 92		dB
I_{CC}	Supply Current, no load T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$		13	20 25		130	160 180	µA
V_{icm}	Input Common Mode Voltage Range	±1			±1			V
CMR	Common Mode Rejection Ratio ($R_s \le$ 10kΩ) T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$	 70 70	 90		 70 70	 90		dB
I_{os}	Output Short-circuit Current	0.5	3	15	2	5	20	mA
$\pm V_{OPP}$	Output Voltage Swing T_{amb} = 25°C R_L = 75kΩ R_L = 5kΩ $T_{min.} \le T_{amb} \le T_{max}$ R_L = 75kΩ R_L = 5kΩ	 2 2	 2.4		 2 1.9 2 1.9	 2.4 2.1		V
V_{ior}	Offset Voltage Adjustment Range		9			18		mV
SR	Slew Rate (V_i = ±1V, C_L = 100pF, unity gain) R_L = 5kΩ R_L = 75kΩ		 0.03			0.35		V/µs
t_r	Rise Time (V_i = ±20mV, C_L = 100pF, unity gain) R_L = 5kΩ R_L = 75kΩ		 3			0.6		µs
K_{OV}	Overshoot (V_i = ±20mV, C_L =100pF, unity gain) R_L = 5kΩ R_L = 75kΩ		 0			5		%
R_i	Input Resistance		50			5		MΩ
C_{id}	Differential Input Capacitance		2			2		pF
R_o	Output Resistance		5			1		kΩ
GBP	Gain Bandwidth Product (T_{amb} = 25°C, C_L = 100pF) f = 100kHz R_L = 5kΩ f = 10kHz R_L = 75kΩ		 0.075			0.5		MHz
THD	Total Harmonic Distortion (f = 1kHz, A_V = 20dB, V_o = 1V_{PP}, C_L = 100pF, T_{amb} = 25°C) R_L = 5kΩ R_L = 75kΩ		 1			0.03		%
e_n	Equivalent Input Noise Voltage (f = 1kHz, R_s = 100Ω)		20			20		$\frac{nV}{\sqrt{Hz}}$

776-04.TBL

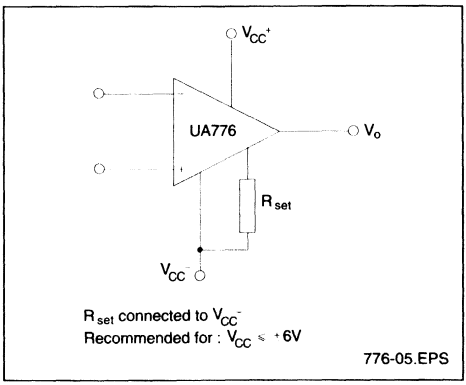
BIASING CIRCUITS

RESISTOR BIASING



R_{set} connected to ground

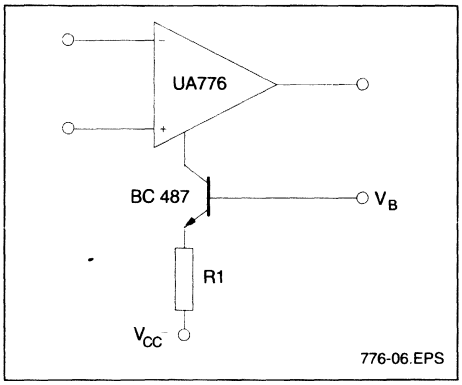
776-04.EPS



R_{set} connected to V_{CC}^-
Recommended for : $V_{CC} \approx +6V$

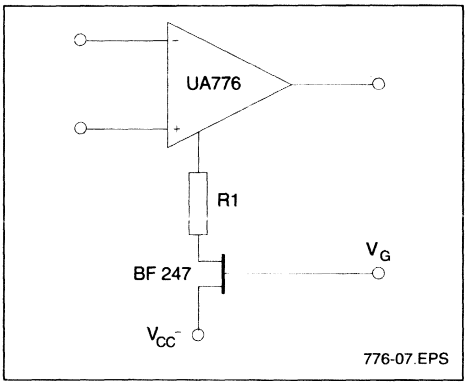
776-05.EPS

TRANSISTOR CURRENT SOURCE BIASING



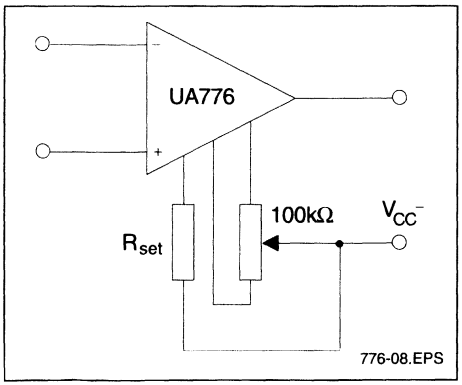
776-06.EPS

FET CURRENT SOURCE BIASING



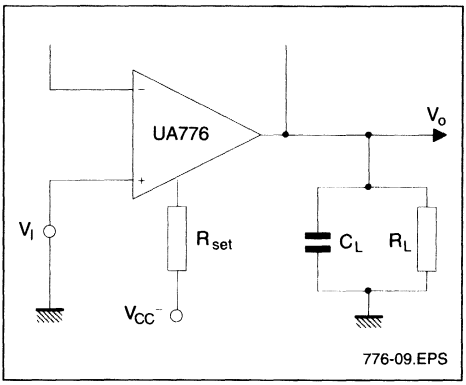
776-07.EPS

OFFSET VOLTAGE NULL CIRCUIT



776-08.EPS

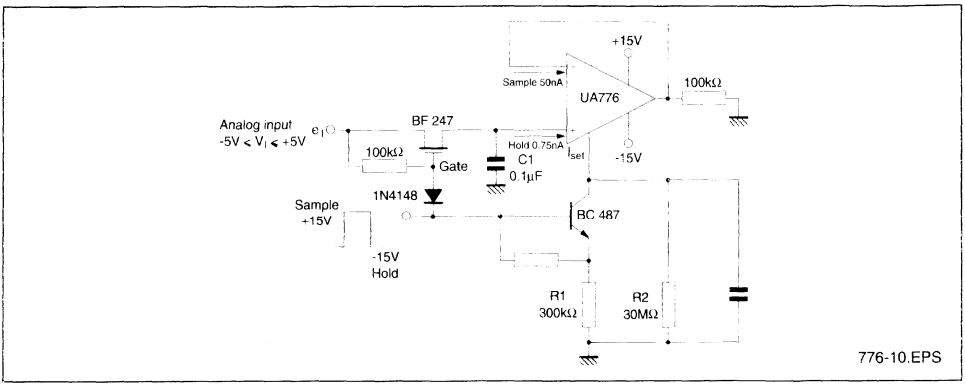
TRANSIENT RESPONSE TIME TEST CIRCUIT



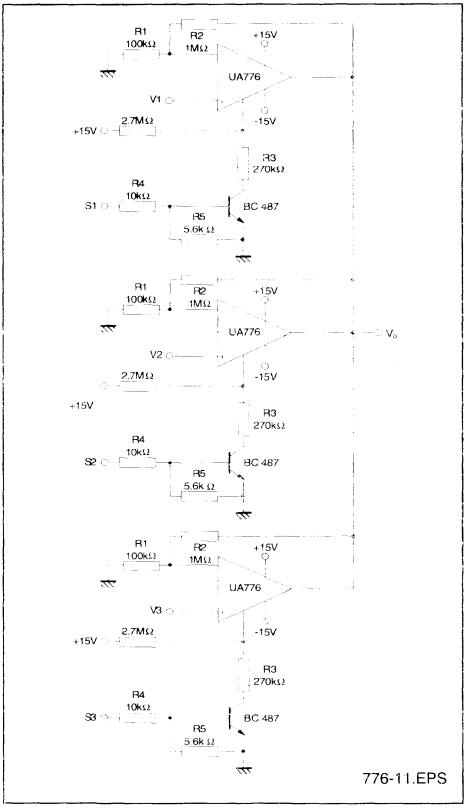
776-09.EPS

TYPICAL APPLICATIONS

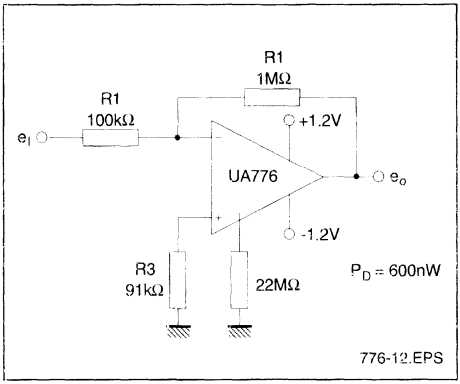
HIGH ACCURACY SAMPLE AND HOLD



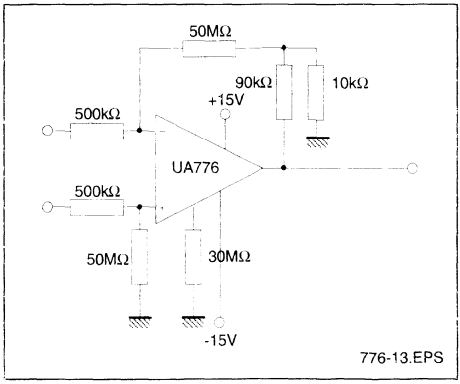
MULTIPLEXING AND SIGNAL CONDITIONING WITHOUT FETs



NANO-WATT AMPLIFIER



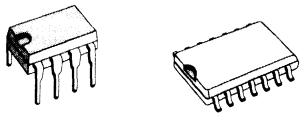
HIGH INPUT IMPEDANCE AMPLIFIER



CURRENT MODE PWM CONTROLLER

For complete specification refer to " Linear & Switching Voltage Regulators Appl. Manual ". (Order Code AMLISVOREST/1)

- OPTIMIZED FOR OFF-LINE AND DC TO DC CONVERTERS
- LOW START-UP CURRENT (< 1 mA)
- AUTOMATIC FEED FORWARD COMPENSATION
- PULSE-BY-PULSE CURRENT LIMITING
- ENHANCED LOAD RESPONSE CHARACTERISTICS
- UNDER-VOLTAGE LOCKOUT WITH HYSTERESIS
- DOUBLE PULSE SUPPRESSION
- HIGH CURRENT TOTEM POLE OUTPUT
- INTERNALLY TRIMMED BANDGAP REFERENCE
- 500 KHz OPERATION
- LOW R_O ERROR AMP



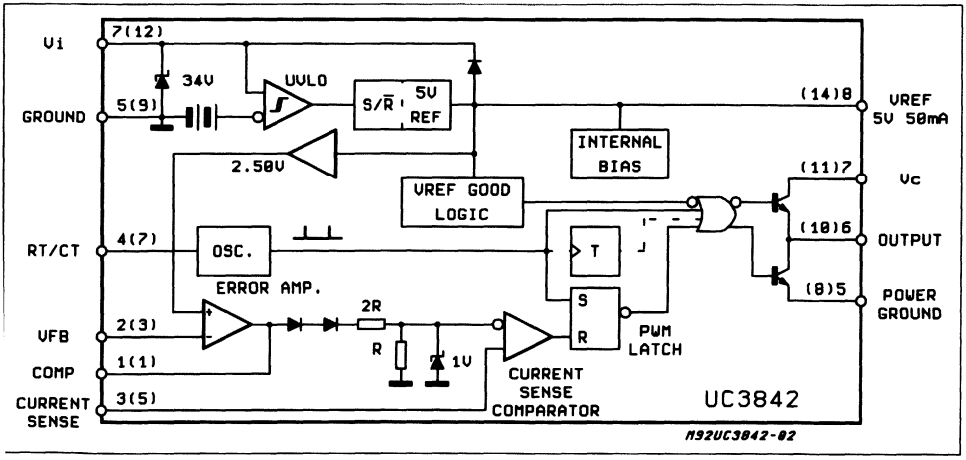
Minidip **SO-14**

DESCRIPTION

The UC3842/3/4/5 family of control ICs provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under voltage lockout featuring start-up current less than 1 mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N-Channel MOSFETs, is low in the off-state.

Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The UC3842 and UC3844 have UVLO thresholds of 16V (on) and 10V (off), ideally suited off-line applications The corresponding thresholds for the UC3843 and UC3845 are 8.5 V and 7.9 V. The UC3842 and UC3843 can operate to duty cycles approaching 100%. A range of the zero to < 50 % is obtained by the UC3844 and UC3845 by the addition of an internal toggle flip flop which blanks the output off every other clock cycle.

BLOCK DIAGRAM (toggle flip flop used only in U3844 and UC3845)



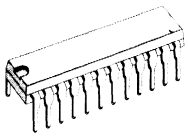
SGS-THOMSON MICROELECTRONICS

UDN2916A

STEPPER MOTOR DRIVER

ADVANCE DATA

- ABLE TO DRIVE BOTH WINDINGS OF BIPOLAR STEPPER MOTOR
- OUTPUT CURRENT UP TO 750mA EACH WINDING
- WIDE VOLTAGE RANGE 10V TO 50V
- HALF-STEP, FULL-STEP AND MICROSTEPPING MODE
- BUILT-IN PROTECTION DIODES
- INTERNAL PWM CURRENT CONTROL
- LOW OUTPUT SATURATION VOLTAGE
- DESIGNED FOR UNSTABILIZED MOTOR SUPPLY VOLTAGE
- INTERNAL THERMAL SHUTDOWN



Powerdip 20+2+2

ORDERING NUMBER: UDN2916A

DESCRIPTION

The UDN2916A is a bipolar monolithic integrated circuits intended to control and drive both winding of a bipolar stepper motor or bidirectionally control two DC motors.

The UDN2916A with a few external components form a complete control and drive circuit for LS-TTL or microprocessor controlled stepper motor system.

The power stage is a dual full bridge capable of sustaining 50V and including four diodes for current recirculation.

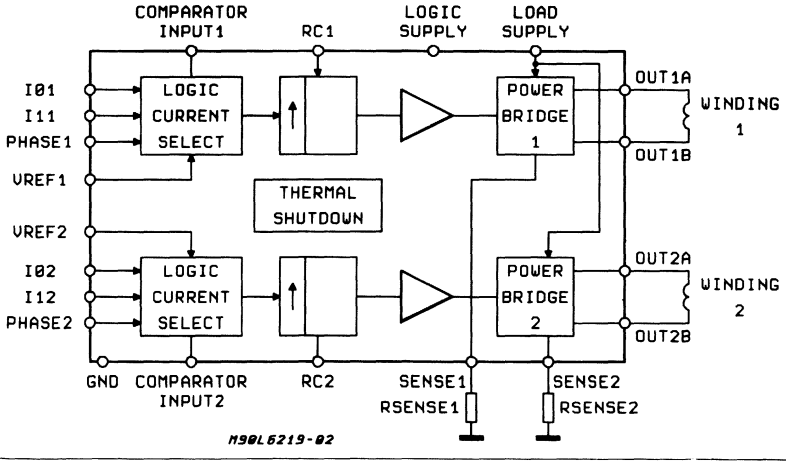
A cross conduction protection is provided to avoid simultaneous cross conduction during switching current direction.

An internal pulse-width-modulation (PWM) controls the output current to 750mA with peak start-up current up to 1A.

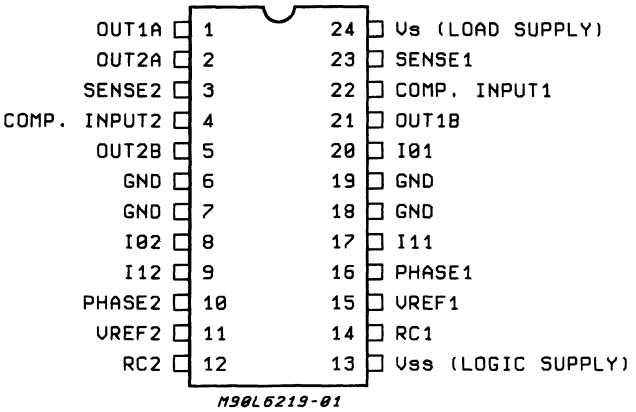
Wide range of current control from 750mA (each bridge) is permitted by means of two logic inputs and an external voltage reference. A phase input to each bridge determines the load current direction.

A thermal protection circuitry disables the outputs if the chip temperature exceeds safe operating limits.

BLOCK DIAGRAM



PIN CONNECTION (Top view)



PIN FUNCTIONS

N°	Name	Function
1;2	OUTPUT A	See pins 5;21
3;23	SENSE RESISTOR	Connection to Lower Emitters of Output Stage for Insertion of Current Sense Resistor
4;22	COMPARATOR INPUT	Input connected to the comparators. The voltage across the sense resistor is feedback to this input throught the low pass filter RC CC. The higher power transistors are disabled when the sense voltage exceeds the reference voltage of the selected comparator. When this occurs the current decays for a time set by R_T C_T (t_{off} = 1.1 R_T C_T). See fig. 1.
5;21	OUTPUT B	Output Connection. The output stage is a "H" bridge formed by four transistors and four diodes suitable for switching applications.
6;19	GROUND	See pins 7;18
7;18	GROUND	Ground Connection. With pins 6 and 19 also conducts heat from die to printed circuit copper.
8;20	INPUT 0	See INPUT 1 (pins 9;17)
9;17	INPUT 1	These pins and pins 8;20 (INPUT 0) are logic inputs which select the outputs of the comparators to set the current level. Current also depends on the sensing resistor and reference voltage. See Funcional Description.
10;16	PHASE	This TTL-compatible logic inputs sets the direction of current flow through the load. A high level causes current to flow from OUTPUT A (source) to OUTPUT B (sink). A schmitt trigger on this input provides good noise immunity and a delay circuit prevents output stage short circuits during switching.
11;15	REFERENCE VOLTAGE	A voltage applied to this pin sets the reference voltage of the comparators, this determining the output current (also thus depending on R_s and the two inputs INPUT 0 and INPUT 1).
12;14	RC	A parallel RC network connected to this pin sets the OFF time of the higher power transistors. The pulse generator is a monostable triggered by the output of the comparators (t_{off} = 1.1 R_T C_T).
13	V_{SS} - LOGIC SUPPLY	Supply Voltage Input for Logic Circuitry
24	V_S - LOAD SUPPLY	Supply Voltage Input for the Output Stages.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	50	V
I_o	Output Current (peak)	±1	A
I_o	Output Current (continuous)	±0.75	A
V_{SS}	Logic Supply Voltage	7	V
V_{IN}	Logic Input Voltage Range	-0.3 to +7	V
V_{sense}	Sense Output Voltage	1.5	V
T_J	Junction Temperature	+150	°C
T_{op}	Operating Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature Range	-55 to +150	°C

THERMAL DATA

Symbol	Description		Value	Unit
$R_{th(j\ case)}$	Thermal Resistance Junction-case	Max	14	°C/W
$R_{th(j\ ambient)}$	Thermal Resistance Junction-ambient	Max	60	°C/W

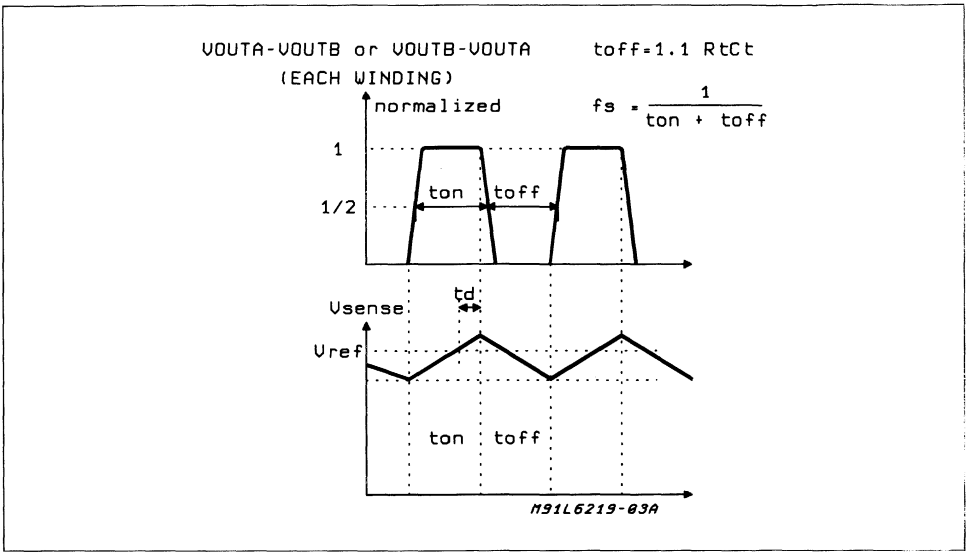
ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, $T_{tab} \leq 70$°C, V_S = 50V, V_{SS} = 4.75V to 5.25V, V_{REF} = 5V; unless otherwise specified) See fig. 3.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
OUTPUT DRIVERS (OUT_A or OUT_B)						
V_S	Motor Supply Range		10		50	V
I_{CEX}	Output Leakage Current	V_{OUT} = Vs V_{OUT} = 0	- -	<1 <-1	50 -50	µA µA
$V_{CE(sat)}$	Output Saturation Voltage	Sink Driver, I_{OUT} = +500mA Sink Driver, I_{OUT} = +750mA Source Driver, I_{OUT} = -500mA Source Driver, I_{OUT} = -750mA	- - - -	0.3 0.7 1.1 1.3	0.6 1 1.4 1.6	V V V V
I_R	Clamp Diode Leakage Current	V_R = 50V	-	<1	50	µA
V_F	Clamp Diode Forward Voltage	Sink Diode Source Diode I_F =750mA		1 1	1.5 1.5	V V
$I_{S(on)}$	Driver Supply Current	Both Bridges ON, No Load	-	8	15	mA
$I_{S(off)}$	Driver Supply Current	Both Bridges OFF	-	6	10	mA
CONTROL LOGIC						
$V_{IN(H)}$	Input Voltage	All Inputs	2.4	-	-	V
$V_{IN(L)}$	Input Voltage	All Inputs	-	-	0.8	V
$I_{IN(H)}$	Input Current	V_{IN} = 2.4V	-	<1	20	µA
$I_{IN(L)}$	Input Current	V_{IN} = 0.84V	-	-3	-200	µA
V_{REF}	Reference Voltage	Operating	1.5	-	7.5	V
$I_{SS(ON)}$	Total Logic Supply Current	I_o = I_1 = 0.8V, No Load	-	54	64	mA
$I_{SS(OFF)}$	Total Logic Supply Current	I_o = I_1 = 2.4V, No Load	-	10	14	mA
COMPARATORS						
V_{REF} / V_{sense}	Current Limit Threshold (at trip point	I_o = I_1 = 0.8V	9.5	10	10.5	-
		I_o = 2.4V, I_1 = 0.8V	13.5	15	16.5	-
		I_o = 0.8V, I_1 = 2.4V	25.5	30	34.5	-
t_{off}	Cutoff Time	R_t = 56KΩ C_t = 820pF	-	50		µs
t_d	Turn Off Delay	Fig. 1	-	1		µs

ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
PROTECTION						
T_J	Thermal Shutdown Temperature		-	170	-	°C

Figure 1



FUNCTIONAL DESCRIPTION

The circuit is intended to drive both windings of a bipolar stepper motor.

The peak current control is generated through switch mode regulation.

There is a choice of three different current levels with the two logic inputs I_{01} - I_{11} for winding 1 and I_{02} - I_{12} for winding 2.

The current can also be switched off completely

Input Logic (I_0 and I_1)

The current level in the motor winding is selected with these inputs. (See fig. 2)

If any of the logic inputs is left open, the circuit will treat it has a high level input.

I_0	I_1	Current Level
H	H	No Current
L	H	Low Current 1/3 I_0 max
H	L	Medium Current 2/3 I_0 max
L	L	Maximum Current I_0 max

Phase

This input determines the direction of current flow in the windings, depending on the motor connections. The signal is fed through a Schmidt-trigger for noise immunity, and through a time delay in order to guarantee that no short-circuit occurs in the output stage during phase-shift.

High level on the PHASE input causes the motor current flow from Out A through the winding to Out B

Current Sensor

This part contains a current sensing resistor (R_S), a low pass filter (R_C, C_C) and three comparators.

Only one comparator is active at a time. It is activated by the input logic according to the current level chosen with signals I_0 and I_1.

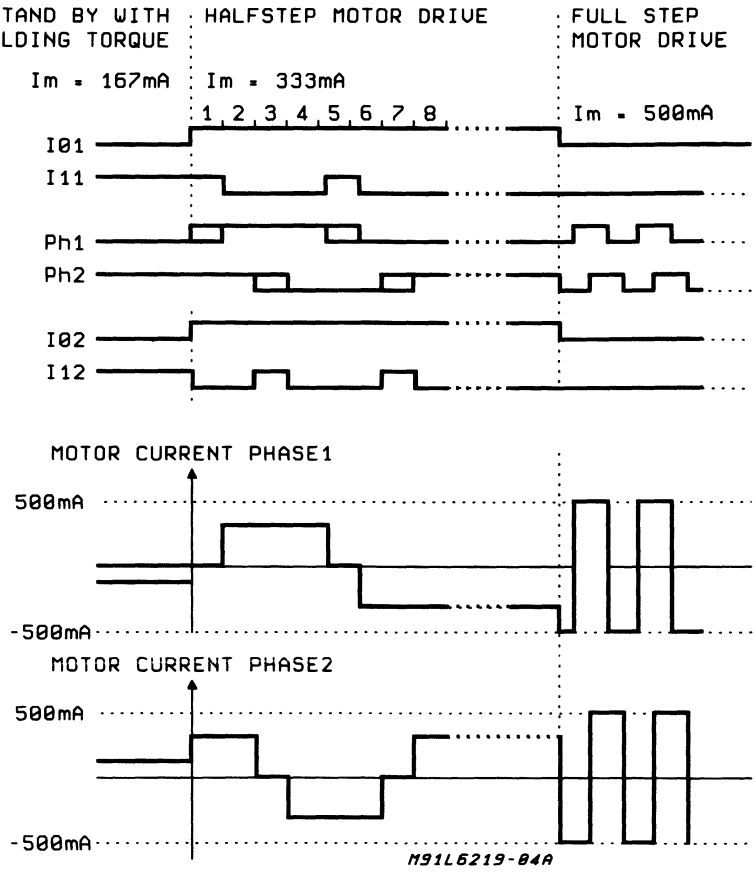
The motor current flows through the sensing resistor R_S.

When the current has increased so that the voltage across R_S becomes higher than the reference voltage on the other comparator input, the comparator goes high, which triggers the pulse generator.

The max peak current I_{max} can be defined by:

$$I_{max} = \frac{V_{ref}}{10\ R_s}$$

Figure 2: Principle Operating Sequence



Single-pulse Generator

The pulse generator is a monostable triggered on the positive going edge of the comparator output. The monostable output is high during the pulse time, t_{off} , which is determined by the time components R_t and C_t.

$$t_{off} = 1.1 \cdot R_t C_t$$

The single pulse switches off the power feed to the motor winding, causing the winding current to decrease during t_{off}.
If a new trigger signal should occur during t_{off}, it is ignored.

Output Stage

The output stage contains four Darlington transistors (source drivers) four saturated transistors (sink drivers) and eight diodes, connected in two H bridge.
The source transistors are used to switch the power supplied to the motor winding, thus driving a constant current through the winding.
It should be noted however, that is not permitted to short circuit the outputs.
Internal circuitry is added in order to increse the accuracy of the motor current particularly with low current levels.

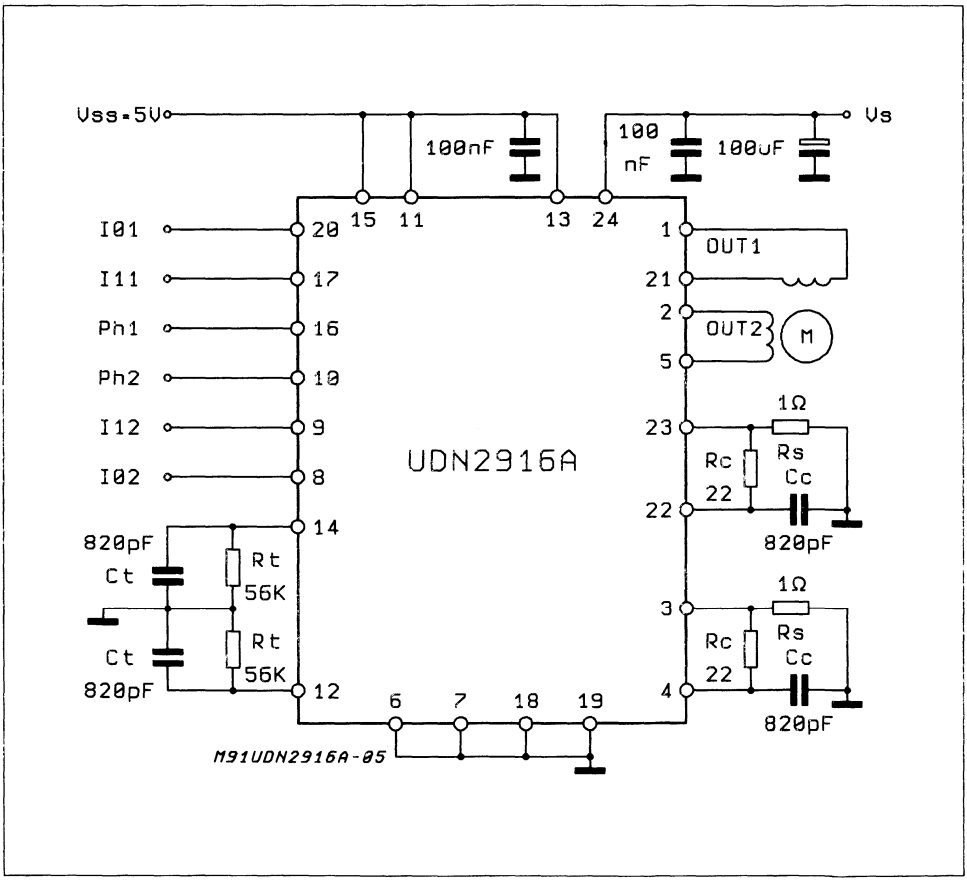
V_S, V_{SS}, V_{Ref}
The circuit will stand any order of turn-on or turn-off the supply voltages V_S and V_{SS}. Normal dV/dt values are then assumed.
Preferably, V_{Ref} should be tracking V_{SS} during power-on and power-off if V_S is established.

APPLICATION INFORMATIONS (Note 1)
Some stepper motors are not designed for continuous operation at maximum current. As the circuit drives a constant current through the motor, its temperature might increase exceedingly both at low and high speed operation.
Also, some stepper motors have such high core losses that they are not suited for switch mode current regulation.
Unused inputs should be connected to proper voltage levels in order to get the highest noise immunity.

As the circuit operates with switch mode current regulation, interference generation problems might arise in some applications. A good measure might then be to decouple the circuit with a 100nF capacitor, located near the package between power line and ground.
The ground lead between R_S, and circuit GND should be kept as short as possible.
A typical Application Circuit is shown in Fig. 3.
Note that C_t must be NPO type or similar else.
To sense the winding current, paralleled metal film resistors are recommended (R_S)

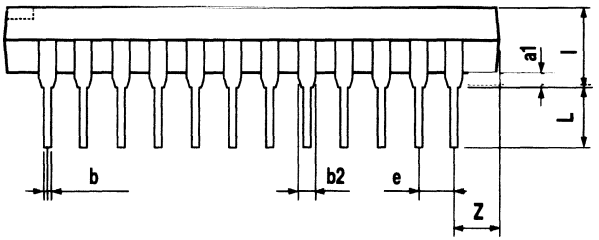
Note 1 - Other information is available as "Smart Power Development System": HWPC2916A.

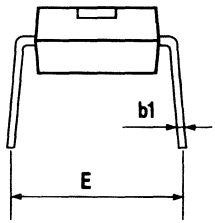
Figure 3: Typical Application Circuit.

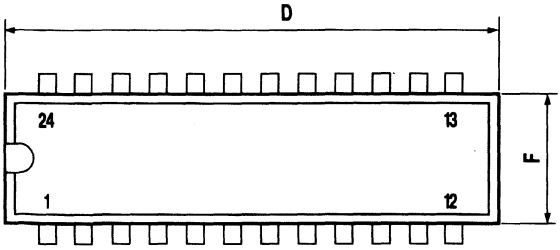


DIP24 (20+2+2) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.38			0.015		
b	0.41		0.51	0.016		0.020
b1	0.20	0.25	0.30	0.008	0.010	0.012
b2	1.40	1.52	1.65	0.055	0.060	0.065
D			30.23			1.19
E		7.62			0.300	
e		2.54			0.100	
F			6.86			0.270
I			4.32			0.170
L	3.18			0.125		







SGS-THOMSON MICROELECTRONICS

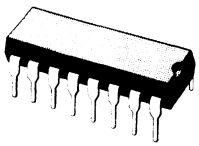
ULN2001A-ULN2003A
ULN2002A-ULN2004A

SEVEN DARLINGTON ARRAYS

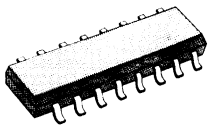
- SEVEN DARLINGTONS PER PACKAGE
- OUTPUT CURRENT 500 mA PER DRIVER (600 mA PEAK)
- OUTPUT VOLTAGE 50 V
- INTEGRAL SUPPRESSION DIODES FOR INDUCTIVE LOADS
- OUTPUTS CAN BE PARALLELED FOR HIGHER CURRENT
- TTL/CMOS/PMOS/DTL COMPATIBLE INPUTS
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY LAYOUT

These versatile devices are useful for driving a wide range of loads including solenoids, relays DC motors, LED displays filament lamps, thermal printheads and high power buffers.

The ULN2001A/2002A/2003A and 2004A are supplied in 16 pin plastic DIP packages with a copper leadframe to reduce thermal resistance. They are available also in small outline package (SO-16) as ULN2001D/2002D/2003D/2004D.



DIP-16 Plastic
(0.25)



SO-16J

ORDER CODES :
ULN2001A/2A/3A/4A (DIP-16)
ULN2001D/2D/3D/4D (SO-16)

DESCRIPTION

The ULN2001A, ULN2002A, ULN2003 and ULN2004A are high voltage, high current darlington arrays each containing seven open collector darlington pairs with common emitters. Each channel is rated at 500 mA and can withstand peak currents of 600 mA. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout.

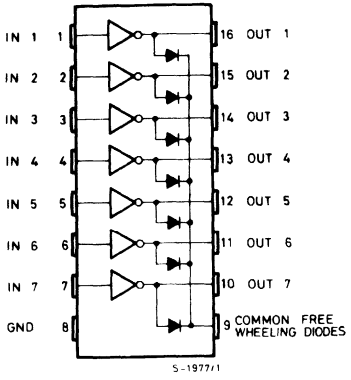
The four versions interface to all common logic families :

ULN2001A	General Purpose. DTL. TTL. PMOS. CMOS
ULN2002A	14-25 V PMOS
ULN2003A	5 V TTL. CMOS
ULN2004A	6–15 V CMOS. PMOS

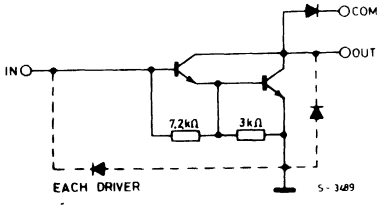
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_o	Output Voltage	50	V
V_{in}	Input Voltage (for ULN2002A/D - 2003A/D - 2004A/D)	30	V
I_c	Continuous Collector Current	500	mA
I_b	Continuous Base Current	25	mA
T_{amb}	Operating Ambient Temperature Range	– 20 to 85	C
T_{stg}	Storage Temperature Range	– 55 to 150	C
T_j	Junction Temperature	150	C

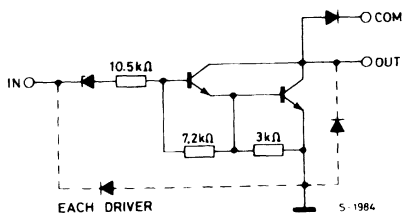
PIN CONNECTION



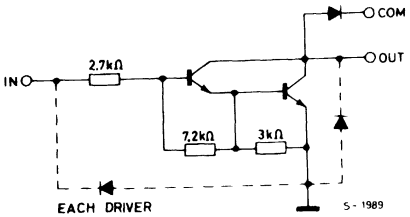
SCHEMATIC DIAGRAM



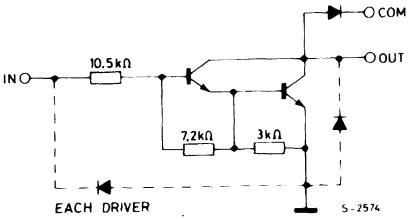
Series ULN-2001A
(each driver)



Series ULN-2002A
(each driver)



Series ULN-2003A
(each driver)



Series ULN-2004A
(each driver)

THERMAL DATA

			DIP–16	SO–16
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	70 °C/W	165 °C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	V_{CE} = 50 V			50	µA	1a
		T_{amb} = 70 °C V_{CE} = 50 V			100	µA	1a
		T_{amb} = 70 °C for **ULN2002A**					
		V_{CE} = 50 V V_i = 6 V for **ULN2004A**			500	µA	1b
		V_{CE} = 50 V V_i = 1 V			500	µA	1b
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 100 mA I_B = 250 µA		0.9	1.1	V	2
		I_C = 200 mA I_B = 350 µA		1.1	1.3	V	2
		I_C = 350 mA I_B = 500 µA		1.3	1.6	V	2
$I_{i(on)}$	Input Current	for **ULN2002A** V_i = 17 V		0.82	1.25	mA	3
		for **ULN2003A** V_i = 3.85 V		0.93	1.35	mA	3
		for **ULN2004A** V_i = 5 V		0.35	0.5	mA	3
		V_i = 12 V		1	1.45	mA	3
$I_{i(off)}$	Input Current	T_{amb} = 70 °C I_C = 500 µA	50	65		µA	4
$V_{i(on)}$	Input Voltage	for **ULN2002A**					
		V_{CE} = 2 V I_C = 300 mA			13	V	5
		for **ULN2003A**					
		V_{CE} = 2 V I_C = 200 mA			2.4	V	5
		V_{CE} = 2 V I_C = 250 mA			2.7	V	5
		V_{CE} = 2 V I_C = 300 mA			3	V	5
		for **ULN2004A**					
		V_{CE} = 2 V I_C = 125 mA			5	V	5
		V_{CE} = 2 V I_C = 200 mA			6	V	5
		V_{CE} = 2 V I_C = 275 mA			7	V	5
		V_{CE} = 2 V I_C = 350 mA			8	V	5
h_{FE}	DC Forward Current Gain	for **ULN2001A**					
		V_{CE} = 2 V I_C = 350 mA	1000			–	2
C_i	Input Capacitance			15	25	pF	–
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o		0.25	1	µs	–
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o		0.25	1	µs	–
I_R	Clamp Diode Leakage Current	V_R = 50 V			50	µA	6
		T_{amb} = 70 °C V_R = 50 V			100	µA	6
V_F	Clamp Diode Forward Voltage	I_F = 350 mA		1.7	2	V	7

TEST CIRCUITS

Figure 1a.

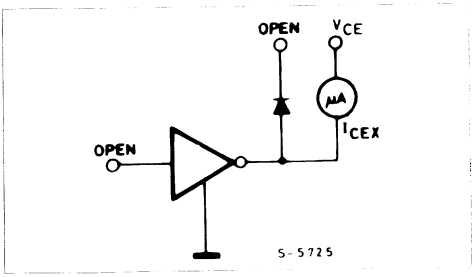


Figure 1b.

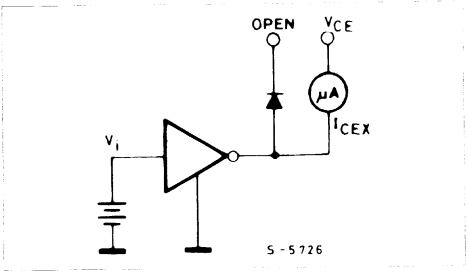


Figure 2.

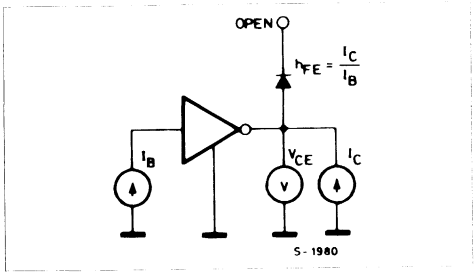


Figure 3.

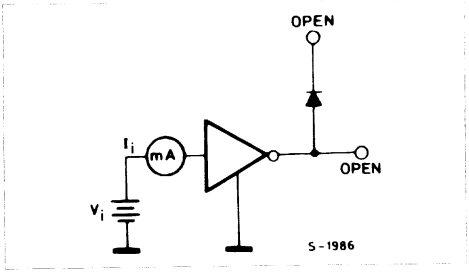


Figure 4.

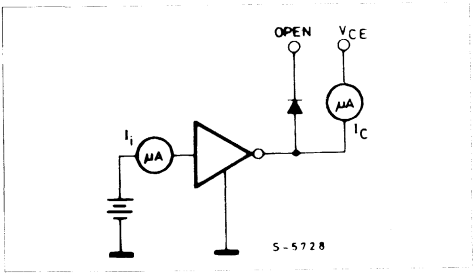


Figure 5.

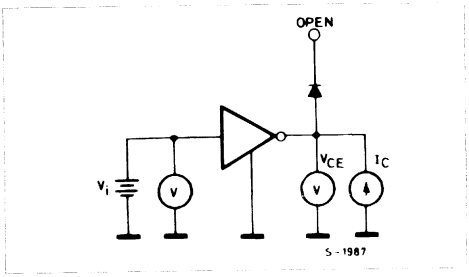


Figure 6.

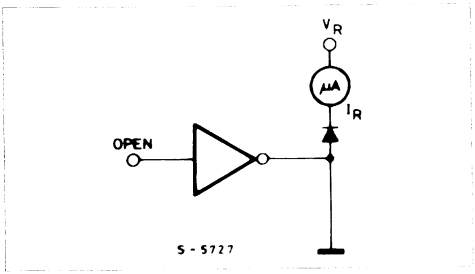
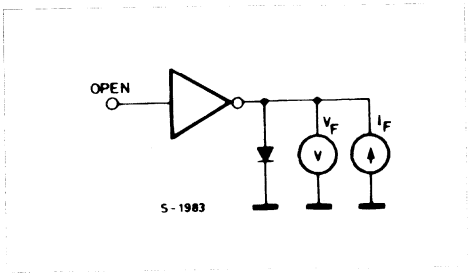


Figure 7.



SGS-THOMSON MICROELECTRONICS

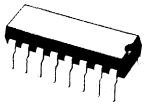
ULN2064B ULN2070B
ULN2066B ULN2074B
ULN2068B ULN2076B

50 V - 1.5 A QUAD DARLINGTON SWITCHES

- OUTPUT CURRENT TO 1.5 A EACH DARLINGTON
- MINIMUM BREAKDOWN 50 V
- SUSTAINING VOLTAGE AT LEAST 35 V
- INTEGRAL SUPPRESSION DIODES (ULN2064B, ULN2066B, ULN2068B and ULN2070B)
- ISOLATED DARLINGTON PINOUT (ULN2074B, ULN2076B)
- VERSIONS COMPATIBLE WITH ALL POPULAR LOGIC FAMILIES

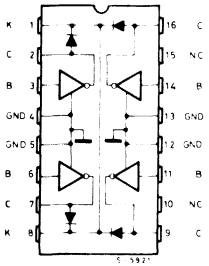
DESCRIPTION

Designed to interface logic to a wide variety of high current, high voltage loads, these devices each contain four NPN darlington switches delivering up to 1.5 A with a specified minimum breakdown of 50 V and a sustaining voltage of 35 V measured at 100 mA. The ULN2064B, ULN2066B, ULN2068B and ULN2070B contain integral suppression diodes for inductive loads have common emitters. The ULN2074B and ULN2076B feature isolated darlington pinouts and are intended for applications such as emitter follower configurations. Inputs of the ULN2064B, ULN2068B and ULN2074B are compatible with popular 5 V logic families and the ULN2066B and ULN2076B are compatible with 6-15 V CMOS and PMOS. Types ULN2068B and ULN2070B include a predriver stage to reduce loading on the control logic.

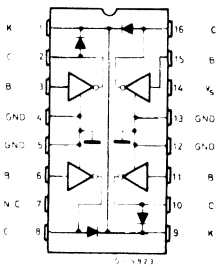


POWERDIP
12 + 2 + 2

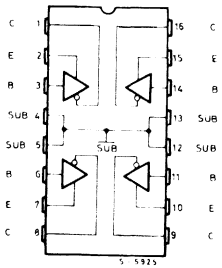
PIN CONNECTIONS (top view) and ORDER CODES



ULN2064B
ULN2068B



ULN2068B
ULN2070B

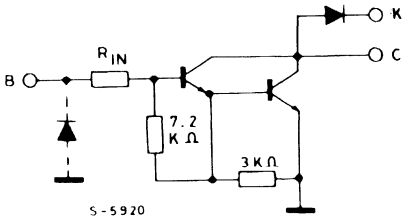


ULN2074B
ULN2076B

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CEX}	Output Voltage	50	V
$V_{CE(sus)}$	Output Sustaining Voltage	35	V
I_o	Output Current	1.75	A
V_i	Input Voltage for **ULN2066B/70B/74B/76B** for **ULN2064B/68B**	30 15	V V
I_i	Input Current	25	mA
V_s	Supply Voltage for **ULN2068B** for **ULN2070B**	10 20	V V
P_{tot}	Power Dissipation : at T_{amb} = 90 °C at T_{amb} = 70 °C	4.3 1	W W
T_{amb}	Operating Ambient Temperature Range	– 20 to 85	°C
T_{stg}	Storage Temperature	– 55 to 150	°C

SCHEMATIC DIAGRAM



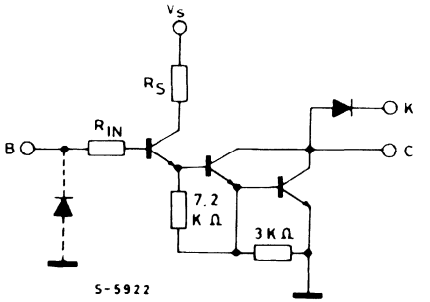
ULN2064B : R_{IN} = 35 Ω
ULN2066B : R_{IN} = 3 kΩ

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig
I_{CEX}	Output Leakage Current	for **ULN2064B – ULN2066B**					
		V_{CE} = 50 V			100	µA	1
		V_{CE} = 50 V T_{amb} = 70 °C			500	µA	
$V_{CE(sus)}$	Collector-emitter Sustaining Voltage	for **ULN2064B – ULN2066B** I_C = 100 mA V_i = 0.4 V	35			V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 500 mA I_B = 625 µA			1.1	V	3
		I_C = 750 mA I_B = 935 µA			1.2	V	
		I_C = 1 A I_B = 1.25 mA			1.3	V	
		I_C = 1.25 A I_B = 2 mA			1.4	V	
$I_{i(on)}$	Input Current	for **ULN2064B** V_i = 2.4 V	1.4		4.3	mA	4
		for **ULN2064B** V_i = 3.75 V	3.3		9.6	mA	
		for **ULN2066B** V_i = 5 V	0.6		1.8	mA	
		for **ULN2066B** V_i = 12 V	1.7		5.2	mA	
$V_{i(on)}$	Input Voltage	for **ULN2064B**					5
		V_{CE} = 2 V I_C = 1 A			2	V	
		V_{CE} = 2 V I_C = 1.5 A			2.5	V	
		for **ULN2066B**					
		V_{CE} = 2 V I_C = 1 A			6.5	V	
		V_{CE} = 2 V I_C = 1.5 A			10	V	
t_{PLH}	Turn – on Delay Time	0.5 V_i to 0.5 V_o			1	µs	
t_{PHL}	Turn – off Delay Time	0.5 V_i to 0.5 V_o			1.5	µs	
I_R	Clamp Diode Leakage Current	for **ULN2064B – ULN2066B**					6
		V_R = 80 V			50	µA	
		V_R = 80 V T_{amb} = 70 °C			100	µA	
V_F	Clamp Diode Forward Voltage	I_F = 1 A			1.75	V	7
		I_F = 1.5 A			2	V	

Notes : 1. Input voltage is with reference to the substrate (no connection to any other pins) for the ULN2074B and ULN2076B reference is ground for all other types.
2. Input current may be limited by maximum allowable input voltage.

SCHEMATIC DIAGRAM

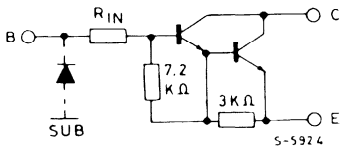


ULN2068B : R_{IN} = 2.5 kΩ R_s = 900 Ω
ULN2070B : R_{IN} = 11.6 kΩ R_s = 3.4 KHΩ

ELECTRICAL CHARACTERISTICS (V_s = 5 V for ULN2068B, V_s = 12 V for ULN2070B, T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig
I_{CEX}	Output Leakage Current	for **ULN2068B – ULN2070B**					
		V_{CE} = 50 V			100	µA	1
		V_{CE} = 50 V T_{amb} = 70 °C			500	µA	
$V_{CE(sus)}$	Collector-emitter Sustaining Voltage	for **ULN2068B – ULN2070B** I_C = 100 mA V_I = 0.4 V	35			V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	for **ULN2068B**					
		I_C = 500 mA V_I = 2.75 V			1.1	V	
		I_C = 750 mA V_I = 2.75 V			1.2	V	
		I_C = 1 A V_I = 2.75 V			1.3	V	
		I_C = 1.25 A V_I = 2.75 V			1.4	V	2
		for **ULN2070B**					
		I_B = 500 mA V_I = 5 V			1.1	V	
		I_B = 750 mA V_I = 5 V			1.2	V	
		I_B = 1 A V_I = 5 V			1.3	V	
		I_B = 1.25 A V_I = 5 V			1.4	V	
$I_{I(on)}$	Input Current	for **ULN2068B** V_I = 2.75 V			550	µA	
		for **ULN2068B** V_I = 3.75 V			1000	µA	
		for **ULN2070B** V_I = 5 V			400	µA	4
		for **ULN2070B** V_I = 12 V			1250	µA	
$V_{I(on)}$	Input Voltage	V_{CE} = 2 V I_C = 1.5 A					
		for **ULN2068B**			2.75	V	5
		for **ULN2070B**			5	V	
I_S	Supply Current	for **ULN2068B**					
		I_C = 500 mA V_I = 2.75 V			6	mA	
		for **ULN2070B**					8
		I_C = 500 mA V_I = 5 V			4.5	mA	
t_{PLH}	Turn-on Delay Time	0.5 V_I to 0.5 V_o			1	µs	
t_{PHL}	Turn-off Delay Time	0.5 V_I to 0.5 V_o I_C = 1.25 A			1.5	µs	
I_R	Clamp Diode Leakage Current	for **ULN2068B – ULN2070B**					
		V_R = 50 V			50	µA	6
		V_R = 50 V T_{amb} = 70 °C			100	µA	
V_F	Clamp Diode Forward Voltage	I_F = 1 A			1.75	V	7
		I_F = 1.5 A			2	V	

SCHEMATIC DIAGRAM



ULN2074B : R_{IN} = 350 Ω
ULN2076B : R_{IN} = 3 kΩ

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig
I_{CEX}	Output Leakage Current	for **ULN2074B – ULN2076B**					
		V_{CE} = 50 V			100	µA	1
		V_{CE} = 50 V T_{amb} = 70 °C			500	µA	
$V_{CE(sust)}$	Collector-emitter Sustaining Voltage	for **ULN2074B – ULN2076B** I_C = 100 mA V_i = 0.4 V	35			V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 500 mA I_B = 625 µA			1.1	V	3
		I_C = 750 mA I_B = 935 µA			1.2	V	
		I_C = 1 A I_B = 1.25 mA			1.3	V	
		I_C = 1.25 A I_B = 2 mA			1.4	V	
$I_{i(on)}$	Input Current	for **ULN2074B** V_i = 2.4 V	1.4		4.3	mA	4
		for **ULN2074B** V_i = 3.75 V	3.3		9.6	mA	
		for **ULN2076B** V_i = 5 V	0.6		1.8	mA	
		for **ULN2076B** V_i = 12 V	1.7		5.2	mA	
$V_{i(on)}$	Input Voltage	for **ULN2074B**					5
		V_{CE} = 2 V I_C = 1 A			2	V	
		V_{CE} = 2 V I_C = 1.5 A			2.5	V	
		for **ULN2076B**					
		V_{CE} = 2 V I_C = 1 A			6.5	V	
		V_{CE} = 2 V I_C = 1.5 A			10	V	
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o			1	µs	
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o			1.5	µs	

TEST CIRCUITS

Figure 1.

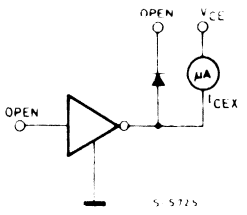


Figure 2.

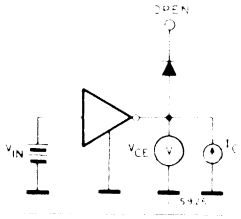


Figure 3.

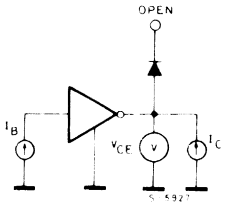


Figure 4.

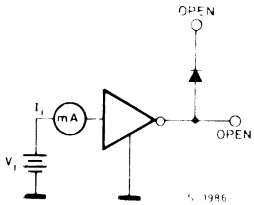


Figure 5.

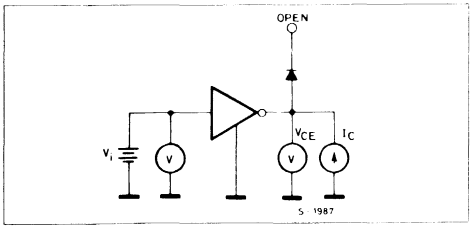


Figure 6.

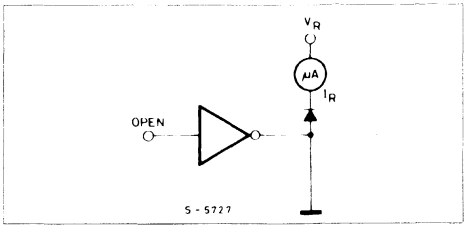


Figure 7.

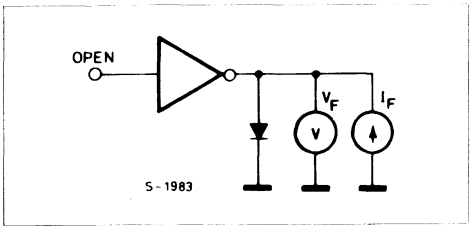


Figure 8.

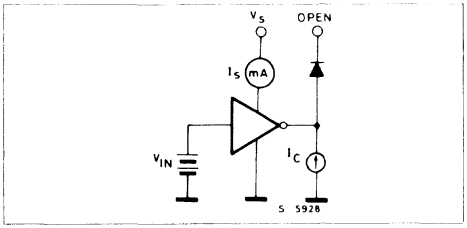


Figure 9 : Input Current as a Function of Input Voltage.

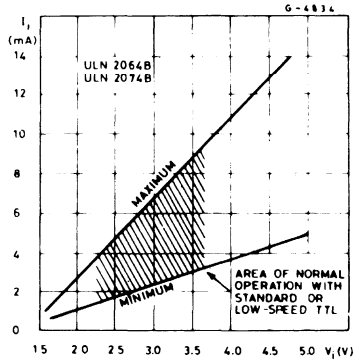


Figure 10 : Input Current as a Function of Input Voltage.

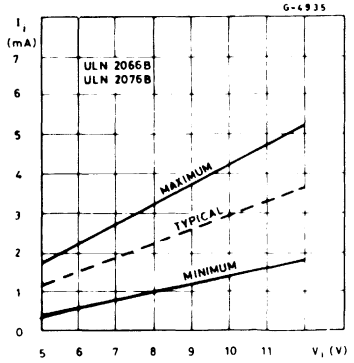
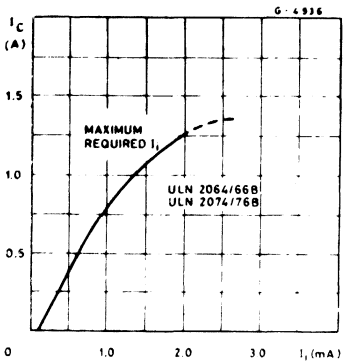


Figure 11 : Collector Current as a Function of Input Current.



TYPICAL APPLICATIONS

Figure 12 : Common-anode LED Drivers.

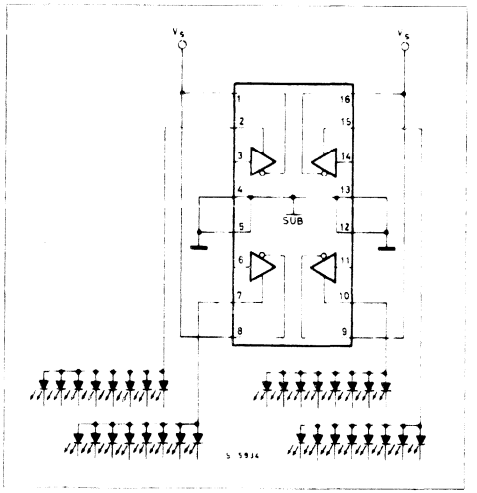
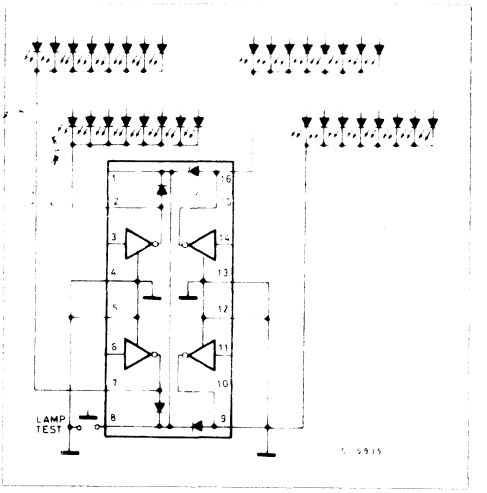


Figure 13 : Common-cathode LED Drivers.



MOUNTING INSTRUCTIONS

The $R_{th\ j\text{-}amb}$ can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 14) or to an external heatsink (Fig. 15).

The diagram of figure 16 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side "α" of two equal square copper areas having a thickness of 35 µ (1.4 mils).

During soldering the pins temperature must not exceed 260 °C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 14 : Example of P.C. Board Copper Area which is Used as Heatsink.

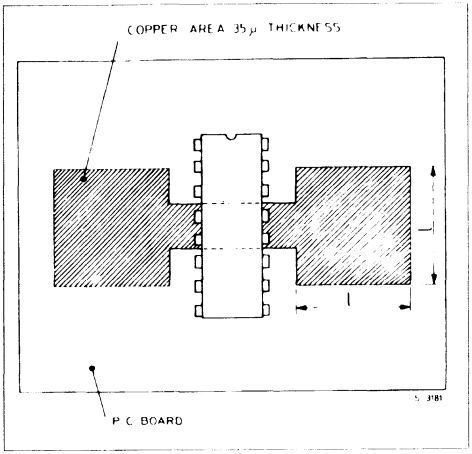


Figure 15 : External Heatsink Mounting Example.

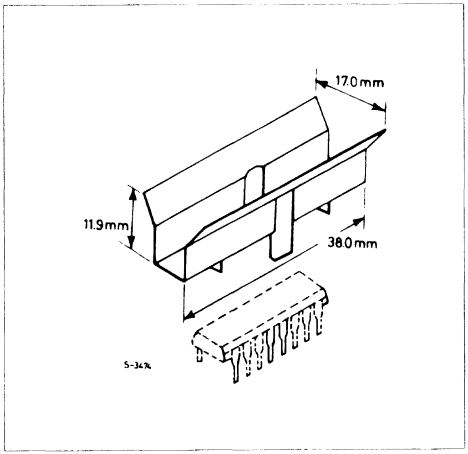


Figure 16 : Maximum Dissipable Power and Junction to Ambient Thermal Resistance vs. Side "α".

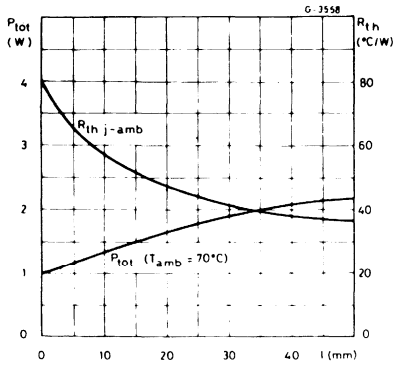
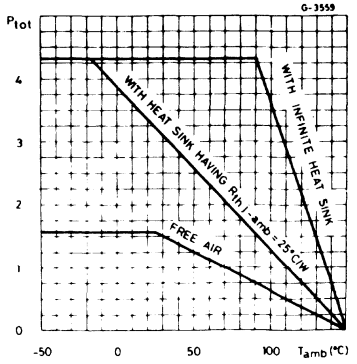


Figure 17 : Maximum Allowable Power Dissipation vs. Ambient Temperature.



SGS-THOMSON MICROELECTRONICS

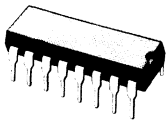
ULN2065B ULN2067B ULN2069B ULN2071B ULN2075B ULN2077B

80 V - 1.5 A QUAD DARLINGTON SWITCHES

- OUTPUT CURRENT TO 1.5 A EACH DARLINGTON
- MINIMUM BREAKDOWN 80 V
- SUSTAINING VOLTAGE AT LEAST 50 V
- INTEGRAL SUPPRESSION DIODES (ULN2065B, ULN2067B, ULN2069B and ULN2071B)
- ISOLATED DARLINGTON PINOUT (ULN2075B and ULN2077B)
- VERSIONS COMPATIBLE WITH ALL POPULAR LOGIC FAMILIES

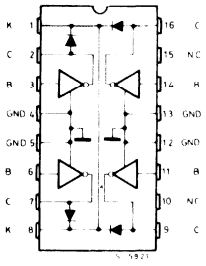
DESCRIPTION

Designed to interface logic to a wide variety of high current, high voltage loads, these devices each contain four NPN darlington switches delivering up to 1.5 A with a specified minimum breakdown of 80 V and a sustaining voltage of 50 V. The ULN2065B, ULN2067B, ULN2069B and ULN2071B contain integral suppression diodes for inductive loads and have common emitters ; the ULN2075B and ULN2077B feature isolated darlington pinouts and are intended for applications such as emitter follower configurations. Inputs of the ULN2065B, ULN2069B and ULN2075B are compatible with popular 5 V logic families and the ULN2067B, ULN2071B and ULN2077B are compatible with 6-15 VCMOS and PMOS. The ULN2069B and ULN2071B include a predriver stage to provide extragain, reducing the load on control logic.

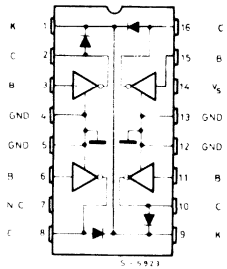


POWERDIP
12 + 2 + 2

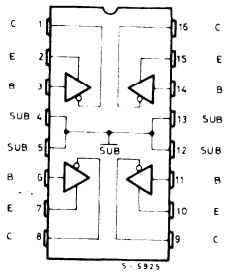
PIN CONNECTIONS AND ORDER CODES



ULN2065B
ULN2067B



ULN2069B
ULN2071B

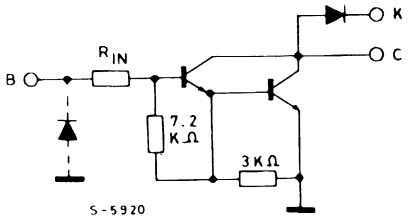


ULN2075B
ULN2077B

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CEX}	Output Voltage	80	V
$V_{CE(sus)}$	Output Sustaining Voltage	50	V
I_O	Output Current	1.75	A
V_i	Input Voltage for **ULN2075B – 2077B**	60	V
	for **ULN2067B – 2071B**	30	V
	for **ULN2065B – 2069B**	15	V
I_i	Input Current	25	mA
V_s	Supply Voltage for **ULN2069B**	10	V
	for **ULN2071B**	20	V
P_{tot}	Power Dissipation : at T_{pins} = 90 °C	4.3	W
	at T_{amb} = 70 °C	1	W
T_{amb}	Operating Ambient Temperature Range	– 20 to 85	°C
T_{stg}	Storage Temperature	– 55 to 150	°C

SCHEMATIC DIAGRAM



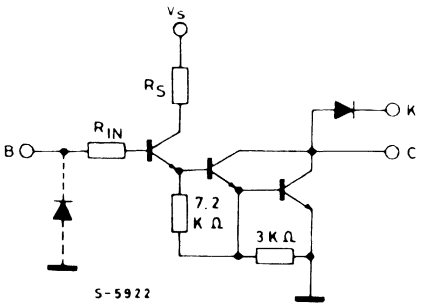
ULN2065B : R_{IN} = 350 Ω
ULN2067B : R_{IN} = 3 kΩ

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	for **ULN2065B – ULN2067B**					
		V_{CE} = 80 V			100	µA	1
		V_{CE} = 80 V T_{amb} = 70 °C			500	µA	
$V_{CE(sus)}$	Collector-emitter Sustaining Voltage	for **ULN2065B – ULN2067B** I_C = 100 mA V_i = 0.4 V	50			V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 500 mA I_B = 625 µA			1.1	V	3
		I_C = 750 mA I_B = 935 µA			1.2	V	
		I_C = 1 A I_B = 1.25 mA			1.3	V	
		I_C = 1.25 A I_B = 2 mA			1.4	V	
		for **ULN2065B – ULN2067B**					
		I_C = 1.5 A I_B = 2.25 mA			1.5	V	
$I_{i(on)}$	Input Current	for **ULN2065B** V_i = 2.4 V	1.4		4.3	mA	4
		for **ULN2065B** V_i = 3.75 V	3.3		9.6	mA	
		for **ULN2067B** V_i = 5 V	0.6		1.8	mA	
		for **ULN2067B** V_i = 12 V	1.7		5.2	mA	
$V_{i(on)}$	Input Voltage	for **ULN2065B**					5
		V_{CE} = 2 V I_C = 1 A			2	V	
		V_{CE} = 2 V I_C = 1.5 A			2.5	V	
		for **ULN2067B**					
		V_{CE} = 2 V I_C = 1 A			6.5	V	
		V_{CE} = 2 V I_C = 1.5 A			10	V	
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o			1	µs	
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o			1.5	µs	
I_R	Clamp Diode Leakage Current	for **ULN2065B – ULN2067B**					
		V_R = 80 V			50	µA	6
		V_R = 80 V T_{amb} = 70 °C			100	µA	
V_F	Clamp Diode Forward Voltage	I_F = 1 A			1.75	V	7
		I_F = 1.5 A			2	V	

Notes : 1. Input voltage is with reference to the substrate (no connection to any other pins) for the ULN2075B and ULN2077B reference is ground for all other types.
2. Input current may be limited by maximum allowable input voltage.

SCHEMATIC DIAGRAM

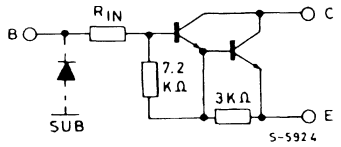


ULN2069B : R_{IN} = 2.5 KΩ, R_S = 900 Ω
ULN2071B : R_{IN} = 11.6 KΩ, R_S = 3.4 KΩ

ELECTRICAL CHARACTERISTICS (V_s = 5 V for ULN2069B, V_s = 12 V for ULN2071B, T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	for **ULN2069B – ULN2071B**					
		V_{CE} = 80 V			100	µA	1
		V_{CE} = 80 V T_{amb} = 70 °C			500	µA	
$V_{CE(sus)}$	Collector-emitter Sustaining Voltage	for **ULN2069B – ULN2071B**					
		I_C = 100 mA V_i = 0.4 V	50			V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	for **ULN2069B**					
		I_C = 500 mA V_i = 2.75 V			1.1	V	2
		I_C = 750 mA V_i = 2.75 V			1.2	V	
		I_C = 1 A V_i = 2.75 V			1.3	V	
		I_C = 1.25 A V_i = 2.75 V			1.4	V	
		I_C = 1.5 A V_i = 2.75 V			1.5	V	
		for **ULN2071B**					
		I_C = 500 mA V_i = 5 V			1.1	V	
		I_C = 750 mA V_i = 5 V			1.2	V	
		I_C = 1 A V_i = 5 V			1.3	V	
		I_C = 1.25 A V_i = 5 V			1.4	V	
		I_C = 1.5 A V_i = 5 V			1.5	V	
$I_{i(on)}$	Input Current	for **ULN2069B** V_i = 2.75 V			550	µA	4
		for **ULN2069B** V_i = 3.75 V			1000	µA	
		for **ULN2071B** V_i = 5 V			400	µA	
		for **ULN2071B** V_i = 12 V			1250	µA	
$V_{i(on)}$	Input Voltage	V_{CE} = 2 V I_C = 1.5 A					
		for **ULN2069B**			2.75	V	5
		for **ULN2071B**			5		
I_s	Supply Current	for **ULN2069B**					
		I_C = 500 mA V_i = 2.75 V			6	mA	8
		for **ULN2071B**					
		I_C = 500 mA V_i = 5 V			4.5	mA	
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o			1	µs	
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o I_C = 1.25 A			1.5	µs	
I_R	Clamp Diode Leakage Current	for **ULN2069B – ULN2071B**					
		V_R = 80 V			50	µA	6
		V_R = 80 V T_{amb} = 70 °C			100	µA	
V_F	Clamp Diode Forward Voltage	I_F = 1 A			1.75	V	7
		I_F = 1.5 A			2	V	

SCHEMATIC DIAGRAM



ULN2075B : R_{IN} = 350 Ω
ULN2077B : R_{IN} = 3 kΩ

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	for **ULN2075B – ULN2077B**					
		V_{CE} = 80 V			100	µA	
		V_{CE} = 80 V T_{amb} = 70 °C			500	µA	1
$V_{CE(sus)}$	Collector-emitter Sustaining Voltage	for **ULN2075B – ULN2077B** I_C = 100 mA V_i = 0.4 V	50			V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 500 mA I_B = 625 µA			1.1	V	3
		I_C = 750 mA I_B = 935 µA			1.2	V	
		I_C = 1 A I_B = 1.25 mA			1.3	V	
		I_C = 1.25 A I_B = 2 mA			1.4	V	
		for **ULN2075B – ULN2077B**					
		I_C = 1.5 A I_B = 2.25 mA			1.5	V	
$I_{i(on)}$	Input Current	for **ULN2075B** V_i = 2.4 V	1.4		4.3	mA	4
		for **ULN2075B** V_i = 3.75 V	3.3		9.6	mA	
		for **ULN2077B** V_i = 5 V	0.6		1.8	mA	
		for **ULN2077B** V_i = 12 V	1.7		5.2	mA	
$V_{i(on)}$	Input Voltage	for **ULN2075B**					5
		V_{CE} = 2 V I_C = 1 A			2	V	
		V_{CE} = 2 V I_C = 1.5 A			2.5	V	
		for **ULN2077B**					
		V_{CE} = 2 V I_C = 1 A			6.5	V	
		V_{CE} = 2 V I_C = 1.5 A			10	V	
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o			1	µs	
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o			1.5	µs	

TEST CIRCUITS

Figure 1.

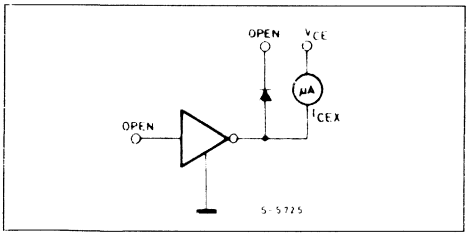


Figure 2.

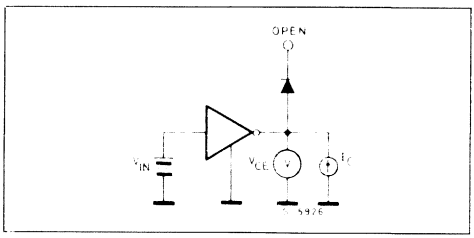


Figure 3.

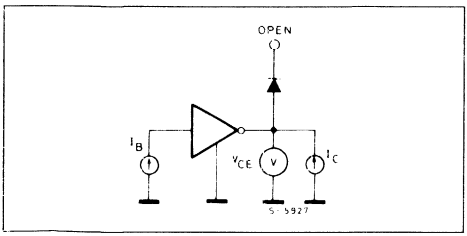


Figure 4.

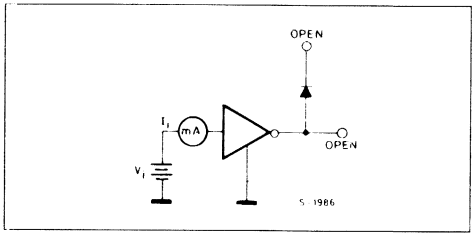


Figure 5.

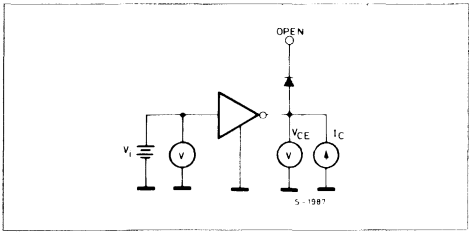


Figure 6.

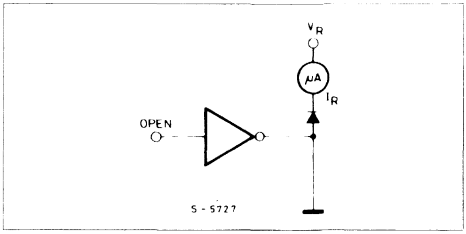


Figure 7.

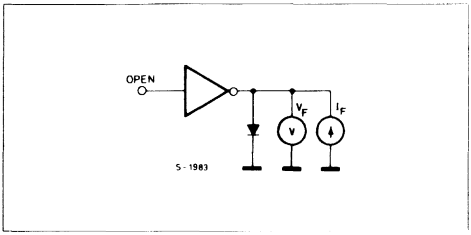


Figure 8.

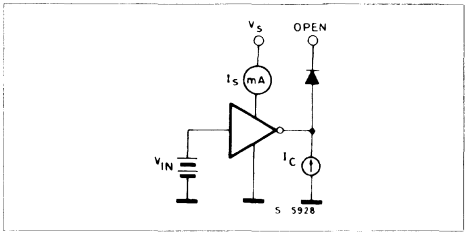


Figure 9 : Input Current as a Function of Input Voltage.

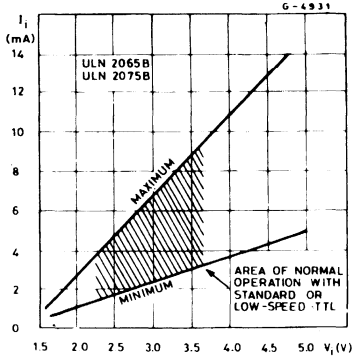


Figure 10 : Input Current as a Function of Input Voltage.

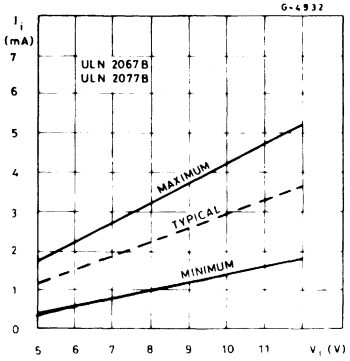
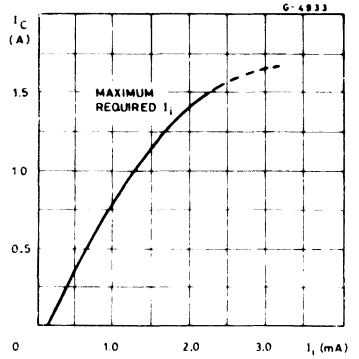


Figure 11 : Collector Current as a Function of Input Current.



MOUNTING INSTRUCTIONS

The $R_{th\ j\text{-}amb}$ can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 12) or to an external heatsink (Fig. 13).

The diagram of figure 14 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side "ℓ" of two equal square copper areas having a thickness of 35 μ (1.4 mils).

During soldering the pins temperature must not exceed 260 °C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 12 : Example of P.C. Board Area which is Used as Heatsink.

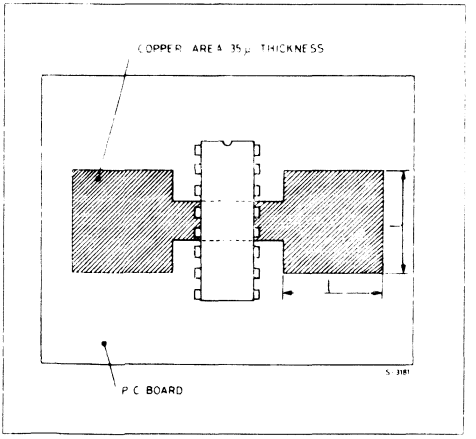


Figure 13 : External Heatsink Mounting Example.

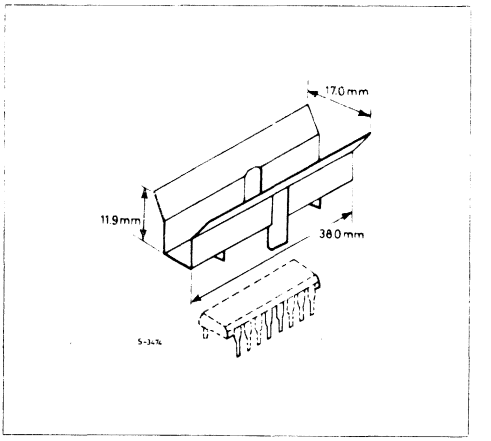


Figure 14 : Maximum Dissipable Power and Junction to Ambient Thermal Resistance vs. Side "l".

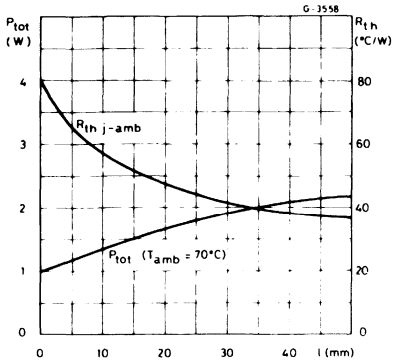
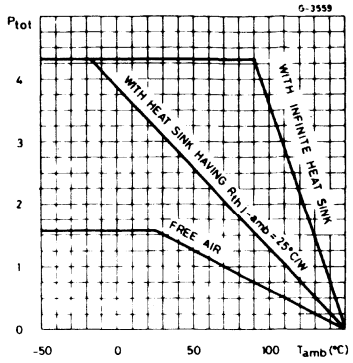


Figure 15 : Maximum Allowable Power Dissipation vs. Ambient Temperature.



SGS-THOMSON
MICROELECTRONICS

ULN2801A ULN2802A ULN2803A ULN2804A ULN2805A

EIGHT DARLINGTON ARRAYS

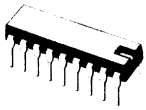
- EIGHT DARLINGTONS WITH COMMON EMITTERS
- OUTPUT CURRENT TO 500 mA
- OUTPUT VOLTAGE TO 50 V
- INTEGRAL SUPPRESSION DIODES
- VERSIONS FOR ALL POPULAR LOGIC FAMILIES
- OUTPUT CAN BE PARALLELED
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY BOARD LAYOUT

DESCRIPTION

The ULN2801A-ULN2805A each contain eight darlington transistors with common emitters and integral suppression diodes for inductive loads. Each darlington features a peak load current rating of 600 mA (500 mA continuous) and can withstand at least 50 V in the off state. Outputs may be paralleled for higher current capability.

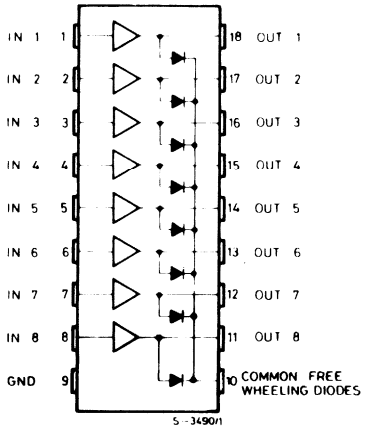
Five versions are available to simplify interfacing to standard logic families : the ULN2801A is designed for general purpose applications with a current limit resistor ; the ULN2802A has a 10.5 KΩ input resistor and zener for 14-25 V PMOS ; the ULN2803A has a 2.7 KΩ input resistor for 5 V TTL and CMOS ; the ULN2804A has a 10.5 KΩ input resistor for 6-15 V CMOS and the ULN2805A is designed to sink a minimum of 350 mA for standard and Schottky TTL where higher output current is required.

All types are supplied in a 18-lead plastic DIP with a copper lead from and feature the convenient input-opposite-output pinout to simplify board layout.



DIP-18
(Plastic)

CONNECTION DIAGRAM (top view)

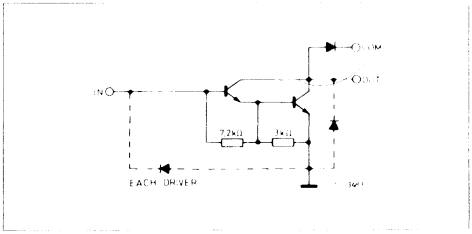


ABSOLUTE MAXIMUM RATINGS

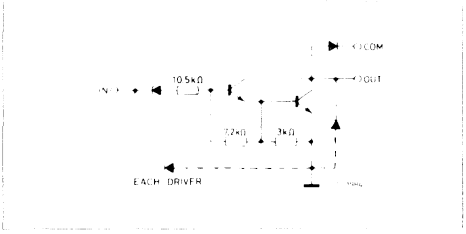
Symbol	Parameter	Value	Unit
V_o	Output Voltage	50	V
V_i	Input Voltage for ULN2802A, 2803A, 2804A for ULN2805A	30 15	V V
I_C	Continuous Collector Current	500	mA
I_B	Continuous Base Current	25	mA
P_{tot}	Power Dissipation (one Darlington pair) (total package)	1.0 2.25	W W
T_{amb}	Operating Ambient Temperature Range	– 20 to 85	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C

SCHEMATIC DIAGRAM AND ORDER CODES

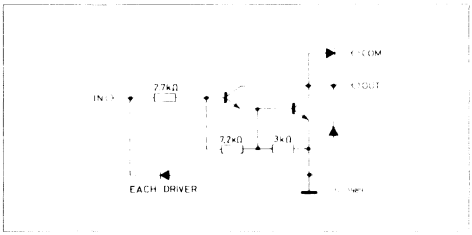
For ULN2801A (each driver for PMOS-CMOS)



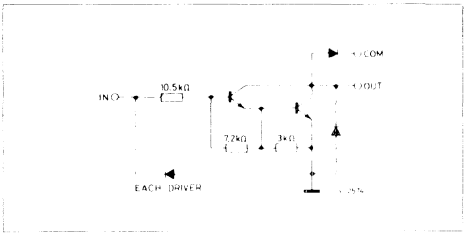
For ULN2802A (each driver for 14-15 V PMOS)



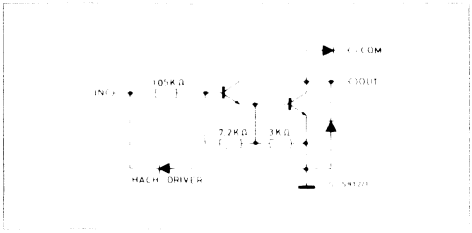
For ULN2803A (each driver for 5 V, TTL/CMOS)



For ULN2804A (each driver for 6-15 V CMOS/PMOS



For ULN2805A (each driver for high out TTL)



THERMAL DATA

$R_{th\ j\ amb}$	Thermal Resistance Junction-ambient	Max.	55	C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 C unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	V_{CE} = 50 V				50	µA	1a
		T_{amb} = 70 C	V_{CE} = 50 V			100	µA	1a
		T_{amb} = 70 C for **ULN2802A**						
		V_{CE} = 50 V	V_i = 6 V			500	µA	1b
		for **ULN2804A**						
		V_{CE} = 50 V	V_i = 1 V			500	µA	1b
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 100 mA	I_B = 250 µA		0.9	1.1	V	
		I_C = 200 mA	I_B = 350 µA		1.1	1.3	V	2
		I_C = 350 mA	I_B = 500 µA		1.3	1.6	V	
$I_{i(on)}$	Input Current	for **ULN2802A**	V_i = 17 V		0.82	1.25	mA	
		for **ULN2803A**	V_i = 3.85 V		0.93	1.35	mA	
		for **ULN2804A**	V_i = 5 V		0.35	0.5	mA	3
			V_i = 12 V		1	1.45	mA	
		for **ULN2805A**	V_i = 3 V		1.5	2.4	mA	
$I_{i(off)}$	Input Current	T_{amb} = 70 C	I_C = 500 µA	50	65		µA	4
$V_{i(on)}$	Input Voltage	for **ULN2802A**						
		V_{CE} = 2 V	I_C = 300 mA			13	V	
		for **ULN2803A**						
		V_{CE} = 2 V	I_C = 200 mA			2.4	V	
		V_{CE} = 2 V	I_C = 250 mA			2.7	V	
		V_{CE} = 2 V	I_C = 300 mA			3	V	
		for **ULN2804A**						5
		V_{CE} = 2 V	I_C = 125 mA			5	V	
		V_{CE} = 2 V	I_C = 200 mA			6	V	
		V_{CE} = 2 V	I_C = 275 mA			7	V	
		V_{CE} = 2 V	I_C = 350 mA			8	V	
		for **ULN2805A**						
		V_{CE} = 2 V	I_C = 350 mA			2.4	V	
h_{FE}	DC Forward Current Gain	for **ULN2801A**						
		V_{CE} = 2 V	I_C = 350 mA	1000			–	2
C_i	Input Capacitance				15	25	pF	–
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o			0.25	1	µs	–
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o			0.25	1	µs	–
I_R	Clamp Diode Leakage Current	V_R = 50 V				50	µA	6
		T_{amb} = 70 C	V_R = 50 V			100	µA	
V_F	Clamp Diode Forward Voltage	I_F = 350 mA			1.7	2	V	7

TEST CIRCUITS

Figure 1a.

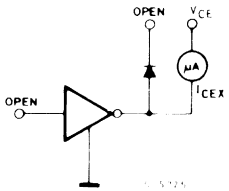


Figure 1b.

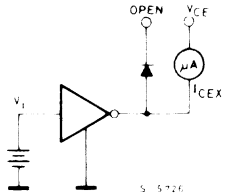


Figure 2.

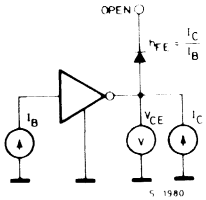


Figure 3.

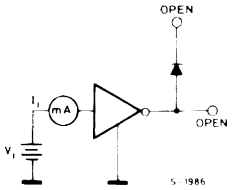


Figure 4.

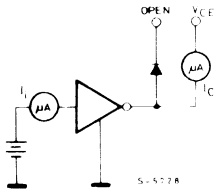


Figure 5.

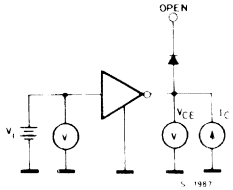


Figure 6.

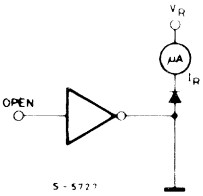


Figure 7.

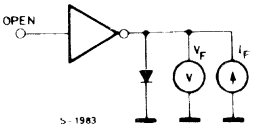


Figure 8 : Collector Current as a Function of Saturation Voltage.

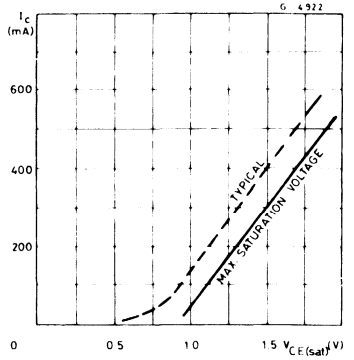


Figure 9 : Collector Current as a Function of Input Current.

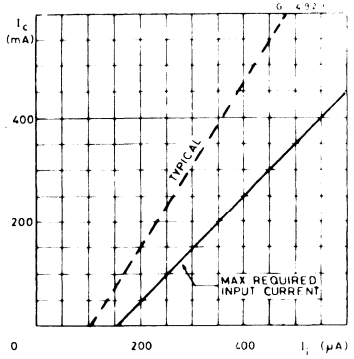


Figure 10 : Allowable Average Power Dissipation as a Function of Ambient Temperature.

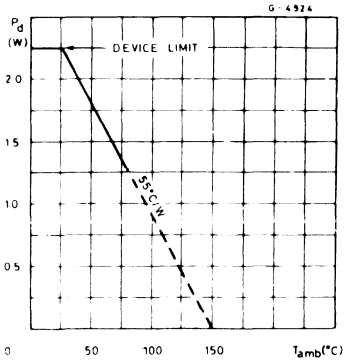


Figure 11 : Peak Collector Current as a Function of Duty Cycle.

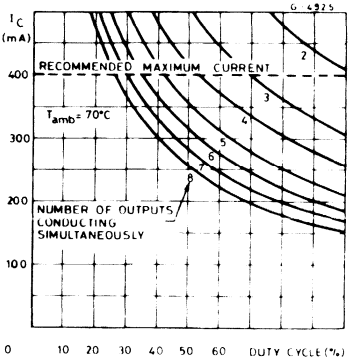


Figure 12 : Peak Collector Current as a Function of Duty.

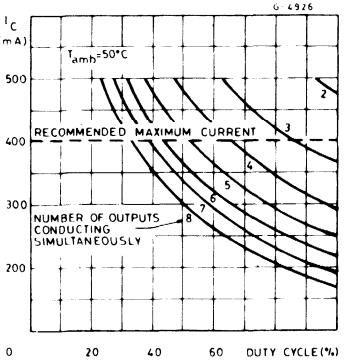


Figure 13 : Input Current as a Function of Input Voltage (for ULN2802A).

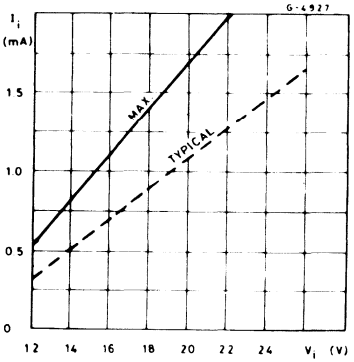


Figure 14 : Input Current as a Function of Input Voltage (for ULN2804A)

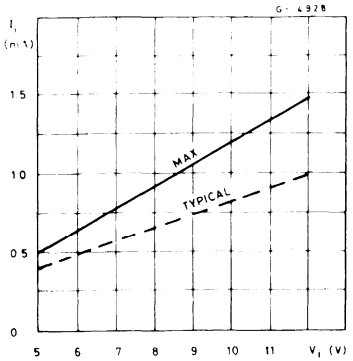


Figure 15 : Input Current as a Function of Input Voltage (for ULN2803A)

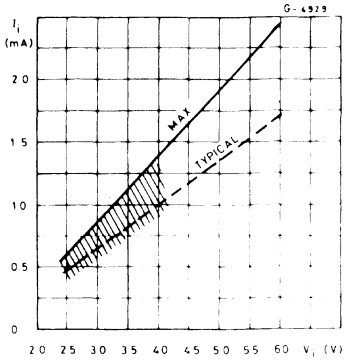
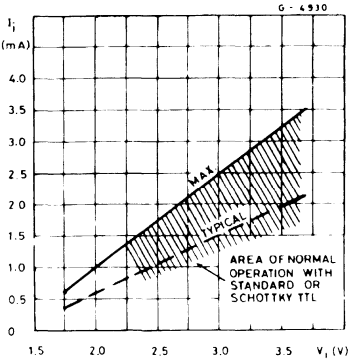


Figure 16 : Input Current as a Function of Input Voltage (for ULN2805A)



SGS-THOMSON MICROELECTRONICS

ULQ2001A-ULQ2003A
ULQ2002A-ULQ2004A

SEVEN DARLINGTON ARRAYS

- SEVEN DARLINGTONS PER PACKAGE
- **EXTENDED TEMPERATURE RANGE (–40 to 105°C)**
- OUTPUT CURRENT 500 mA PER DRIVER (600 mA PEAK)
- OUTPUT VOLTAGE 50 V
- INTEGRAL SUPPRESSION DIODES FOR INDUCTIVE LOADS
- OUTPUTS CAN BE PARALLELED FOR HIGHER CURRENT
- TTL/CMOS/PMOS/DTL COMPATIBLE INPUTS
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY LAYOUT

DESCRIPTION

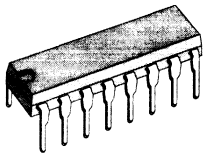
The ULQ2001A, ULQ2002A, ULQ2003 and ULQ2004A are high voltage, high current darlington arrays each containing seven open collector darlington pairs with common emitters. Each channel is rated at 500 mA and can withstand peak currents of 600 mA. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout.

The four versions interface to all common logic families :

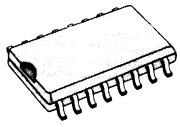
ULQ2001A	General Purpose, DTL, TTL, PMOS, CMOS
ULQ2002A	14-25 V PMOS
ULQ2003A	5 V TTL, CMOS
ULQ2004A	6–15 V CMOS, PMOS

These versatile devices are useful for driving a wide range of loads including solenoids, relays DC mo-tors, LED displays filament lamps, thermal printheads and high power buffers.

The ULQ2001A/2002A/2003A and 2004A are supplied in 16 pin plastic DIP packages with a copper leadframe to reduce thermal resistance. They are available also in small outline package (SO-16) as ULQ2001D1/2002D1/2003D1/2004D1.



DIP16



SO16

ORDERING NUMBERS:

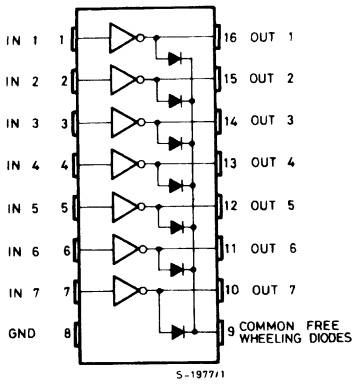
ULQ2001A/2A/3A/4A (DIP-16)

ULQ2001D1/2D1/3D1/4D1 (SO-16)

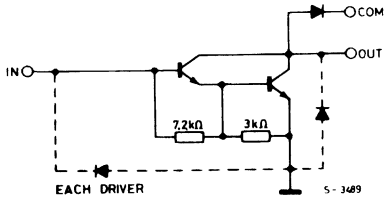
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_o	Output Voltage	50	V
V_{in}	Input Voltage (for ULQ2002A/D1 - 2003A/D1 - 2004A/D1)	30	V
I_c	Continuous Colletor Current	500	mA
I_b	Continuous Base Current	25	mA
T_{amb}	Operating Ambient Temperature Range	–40 to 105	°C
T_{stg}	Storage Temperature Range	–55 to 150	°C
T_j	Junction Temperature	150	°C

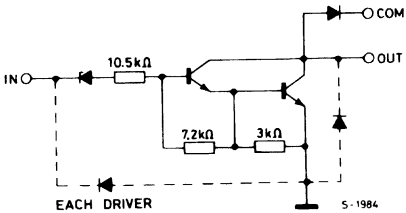
PIN CONNECTION



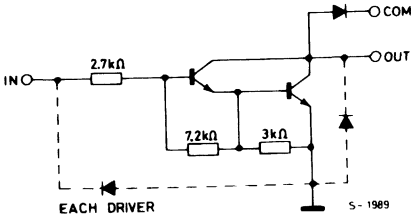
SCHEMATIC DIAGRAM



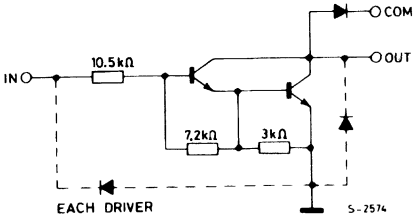
Series ULQ-2001A
(each driver)



Series ULQ-2002A
(each driver)



Series ULQ-2003A
(each driver)



Series ULQ-2004A
(each driver)

THERMAL DATA

			DIP–16	SO–16
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	70 °C/W	165 °C/W

ELECTRICAL CHARACTERISTICS (T_J = –40 to 105 °C for DIP16 unless otherwise specified)
(T_J = 25 to 105 °C for SO16 unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	V_{CE} = 50 V				50	µA	1a
		T_J = 105 °C	V_{CE} = 50 V			100	µA	1a
		T_J = 105 °C for **ULQ2002A**						
		V_{CE} = 50 V	V_i = 6 V			500	µA	1b
		for **ULQ2004A**						
		V_{CE} = 50 V	V_i = 1 V			500	µA	1b
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 100 mA	I_B = 250 µA		0.9	1.1	V	2
		I_C = 200 mA	I_B = 350 µA		1.1	1.3	V	2
		I_C = 350 mA	I_B = 500 µA		1.3	1.6	V	2
$I_{i(on)}$	Input Current	for **ULQ2002A**	V_i = 17 V		0.82	1.25	mA	3
		for **ULQ2003A**	V_i = 3.85 V		0.93	1.35	mA	3
		for **ULQ2004A**	V_i = 5 V		0.35	0.5	mA	3
		V_i = 12 V			1	1.45	mA	3
$I_{i(off)}$	Input Current	T_J = 105 °C	I_C = 500 µA	50	65		µA	4
$V_{i(on)}$	Input Voltage	for **ULQ2002A**						
		V_{CE} = 2 V	I_C = 300 mA			13	V	5
		for **ULQ2003A**						
		V_{CE} = 2 V	I_C = 200 mA			2.4	V	5
		V_{CE} = 2 V	I_C = 250 mA			2.7	V	5
		V_{CE} = 2 V	I_C = 300 mA			3	V	5
		for **ULQ2004A**						
		V_{CE} = 2 V	I_C = 125 mA			5	V	5
		V_{CE} = 2 V	I_C = 200 mA			6	V	5
		V_{CE} = 2 V	I_C = 275 mA			7	V	5
		V_{CE} = 2 V	I_C = 350 mA			8	V	5
h_{FE}	DC Forward Current Gain	for **ULQ2001A**						
		V_{CE} = 2 V	I_C = 350 mA	1000			–	2
C_i	Input Capacitance				15	25 (*)	pF	–
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o			0.25	1 (*)	µs	–
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o			0.25	1 (*)	µs	–
I_R	Clamp Diode Leakage Current	V_R = 50 V				50	µA	6
		T_J = 105 °C	V_R = 50 V			100	µA	6
V_F	Clamp Diode Forward Voltage	I_F = 350 mA			1.7	2	V	7

(*) GUARANTEED BY DESIGN.

TEST CIRCUITS

Figure 1a.

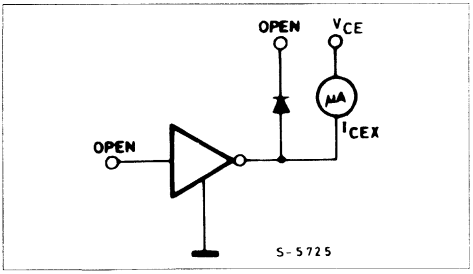


Figure 1b.

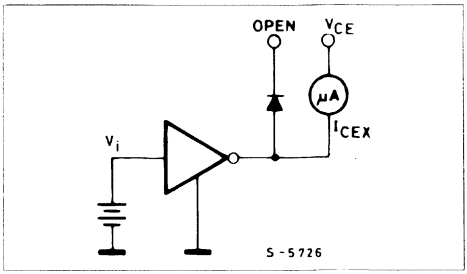


Figure 2.

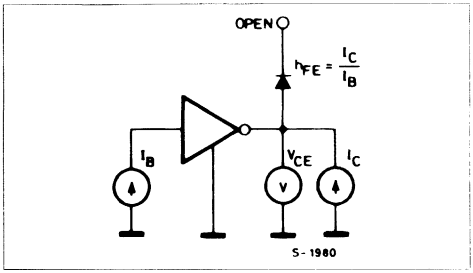


Figure 3.

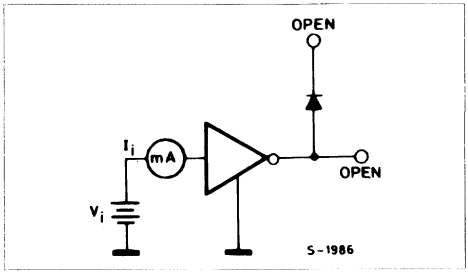


Figure 4.

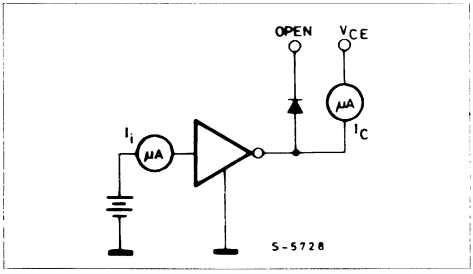


Figure 5.

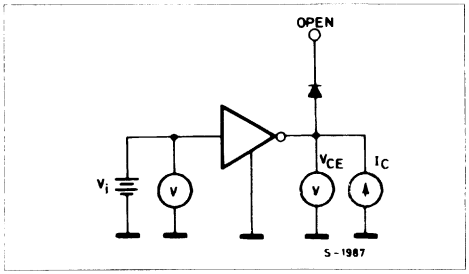


Figure 6.

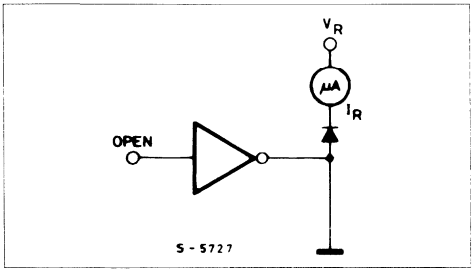
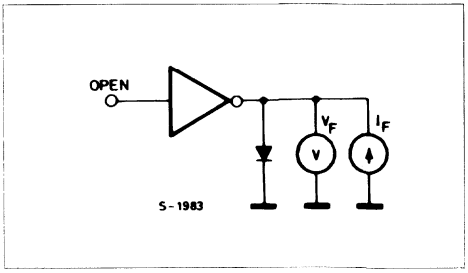
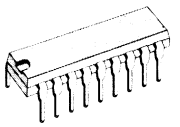


Figure 7.



EIGHT DARLINGTON ARRAYS

- EIGHT DARLINGTONS PER PACKAGE
- **EXTENDED TEMPERATURE RANGE (– 40 to 105°C)**
- OUTPUT CURRENT TO 500 mA
- OUTPUT VOLTAGE TO 50 V
- INTEGRAL SUPPRESSION DIODES
- VERSIONS FOR ALL POPULAR LOGIC FAMILIES
- OUTPUT CAN BE PARALLELED
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY BOARD LAYOUT



DIP-18

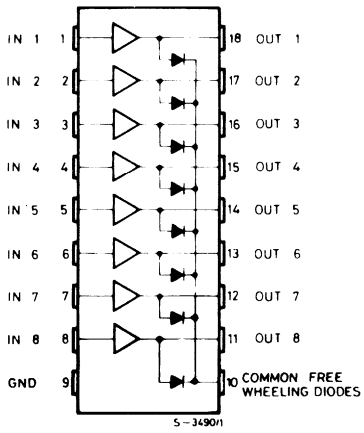
DESCRIPTION

The ULQ2801A-ULQ2805A each contain eight darlington transistors with common emitters and integral suppression diodes for inductive loads. Each darlington features a peak load current rating of 600 mA (500 mA continuous) and can withstand at least 50 V in the off state. Outputs may be paralleled for higher current capability.

Five versions are available to simplify interfacing to standard logic families : the ULQ2801A is designed for general purpose applications with a current limit resistor ; the ULQ2802A has a 10.5 KΩ input resistor and zener for 14-25 V PMOS ; the ULQ2803A has a 2.7 KΩ input resistor for 5 V TTL and CMOS ; the ULQ2804A has a 10.5 KΩ input resistor for 6-15 V CMOS and the ULQ2805A is designed to sink a minimum of 350 mA for standard and Schottky TTL where higher output current is required.

All types are supplied in a 18-lead plastic DIP with a copper lead frame and feature the convenient input-opposite-output pinout to simplify board layout.

PIN CONNECTION (top view)

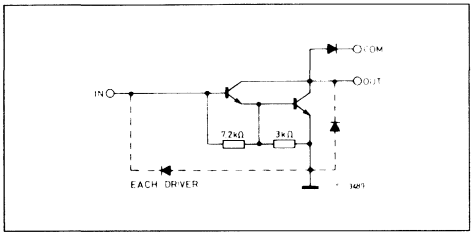


ABSOLUTE MAXIMUM RATINGS

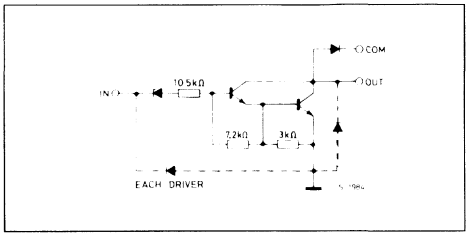
Symbol	Parameter	Value	Unit
V_o	Output Voltage	50	V
V_i	Input Voltage for ULQ2802A, 2803A, 2804A for ULQ2805A	30 15	V V
I_C	Continuous Collector Current	500	mA
I_B	Continuous Base Current	25	mA
P_{tot}	Power Dissipation (one Darlington pair) (total package)	1.0 2.25	W W
T_{amb}	Operating Ambient Temperature Range	– 40 to 105	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C

SCHEMATIC DIAGRAM AND ORDER CODES

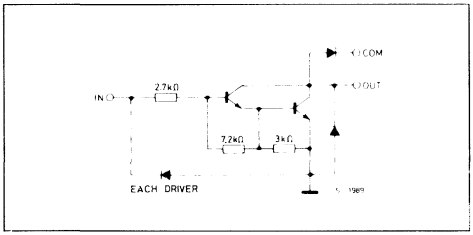
For ULQ2801A (each driver for PMOS-CMOS)



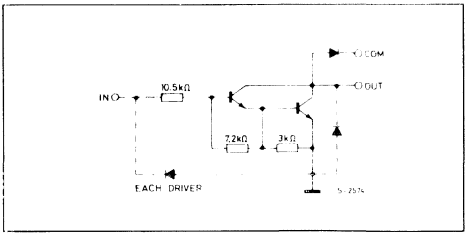
For ULQ2802A (each driver for 14-15 V PMOS)



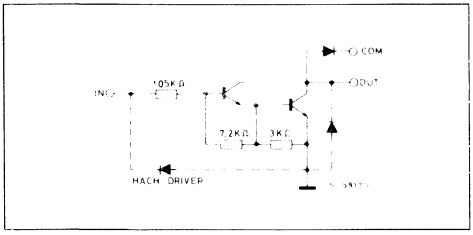
For ULQ2803A (each driver for 5 V, TTL/CMOS)



For ULQ2804A (each driver for 6-15 V CMOS/PMOS



For ULQ2805A (each driver for high out TTL)



THERMAL DATA

$R_{th\ j-amb}$	Thermal Resistance Junction-ambient	Max.	55	°C/W

ELECTRICAL CHARACTERISTICS (Tj = –40 to 105°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	V_{CE} = 50V			50	µA	1a
		T_J = 105°C V_{CE} = 50V			100	µA	1a
		T_J = 105°C for **ULQ2802A** V_{CE} = 50V V_i = 6V			500	µA	1b
		for **ULQ2804A** V_{CE} = 50V V_i = 1V			500	µA	1b
$V_{CE\ (sat)}$	Collector-emitter Saturation Voltage	I_C = 100mA I_B = 250µA		0.9	1.1	V	
		I_C = 200mA I_B = 350µA		1.1	1.3	V	2
		I_C = 350mA I_B = 500µA		1.3	1.6	V	
$I_{i(on)}$	Input Current	for **ULQ2802A** V_i = 17V		0.82	1.25	mA	
		for **ULQ2803A** V_i = 3.85V		0.93	1.35	mA	
		for **ULQ2804A** V_i = 5V		0.35	0.5	mA	3
		V_i = 12V		1	1.45	mA	
		for **ULQ2805A** V_i = 3V		1.5	2.4	mA	
$I_{i(off)}$	Input Current	T_J = 105°C I_C = 500µA	50	65		µA	4
$V_{i(on)}$	Input Voltage	for **ULQ2802A**					
		V_{CE} = 2V I_c = 300mA			13	V	
		for **ULQ2803A**					
		V_{CE} = 2V I_c = 200mA			2.4	V	
		V_{CE} = 2V I_c = 250mA			2.7	V	
		V_{CE} = 2V I_c = 300mA			3	V	
		for **ULQ2804A**					5
		V_{CE} = 2V I_c = 125mA			5	V	
		V_{CE} = 2V I_c = 200mA			6	V	
		V_{CE} = 2V I_c = 275mA			7	V	
		V_{CE} = 2V I_c = 350mA			8	V	
		for **ULQ2805A**					
		V_{CE} = 2V I_c = 350mA			2.4	V	
h_{FE}	DC Forward Current Gain	for **ULQ2802A** V_{CE} = 2V I_c = 350mA	1000			–	2
C_i	Input Capacitance			15	25 (*)	pF	–
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o		0.25	1 (*)	µs	–
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o		0.25	1 (*)	µs	–
I_R	Clamp Diode Leakage Current	V_R = 50V			50	µA	6
		T_J = 105°C V_R = 50V			100	µA	
V_F	Clamp Diode Forward Voltage	I_F = 350mA		1.7	2	V	7

(*) GUARANTEED BY DESIGN.

TEST CIRCUITS

Figure 1a.

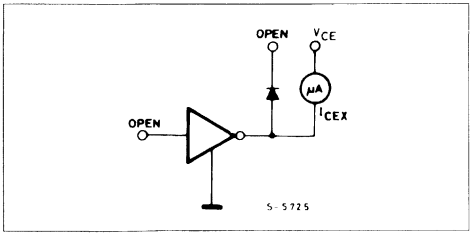


Figure 1b.

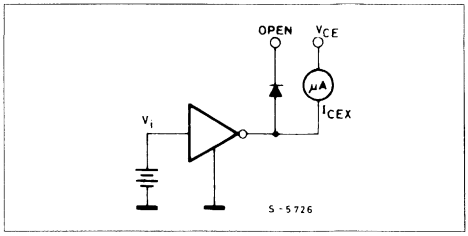


Figure 2.

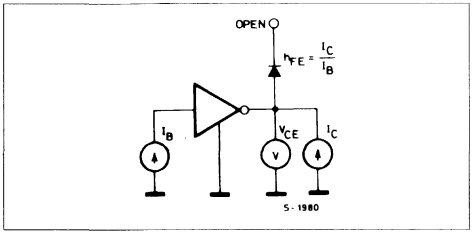


Figure 3.

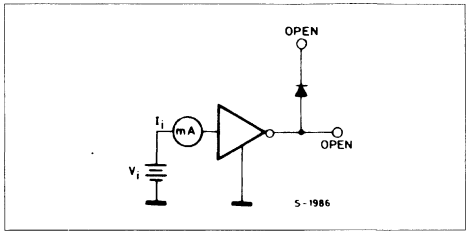


Figure 4.

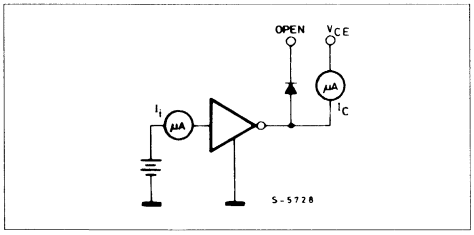


Figure 5.

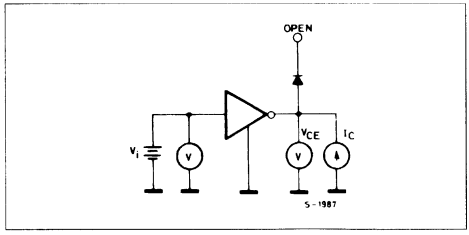


Figure 6.

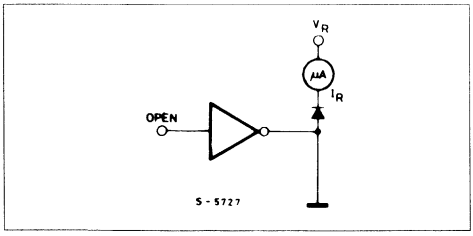


Figure 7.

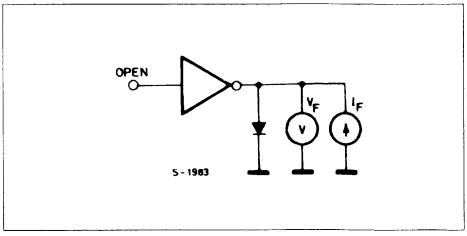


Figure 8 : Collector Current as a Function of Saturation Voltage.

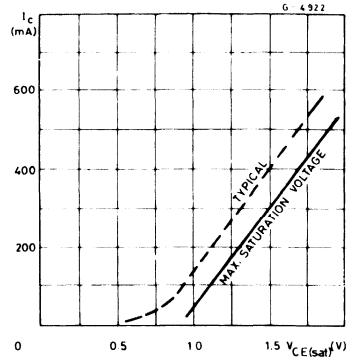


Figure 9 : Collector Current as a Function of Input Current.

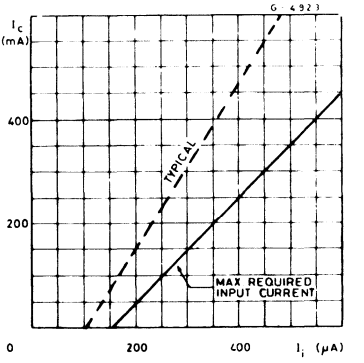


Figure 10 : Allowable Average Power Dissipation as a Function of Ambient Temperature.

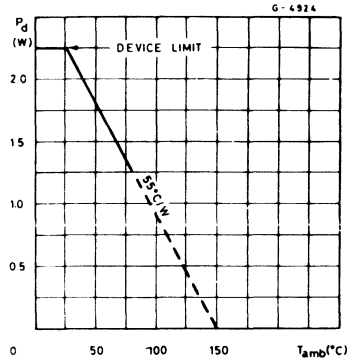


Figure 11 : Peak Collector Current as a Function of Duty Cycle.

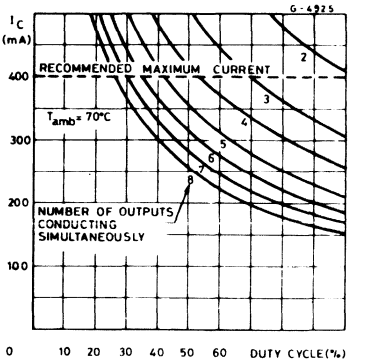


Figure 12 : Peak Collector Current as a Function of Duty.

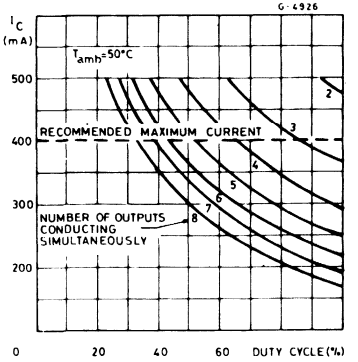


Figure 13 : Input Current as a Function of Input Voltage (for ULQ2802A).

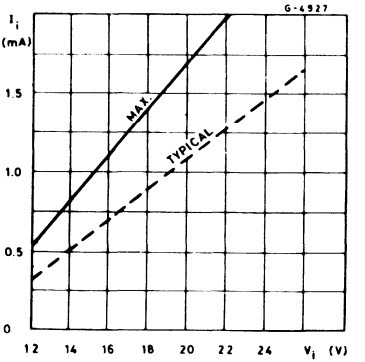


Figure 14 : Input Current as a Function of Input Voltage (for ULQ2804A)

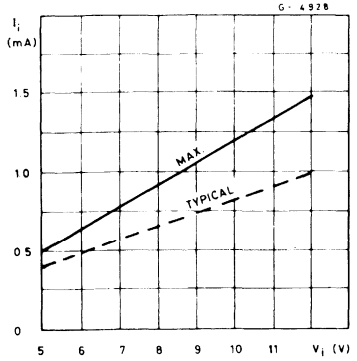


Figure 15 : Input Current as a Function of Input Voltage (for ULQ2803A)

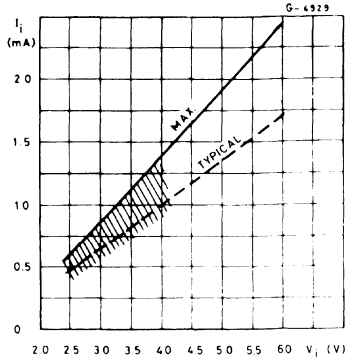
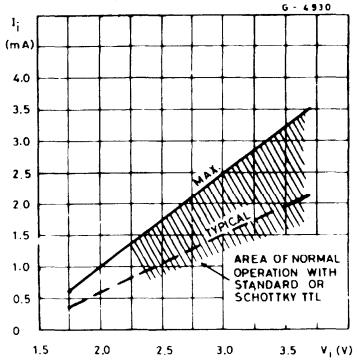


Figure 16 : Input Current as a Function of Input Voltage (for ULQ2805A)

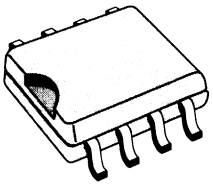


PACKAGES

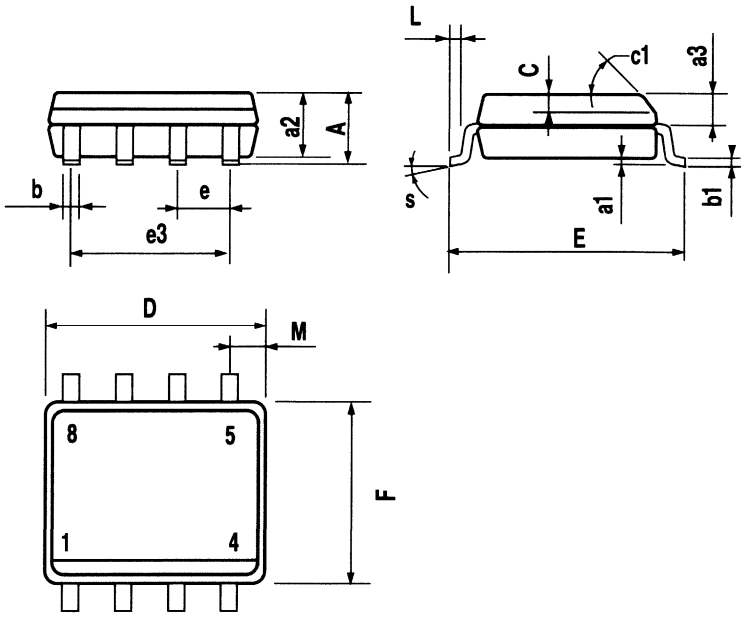
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.15		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO8

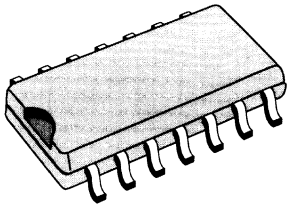


P013M

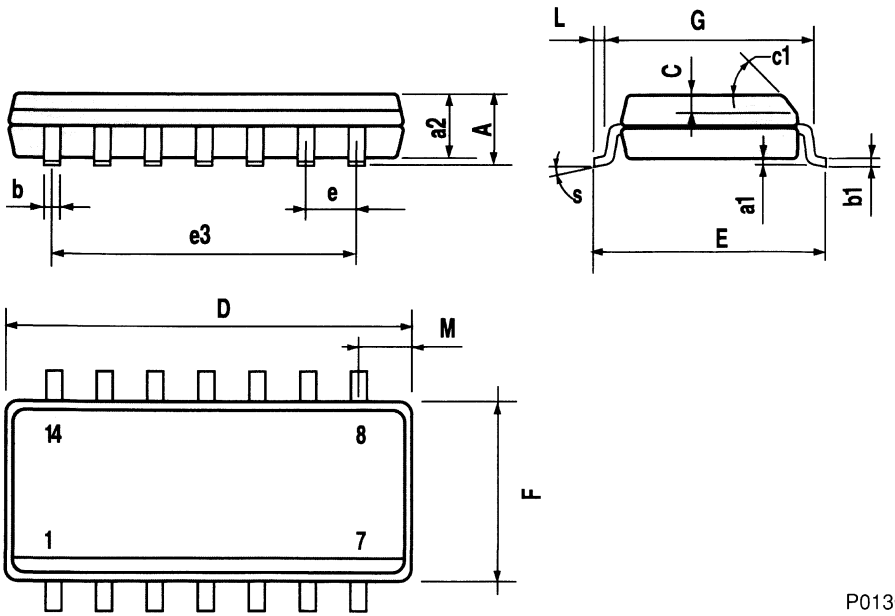
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.2	0.004		0.008
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.15		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.020		0.050
M			0.68			0.027
S	8° (max.)					

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO14

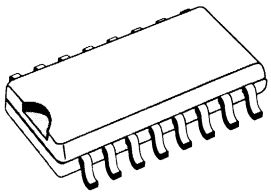


P013G

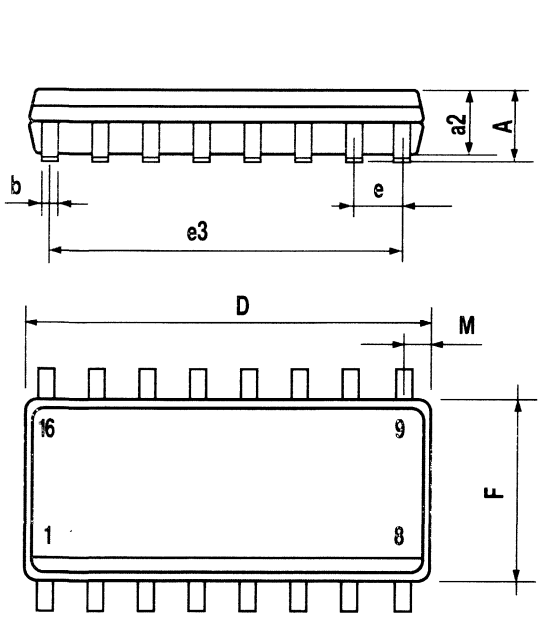
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.2	0.004		0.008
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45° (typ.)					
D	9.8		10	0.386		0.394
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.150		0.157
G	4.6		5.3	0.181		0.209
L	0.5		1.27	0.020		0.050
M			0.62			0.024
S	8° (max.)					

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO16

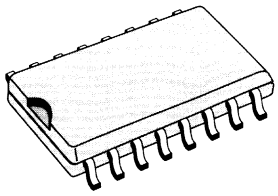


P013H

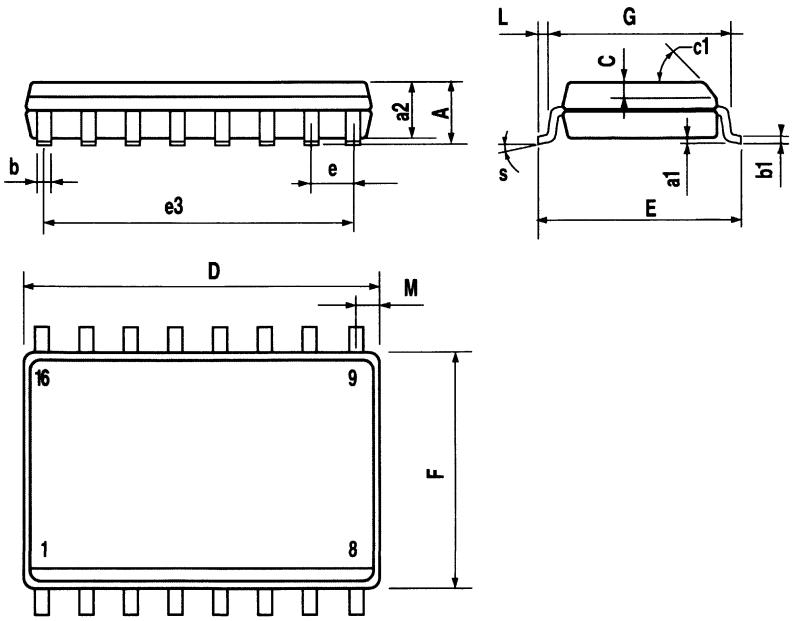
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.057
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45° (typ.)					
D	10.1		10.5	0.397		0.413
E	10.0		10.65	0.393		0.419
e		1.27			0.050	
e3		8.89			0.350	
F	7.4		7.6	0.291		0.300
G	8.8		9.15	0.346		0.360
L	0.5		1.27	0.020		0.050
M			0.75			0.029
S	8° (max.)					

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO16L

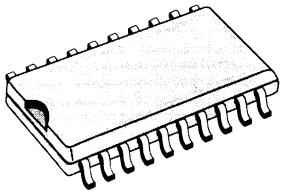


P013I

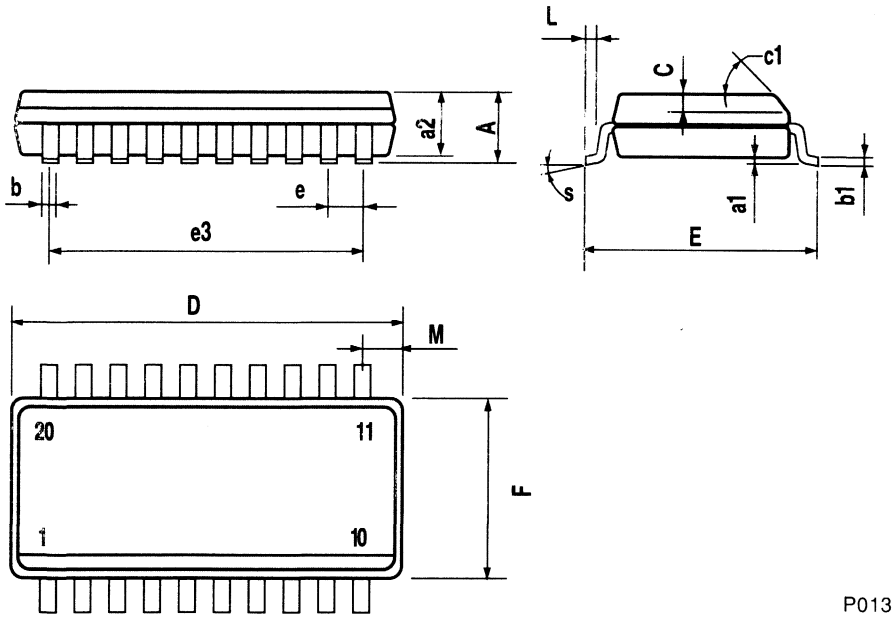
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	12.6		13.0	0.496		0.510
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.4		7.6	0.291		0.300
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8° (max.)					

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO20

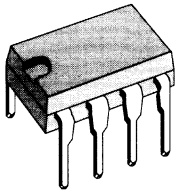


P013L

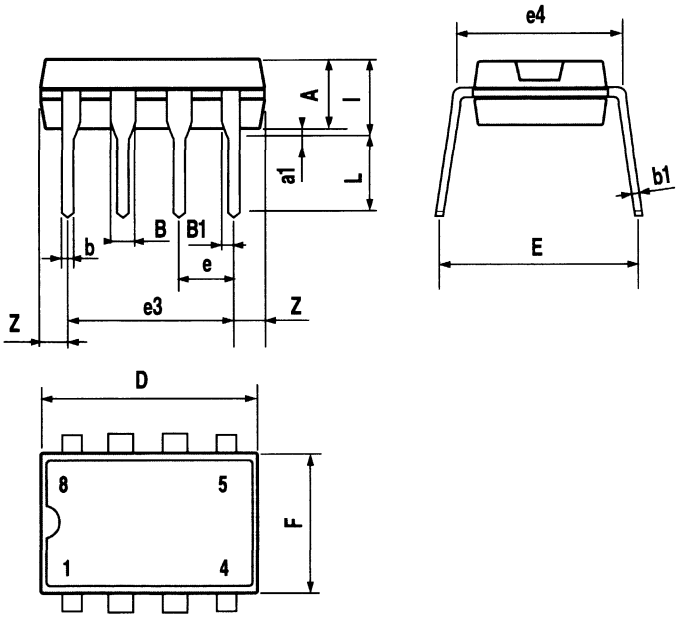
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Minidip (0.25)

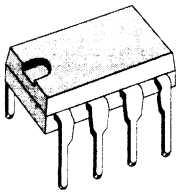


P001W

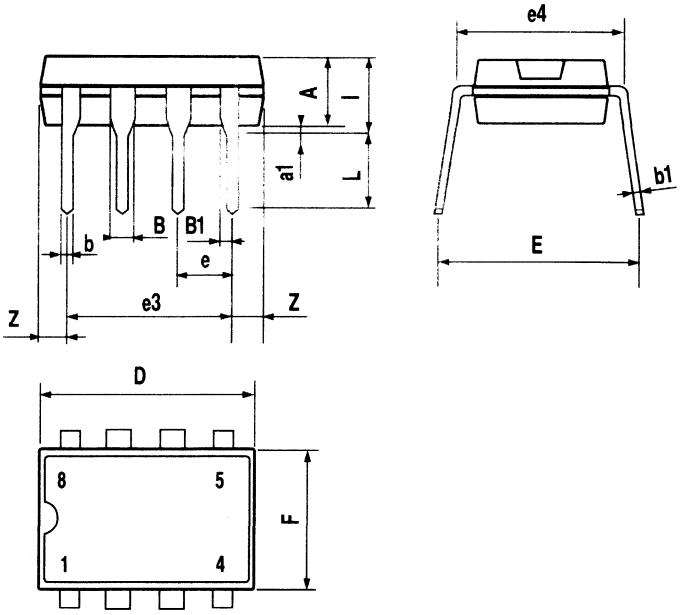
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.3			0.130	
a1	0.7			0.028		
B	1.39		1.65	0.055		0.065
B1	0.91		1.04	0.036		0.041
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			9.8			0.386
E		8.8			0.346	
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			7.1			0.280
I			4.8			0.189
L		3.3			0.130	
Z	0.44		1.6	0.017		0.063

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Minidip (0.4)

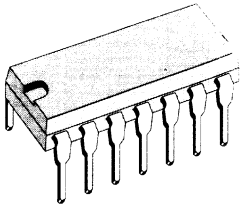


P001F

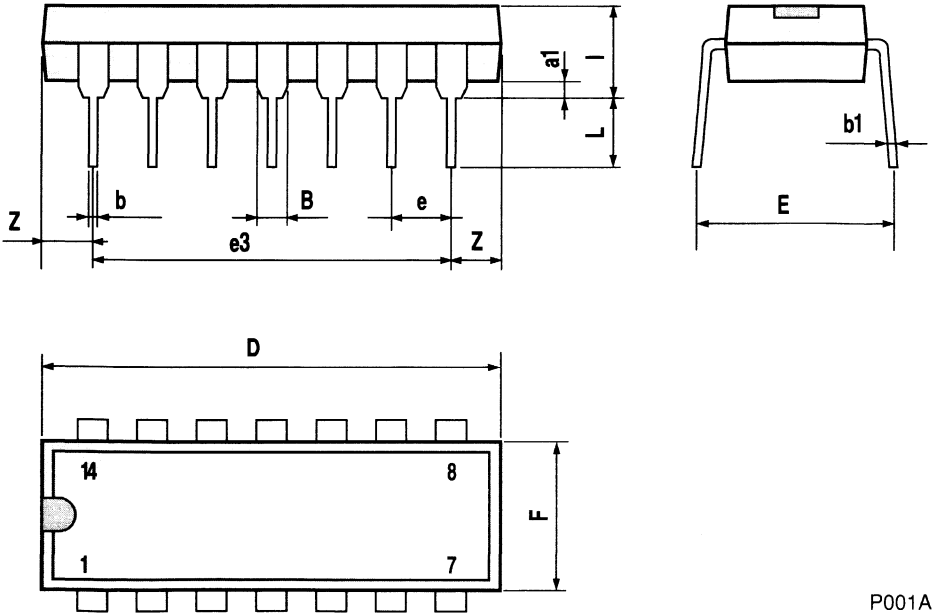
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Plastic DIP14

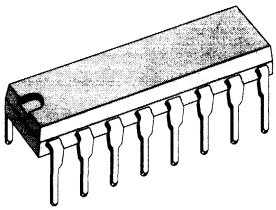


P001A

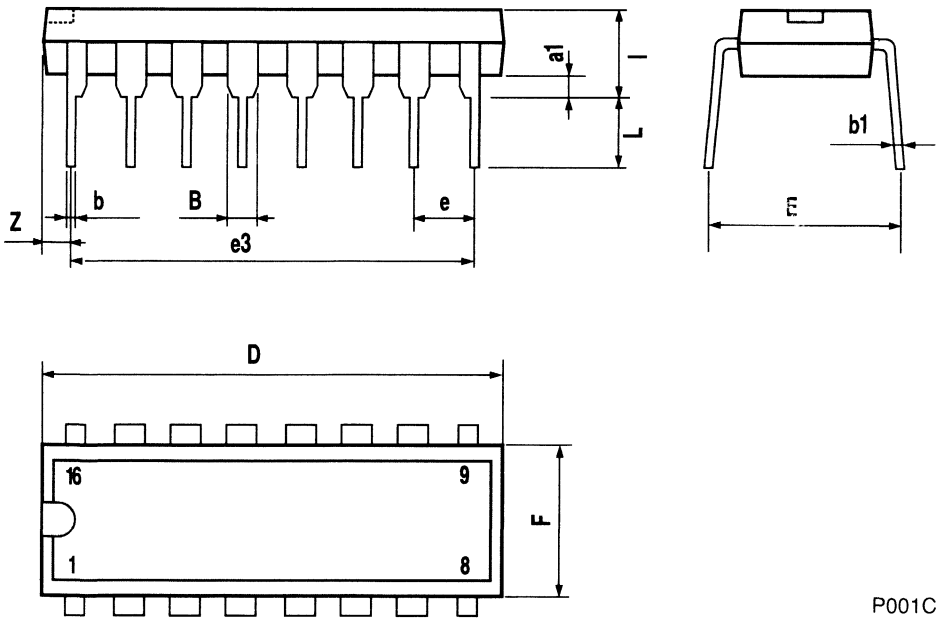
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Plastic DIP16 (0.25)

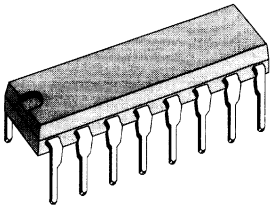


P001C

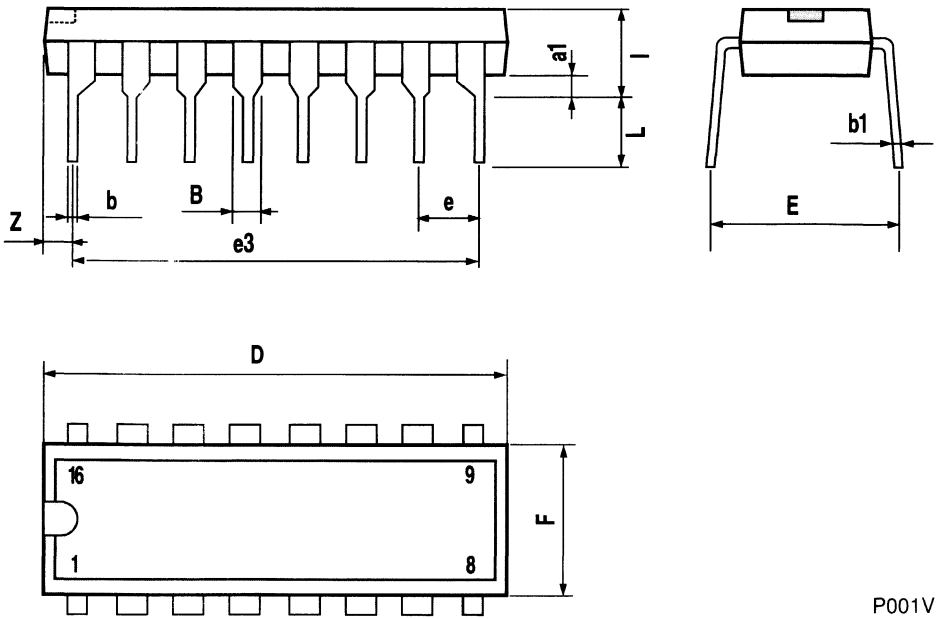
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.4	0.033		0.055
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			20			0.787
E		8.8			0.346	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



POWERDIP: (8+8), (12+2+2)

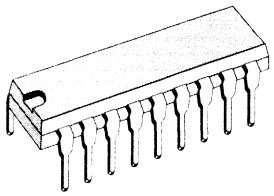


P001V

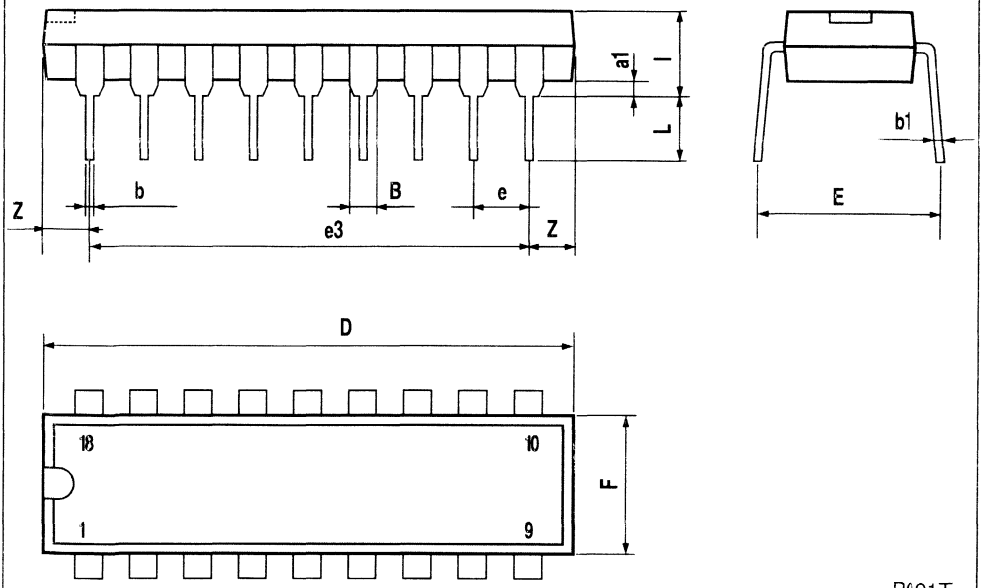
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.064
b		0.46			0.018	
b1		0.25			0.010	
D			23.24			0.914
E		8.5			0.335	
e		2.54			0.100	
e3		20.32			0.800	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z		1.27	1.59		0.050	0.062

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



DIP18 (0.25)

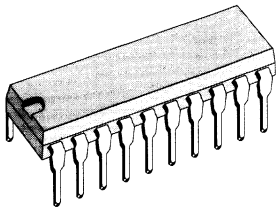


P001T

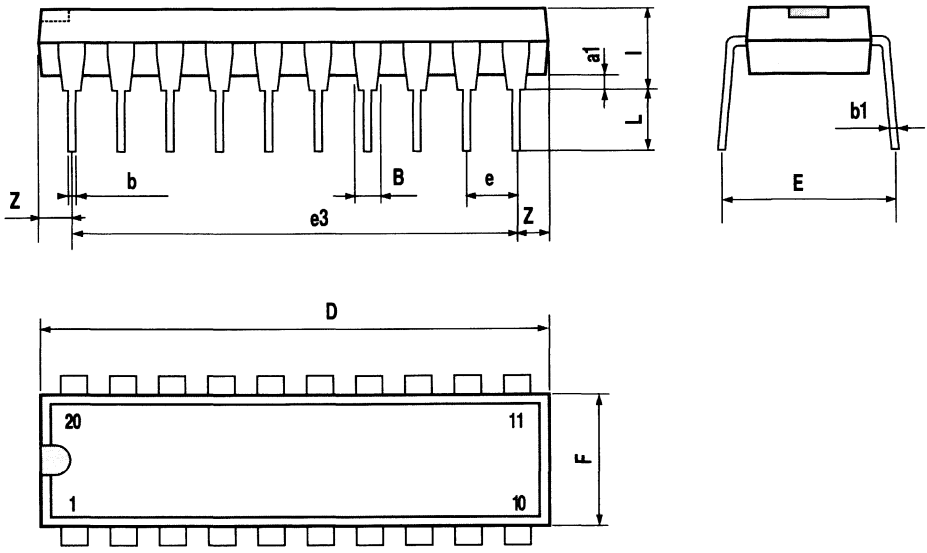
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Plastic DIP20 (0.25)

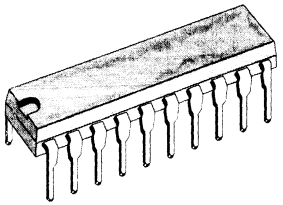


P001J

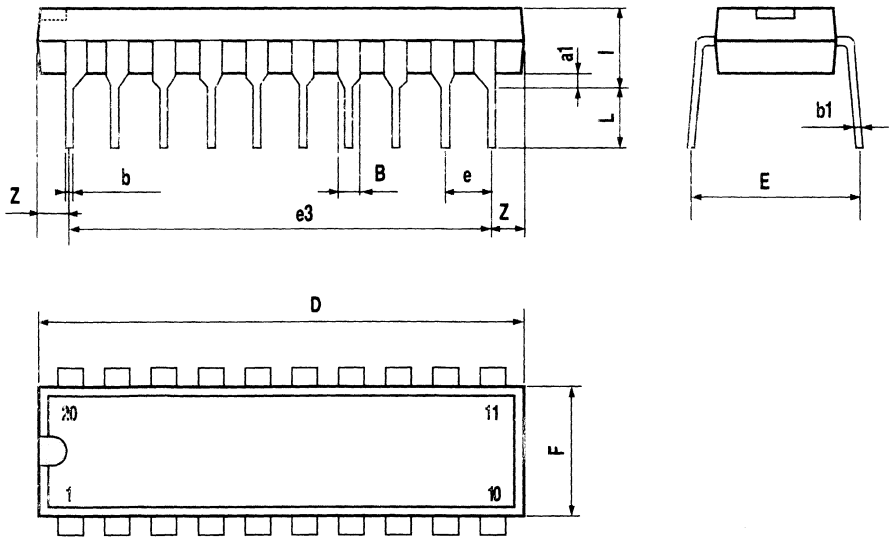
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.4	0.033		0.055
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			24.8			0.976
E		8.8			0.346	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



POWERDIP (16+2+2)

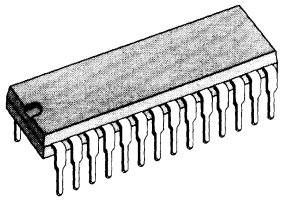


P001X

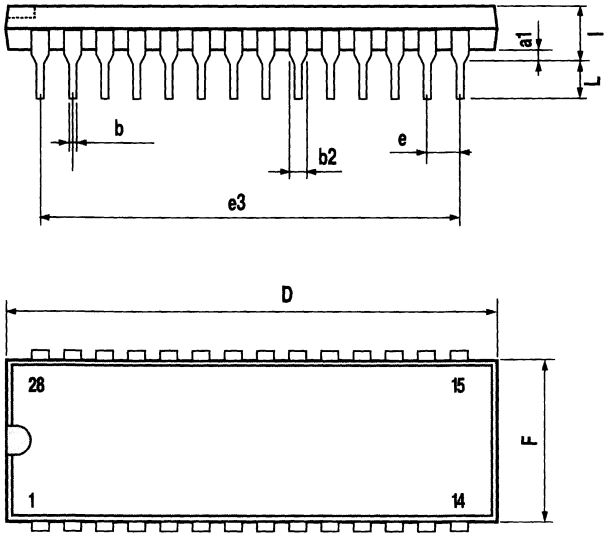
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			37.34			1.470
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		33.02			1.300	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



DIP28

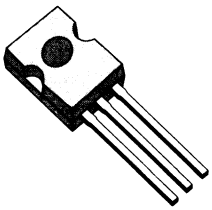


P043D

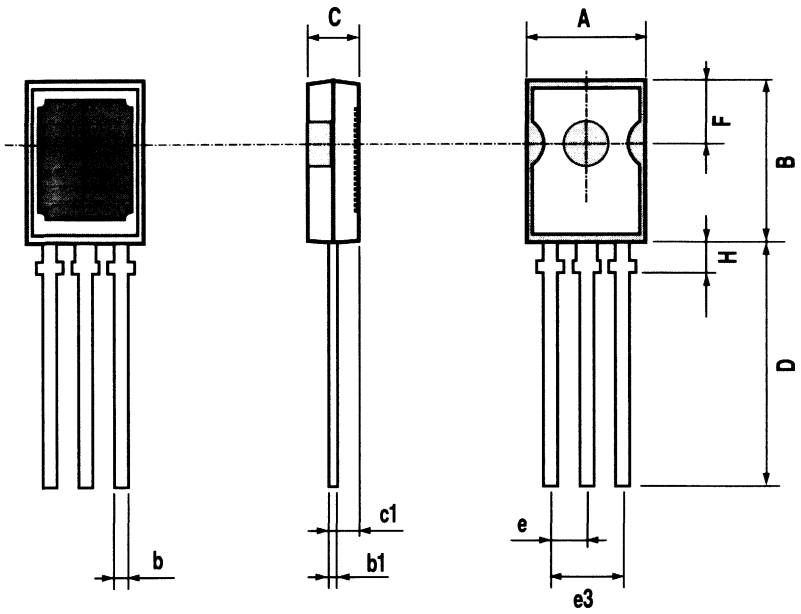
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	7.4		7.8	0.291		0.307
B	10.5		10.8	0.413		0.425
b	0.7		0.9	0.028		0.035
b1	0.49		0.75	0.019		0.030
C	2.4		2.7	0.094		0.106
c1		1.2			0.047	
D		15.7			0.618	
e		2.2			0.087	
e3		4.4			0.173	
F		3.8			0.150	
H			2.54		0.100	

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SOT82

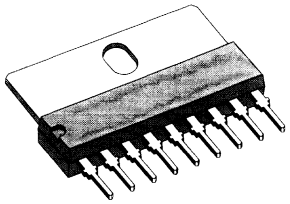


P032A

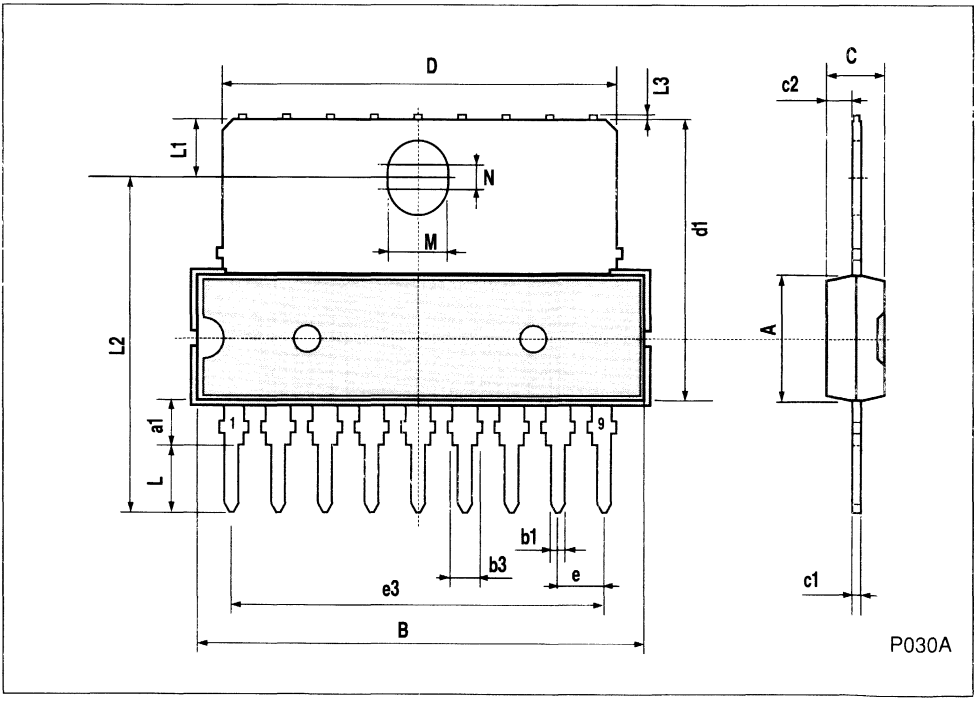
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			7.1			0.280
a1	2.7		3	0.106		0.118
B			24.8			0.976
b1		0.5			0.020	
b3	0.85		1.6	0.033		0.063
C		3.3			0.130	
c1		0.43			0.017	
c2		1.32			0.052	
D			21.2			0.835
d1		14.5			0.571	
e		2.54			0.100	
e3		20.32			0.800	
L	3.1			0.122		
L1		3			0.118	
L2		17.6			0.693	
L3			0.25			0.010
M		3.2			0.126	
N		1			0.039	

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



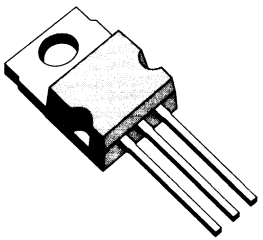
SIP9



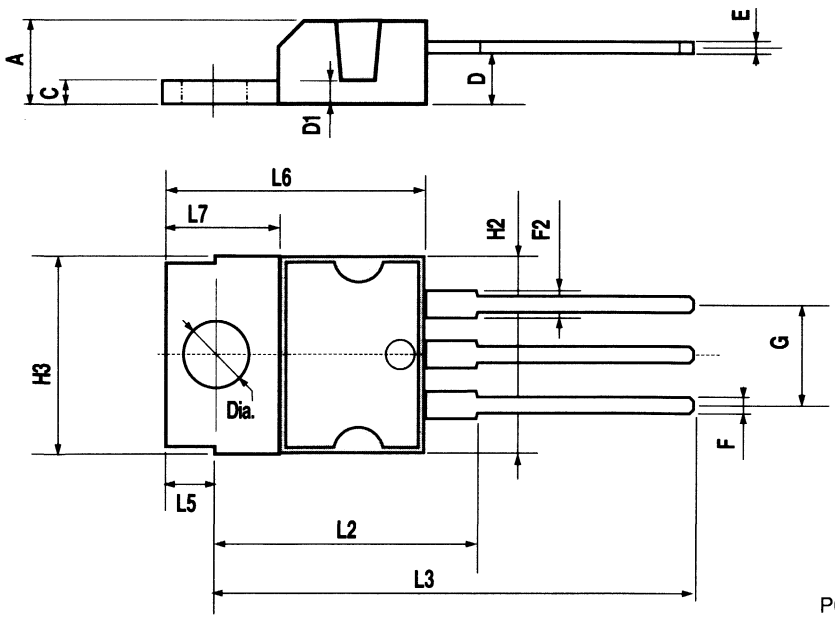
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.8		1.05	0.031		0.041
F2	1.15		1.4	0.045		0.055
G	4.95	5.08	5.21	0.195	0.200	0.205
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L2		16.2			0.638	
L3	26.3	26.7	27.1	1.035	1.051	1.067
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
Dia	3.65		3.85	0.144		0.152

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



TO220

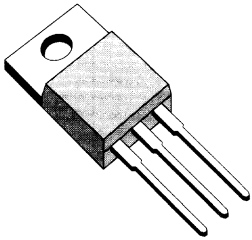


P011D

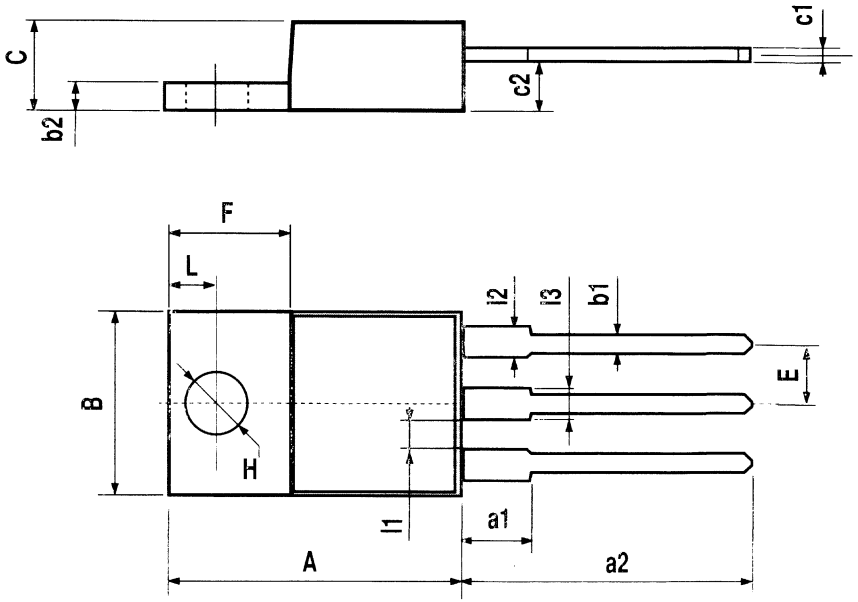
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		15.2			0.598	
a1			4.5			0.177
a2	12.7		14.7	0.5		0.578
B		10.3			0.405	
b1		0.4			0.015	
b2		1.25			0.049	
C		4.65			0.183	
C1		0.5			0.019	
C2		2.4			0.094	
E		2.54			0.1	
F		6.3			0.248	
H		3.6			0.141	
I2	1.45		1.75	0.057		0.068
I3	0.80		1.20	0.031		0.047
L		2.8			0.110	

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



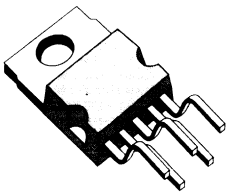
TO220AB



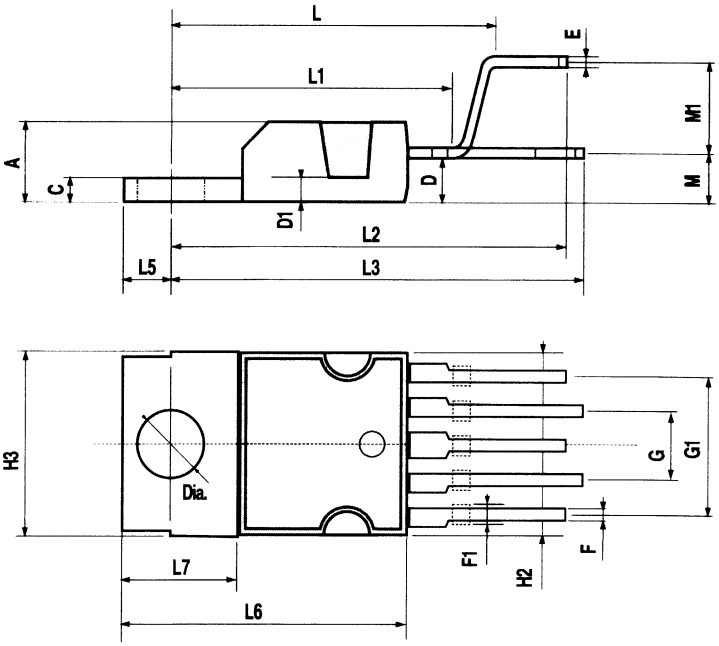
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.8		1.05	0.031		0.041
F1	1		1.4	0.039		0.055
G	3.2	3.4	3.6	0.126	0.134	0.142
G1	6.6	6.8	7	0.260	0.268	0.276
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		17.85			0.703	
L1		15.75			0.620	
L2		21.4			0.843	
L3		22.5			0.886	
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
M		4.5			0.177	
M1		4			0.157	
Dia	3.65		3.85	0.144		0.152

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Pentawatt V

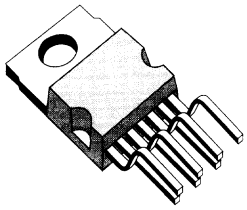


P010E

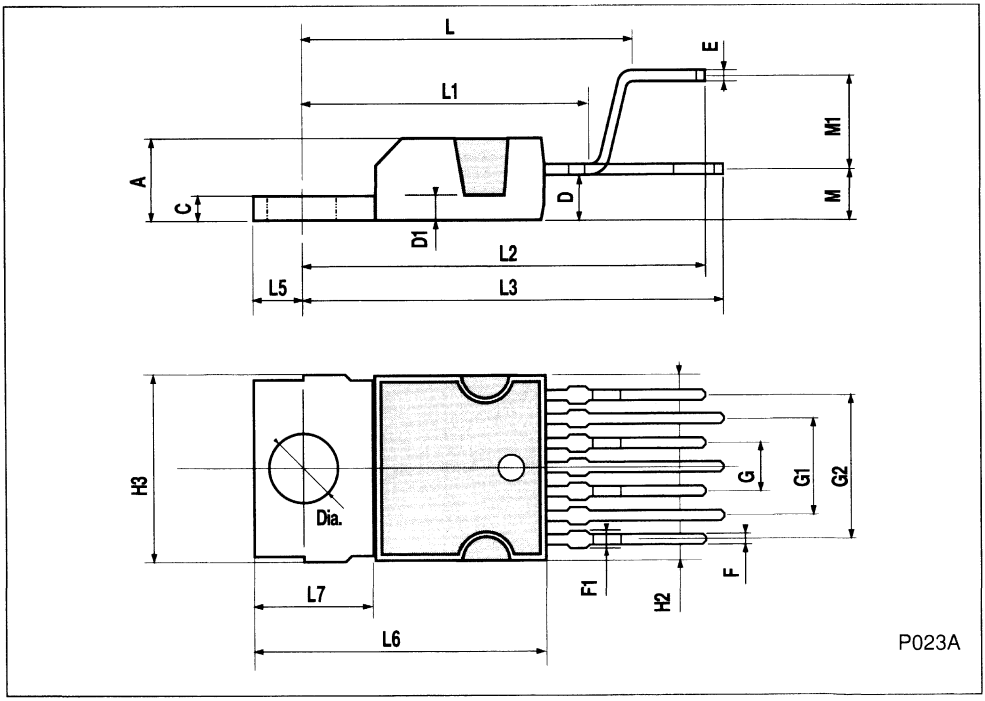
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.6		0.8	0.024		0.031
F1			0.9			0.035
G	2.41	2.54	2.67	0.095	0.100	0.105
G1	4.91	5.08	5.21	0.193	0.200	0.205
G2	7.49	7.62	7.8	0.295	0.300	0.307
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		16.97			0.668	
L1		14.92			0.587	
L2		21.54			0.848	
L3		22.62			0.891	
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
M		2.8			0.110	
M1		5.08			0.200	
Dia	3.65		3.85	0.144		0.152

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



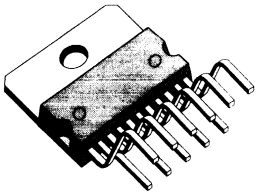
Heptawatt V



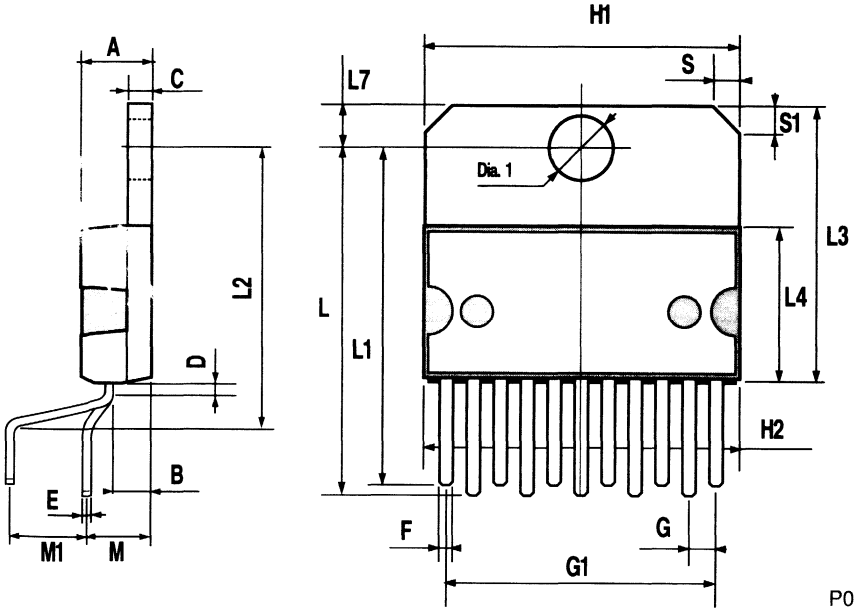
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
D		1			0.039	
E	0.49		0.55	0.019		0.022
F	0.88		0.95	0.035		0.037
G	1.57	1.7	1.83	0.062	0.067	0.072
G1	16.87	17	17.13	0.664	0.669	0.674
H1	19.6			0.772		
H2			20.2			0.795
L	21.5		22.3	0.846		0.878
L1	21.4		22.2	0.843		0.874
L2	17.4		18.1	0.685		0.713
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
M	4.1	4.3	4.5	0.161	0.169	0.177
M1	4.88	5.08	5.3	0.192	0.200	0.209
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Multiwatt11 V

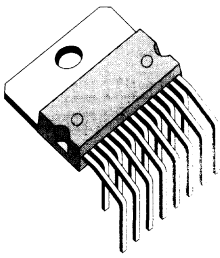


P017A

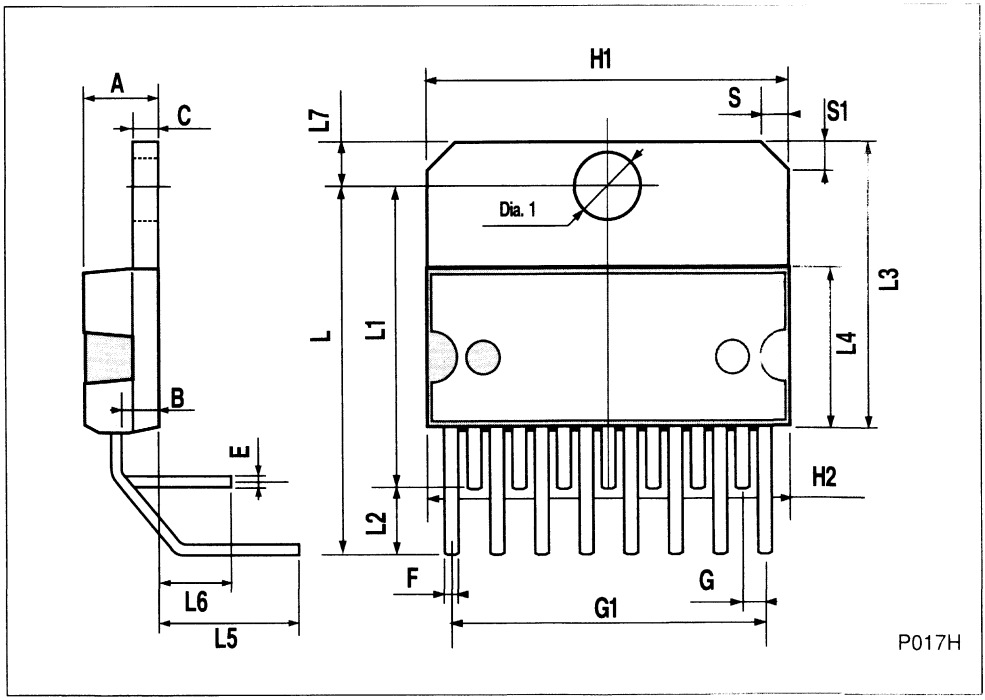
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
E	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.14	1.27	1.4	0.045	0.050	0.055
G1	17.57	17.78	17.91	0.692	0.700	0.705
H1	19.6			0.772		
H2			20.2			0.795
L		20.57			0.810	
L1		18.03			0.710	
L2		2.54			0.100	
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L5		5.28			0.208	
L6		2.38			0.094	
L7	2.65		2.9	0.104		0.114
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



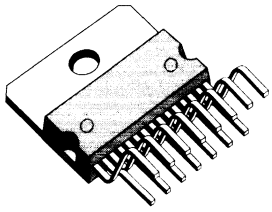
Multiwatt15 H



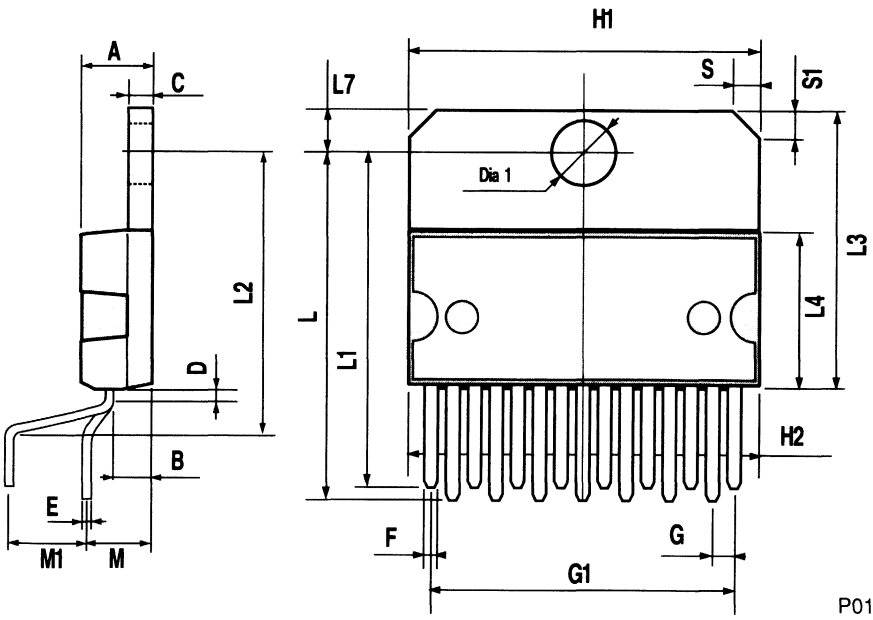
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
D		1			0.039	
E	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.14	1.27	1.4	0.045	0.050	0.055
G1	17.57	17.78	17.91	0.692	0.700	0.705
H1	19.6			0.772		
H2			20.2			0.795
L	22.1		22.6	0.870		0.890
L1	22		22.5	0.866		0.886
L2	17.65		18.1	0.695		0.713
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
M	4.2	4.3	4.6	0.165	0.169	0.181
M1	4.5	5.08	5.3	0.177	0.200	0.209
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



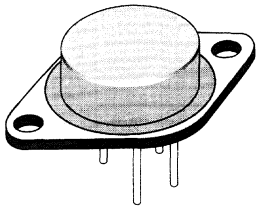
Multiwatt15 V



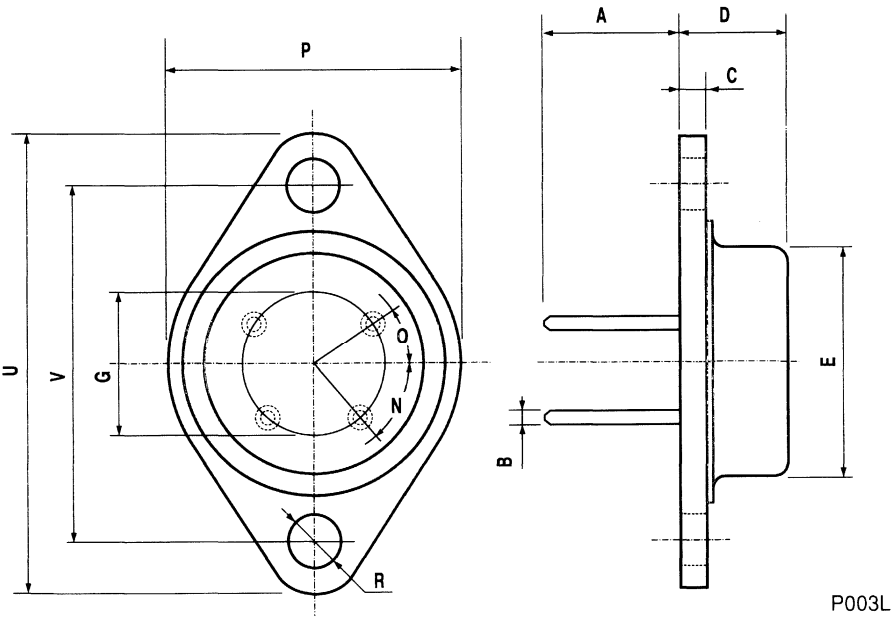
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		11.8			0.46	
B		1			0.39	
C			2.5			0.098
D			9.6			0.37
E			20			0.078
G		12.7			0.50	
N	50° (typ.)					
O	30° (typ.)					
P			26.2			1.03
R	3.88		4.20	0.15		0.16
U			39.5			1.55
V		30.1			1.18	

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



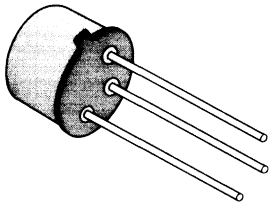
TO3 (Four Leads)



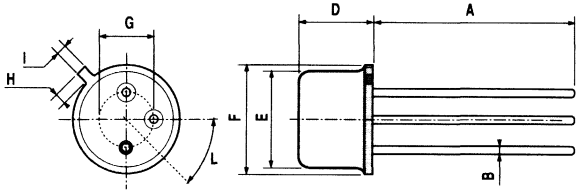
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	12.7			0.500		
B			0.49			0.019
D			6.6			0.260
E			8.5			0.334
F			9.4			0.370
G	5.08			0.200		
H			1.2			0.047
I			0.9			0.035
L	45° (typ.)					

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



TO-39

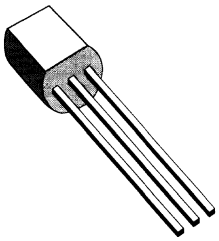


P008B

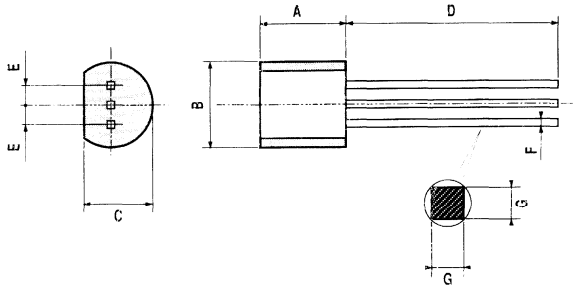
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.58		5.33	0.180		0.210
B	4.45		5.2	0.175		0.204
C	3.2		4.2	0.126		0.165
D	12.7			0.500		
E		1.27			0.050	
F	0.4		0.51	0.016		0.020
G	0.35			0.14		

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



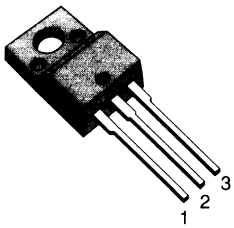
TO-92



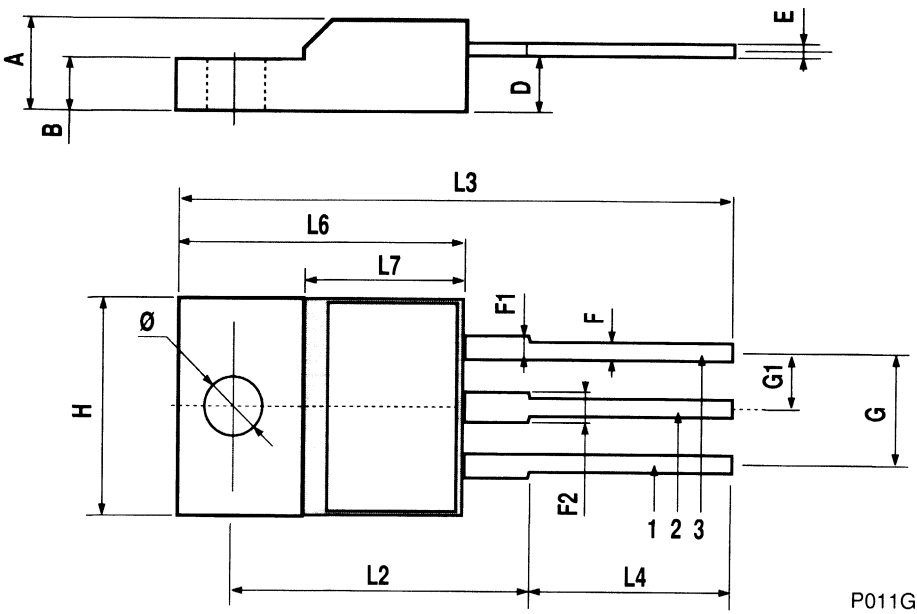
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.4		0.7	0.015		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		3.66
Ø	3		3.2	0.118		0.126

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



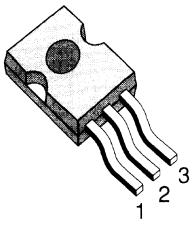
ISOWATT220



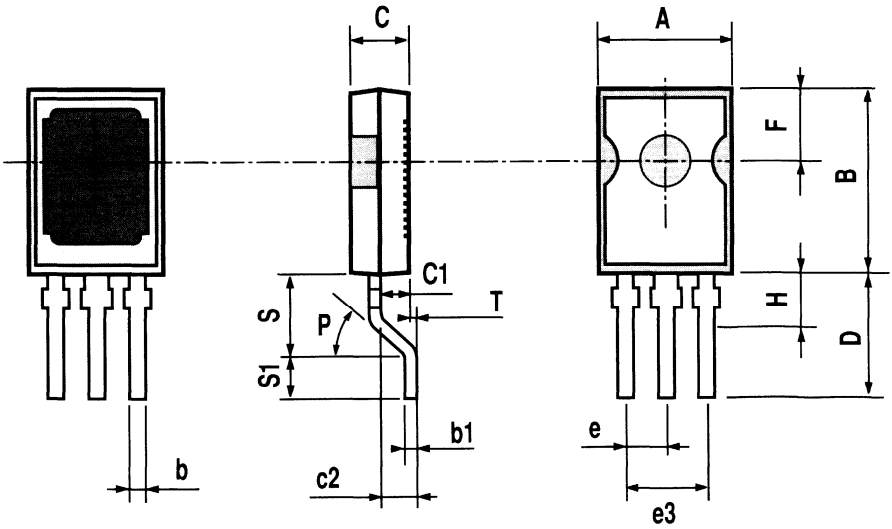
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	7.4		7.8	0.291		0.307
B	10.5		11.3	0.413		0.445
b	0.7		0.9	0.028		0.035
b1	0.49		0.75	0.019		0.030
C	2.4		2.7	0.094		0.106
c1		1.2			0.047	
c2		1.3			0.051	
D		6			0.236	
e		2.2			0.087	
e3		4.4			0.173	
F		3.8			0.150	
H			2.54			0.100
P	45° (typ.)					
S		4			0.157	
S1		2			0.079	
T		0.1			0.004	

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SOT-194

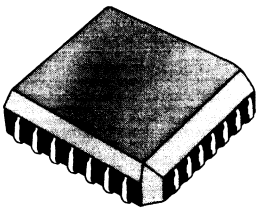


P032B

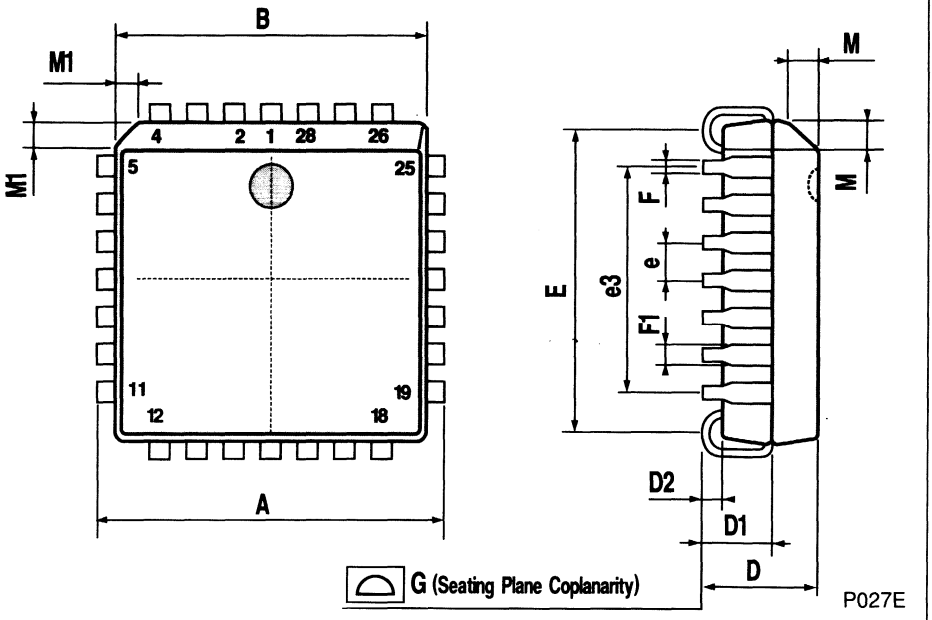
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	12.32		12.57	0.485		0.495
B	11.43		11.58	0.450		0.456
D	4.2		4.57	0.165		0.180
D1	2.29		3.04	0.090		0.120
D2	0.51			0.020		
E	9.91		10.92	0.390		0.430
e		1.27			0.050	
e3		7.62			0.300	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.24			0.049	
M1		1.143			0.045	

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



PLCC28



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